

# 3L\_2D

- Time Resolved  $e^+/e^-$  Light in 2-Dimension
- Goal of this proposal is to build a real time 2x7 array acquisition system (FPGA-based) to study bunch-by-bunch transverse instabilities using the mid-infrared light emitted by synchrotron acceleration from  $e^+/e^-$  DAFNE main ring bending magnets
- Presenter: Alessandro Drago
- Preventivi CSN-V 2013
- LNF - 03/07/2012



# Scientific Framework and International contest

The project has a strong technological content. It contains relevant R&D's in the detector area and involve important know how.

Many researches require ADVANCED 2D detector technologies:

- **beam diagnostics** for basic research with state-of-the-art time resolved uncooled IR detectors
- **e-cloud studies**, these devices may monitor in real time the vertical blow up of individual bunches in a circular accelerator
- **SuperB** IR or x-ray applications

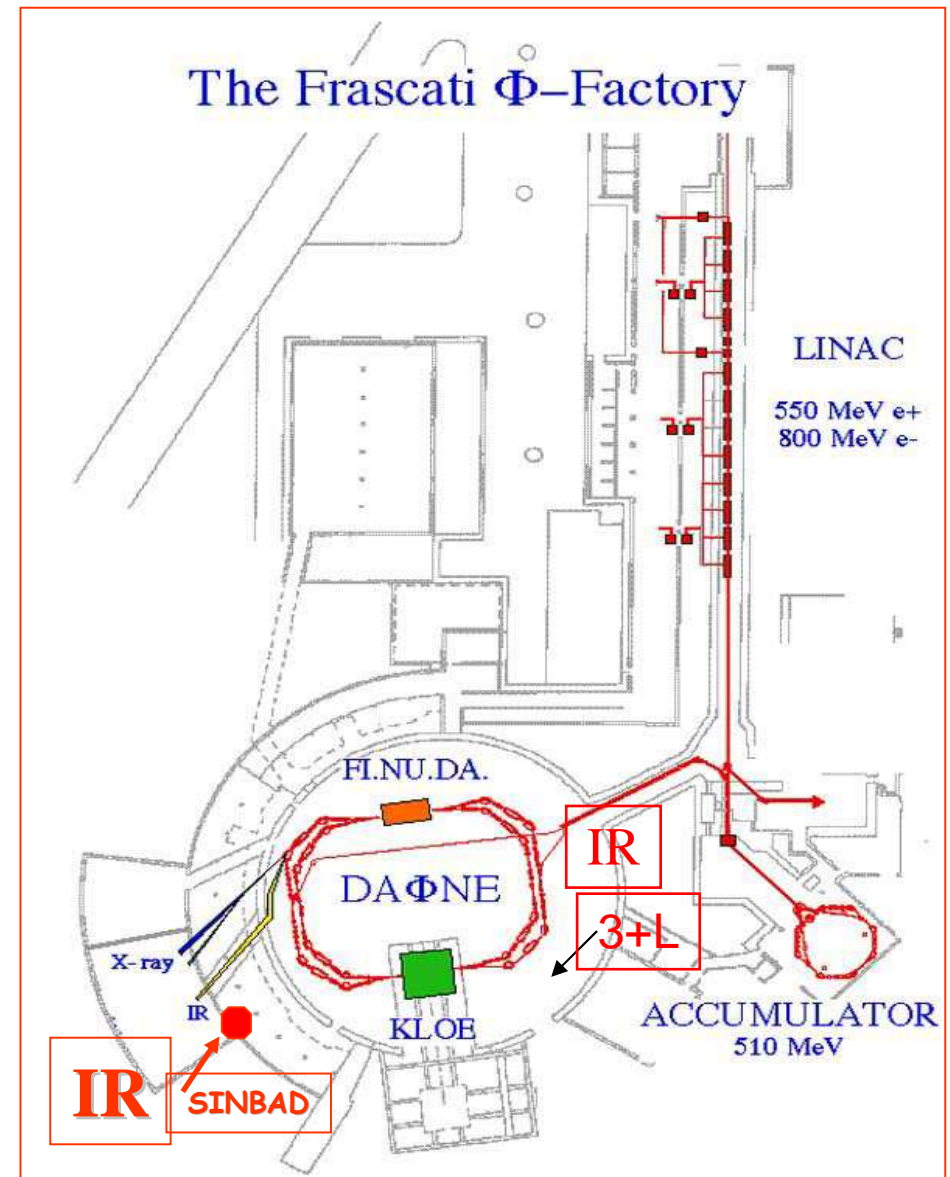
These project may have impact on R&D of UV and soft X-ray 2D detectors (e.g., diamond and/or graphene based devices may share the same FAST electronics)

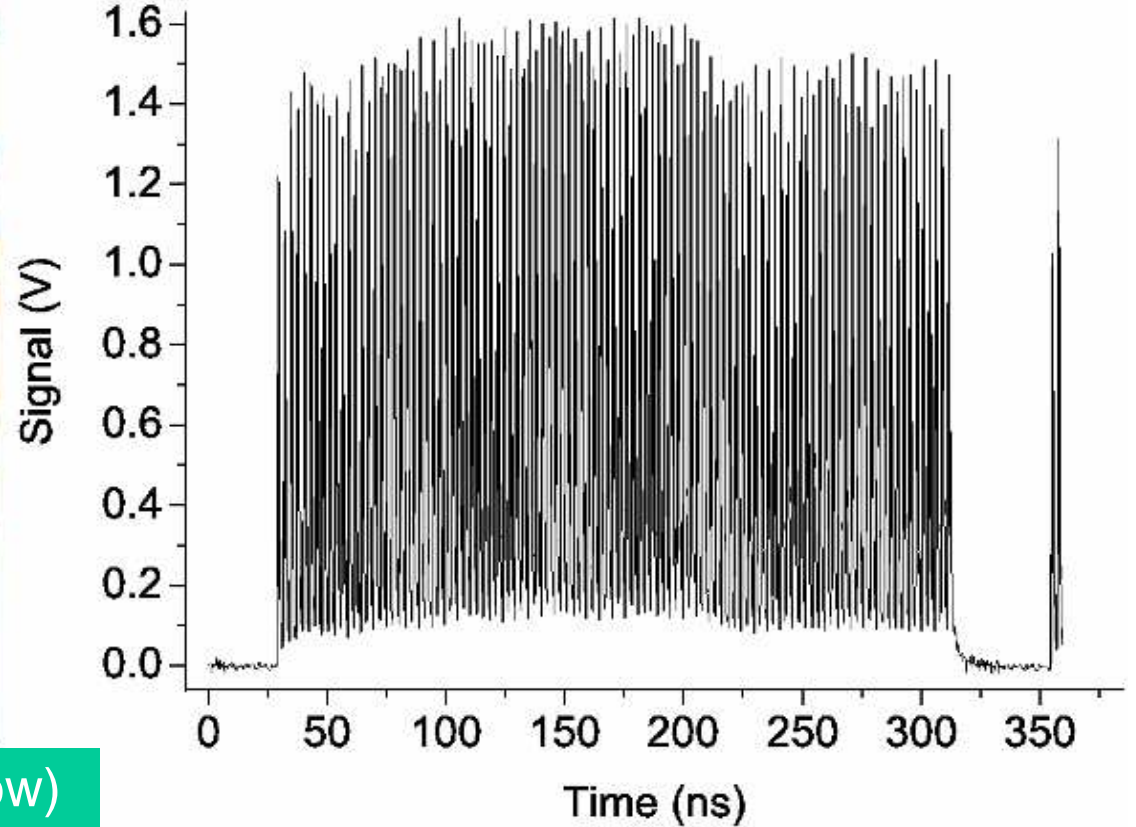
IMPORTANT INDUSTRIAL COOPERATION: Vigo that has already reliably collaborated to our R&D with state-of-art devices is interested to write a MOU with INFN.

POSSIBLE International collaborations at SR facilities: Diamond & HLS (China)

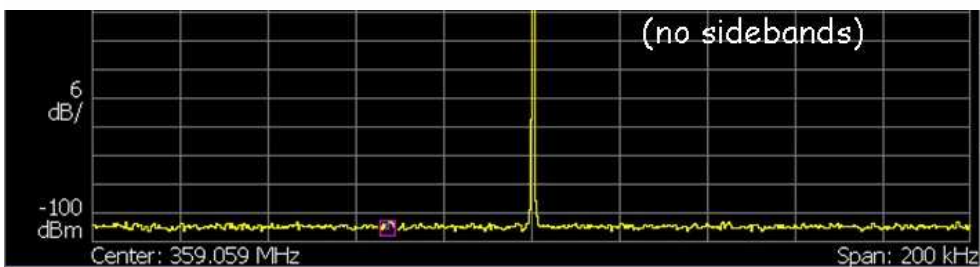
# Past experience on longitudinal IR detectors

- The 3L\_2D proposal collects legacy and experience of several previous experiments of CSN5, 3+L (2007-2009), SFEEED (2010), Time (2011) and also of NTA-ILC.
- 3+L (Time Resolved e+ Light) is a beam diagnostics experiment, funded by the INFN V-th National Scientific Committee in the years 2007-2009, and set-up on one of the bending magnet of the DAΦNE positron ring.
- 3+L experiment has collected the IR synchrotron radiation emission and focus the radiation on a small spot where fast single pixel detectors have been used to perform real-time bunch diagnostics. Several **longitudinal** measurements have been carried out using different IR detector.

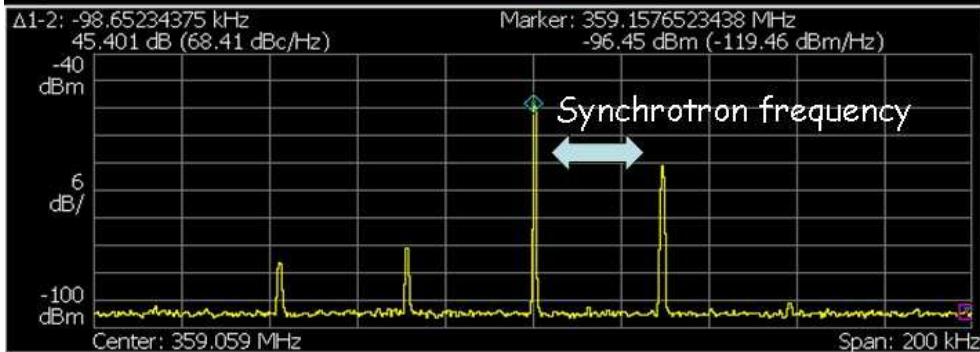




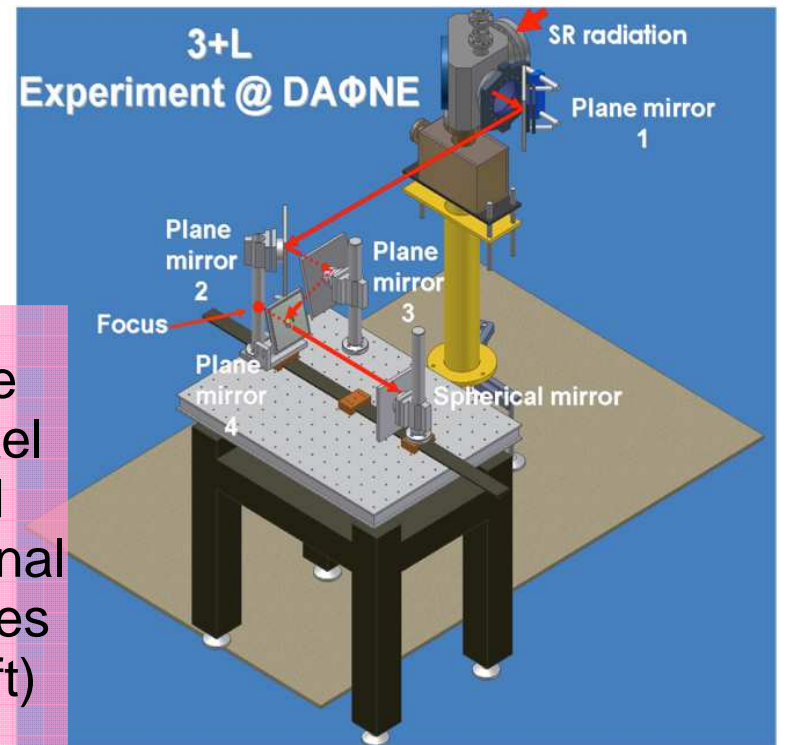
Longitudinal feedback on/off (picture below)



Tektronix RSA 3303A 4/4/2007 7:14:09 PM FREE RUN  
 Frequency: 359.059 MHz RBW: 200 Hz  
 Span: 200 kHz Trace 1: (Average) 10 / 10  
 Input Att: 20 dB Trace 2: (Off)



3+L beamline with single pixel detector and beam longitudinal behavior studies using LFB (left)

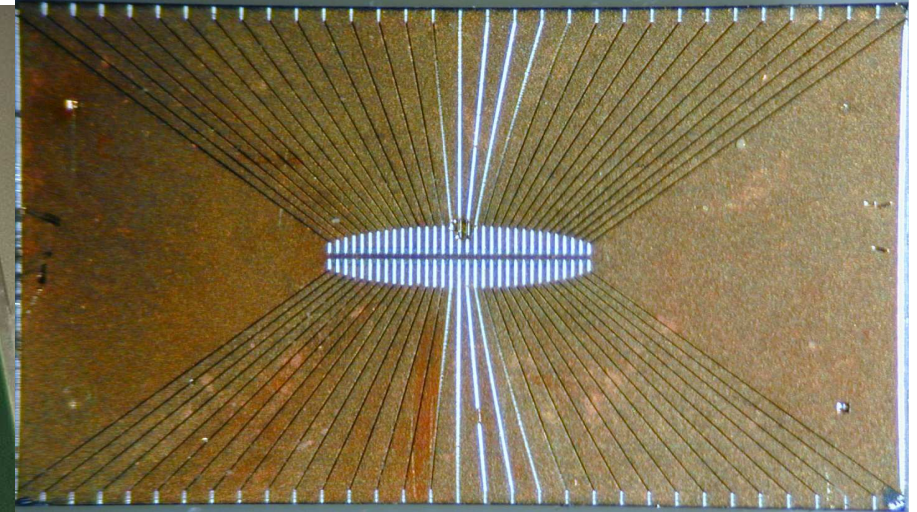
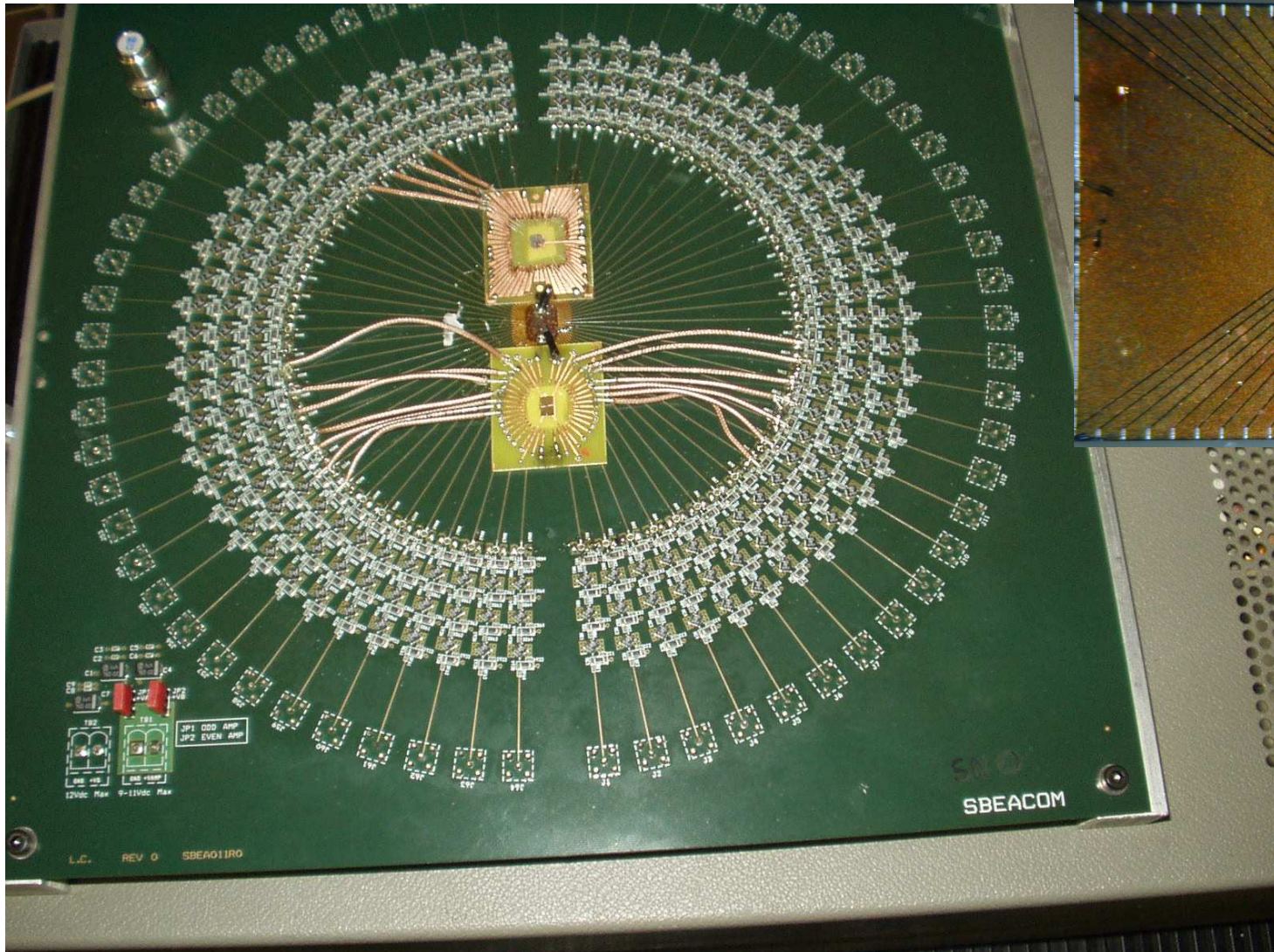




# 2D experiment short description

- An experimental array detector working in mid-infrared has been built in collaboration with the VIGO System company.
- After 2009, efforts have been dedicated to characterize a prototype of a 2x32 IR array detector to monitor the bunch-by-bunch **transverse** (mainly vertical) behavior of the e<sup>+</sup> beam.
- The device is an HgCdTe (grown on a GaAs substrate) array semiconductor that consists of 2x32 fast pixels operating at room temperature. Each element has a size of ~50x50 μm<sup>2</sup> and a rise time of <1 ns.
- The array detector has been assembled on an analog board with three stages of amplifiers giving 60 dB gain for each of 64 input channels.
- The goal is to attempt the first bunch-by-bunch transverse diagnostics of the e<sup>+</sup>/e<sup>-</sup> DAΦNE bunches at IR wavelengths.
- A prototype board has been used for imaging and has been successfully tested at SINBAD-IR beam line. Data analyzed by a Master Degree thesis in physics (G.Zangari, 2011, UNIROMA1)
- On 3+L positron beam line, many problems in terms of space (board too large to be correctly and remotely positioned) and noise (not possible to shield the board due to missing space)

This (on the left) is the analog board designed and built in 2008. In the following years it has been used to collect 2D data at SINBAD infrared beam line. Evident problems are that the board is too large (32 x 32 cm) for many beamlines (for example at Hefei Light Source) and also to made the necessary connections of each pixel to the PCB using the INFN-Firenze bonding machine



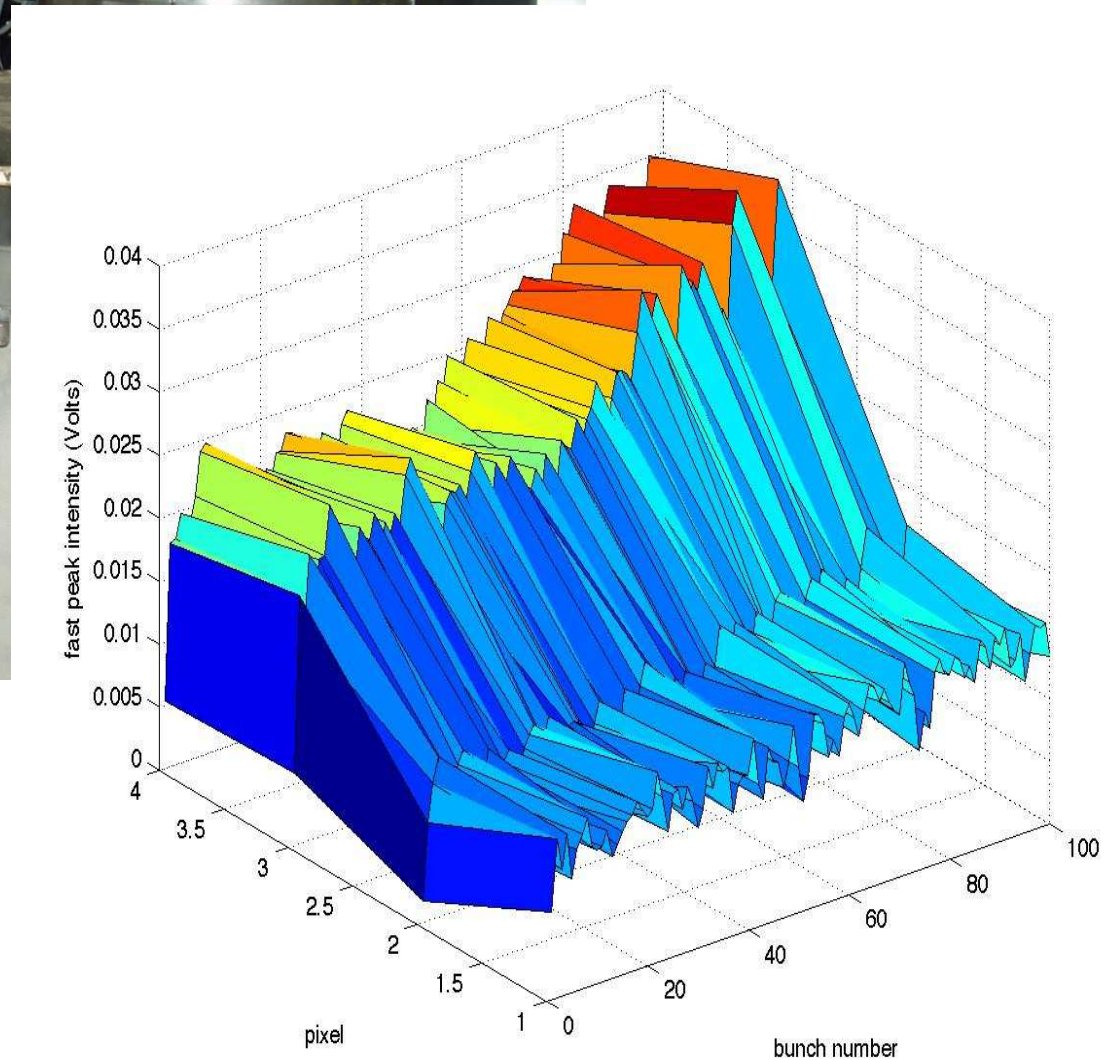
2D VIGO experimental semiconductor array detector (HgCdTe grown on a GaAs substrate - zoomed, up figure) and installed on a PCB with 60 dB amplifiers for each pixel signal (on the left)





A. Bocci makes  
data taking:  
SINBAD-IR  
beamline @ DAFNE  
( July 2009 )

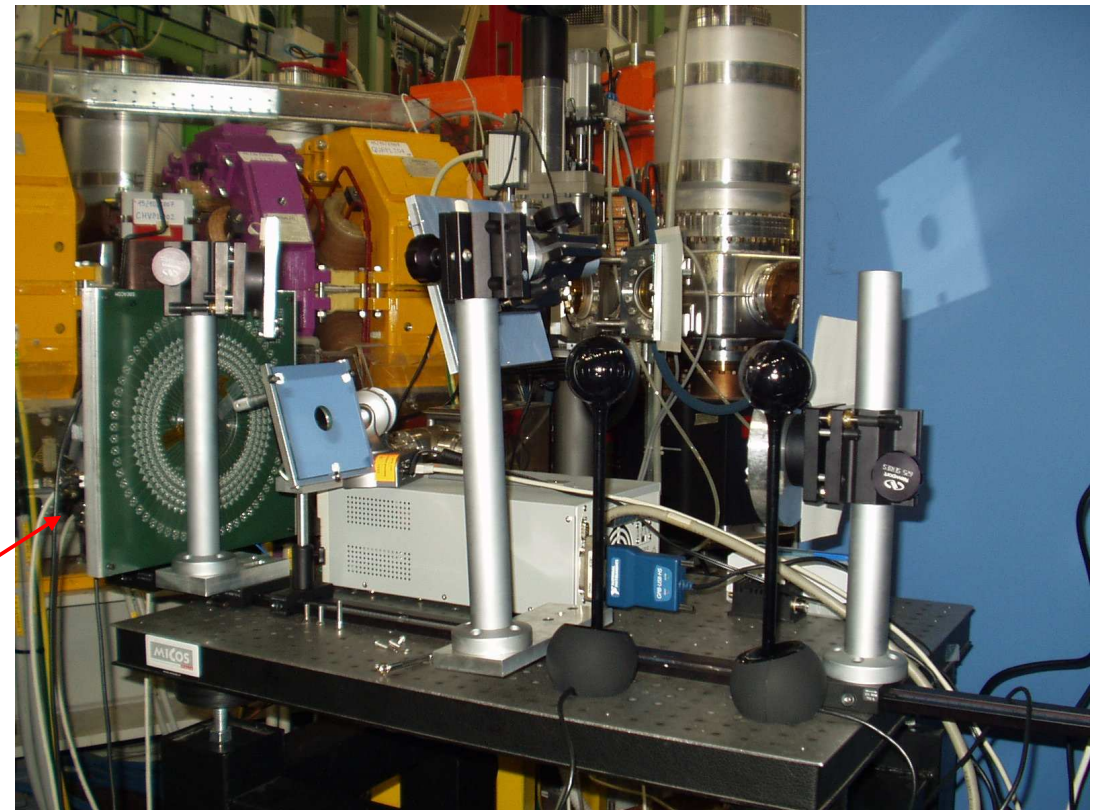
2D Imaging data taking at  
SINBAD-IR from only 4  
pixels using a 4 channel  
oscilloscope. Not possible to  
acquire more pixels!



# First of all a new more compact analog module is necessary

The old analog module works well in term of amplification (60dB in three stages) & perfect skew between channels, but it is so large that makes almost impossible to use it (in the picture has been installed at 3+L positron beam line)

A new, more compact, module (only 16 inputs) is proposed for saving space & also suitable to be shielded.

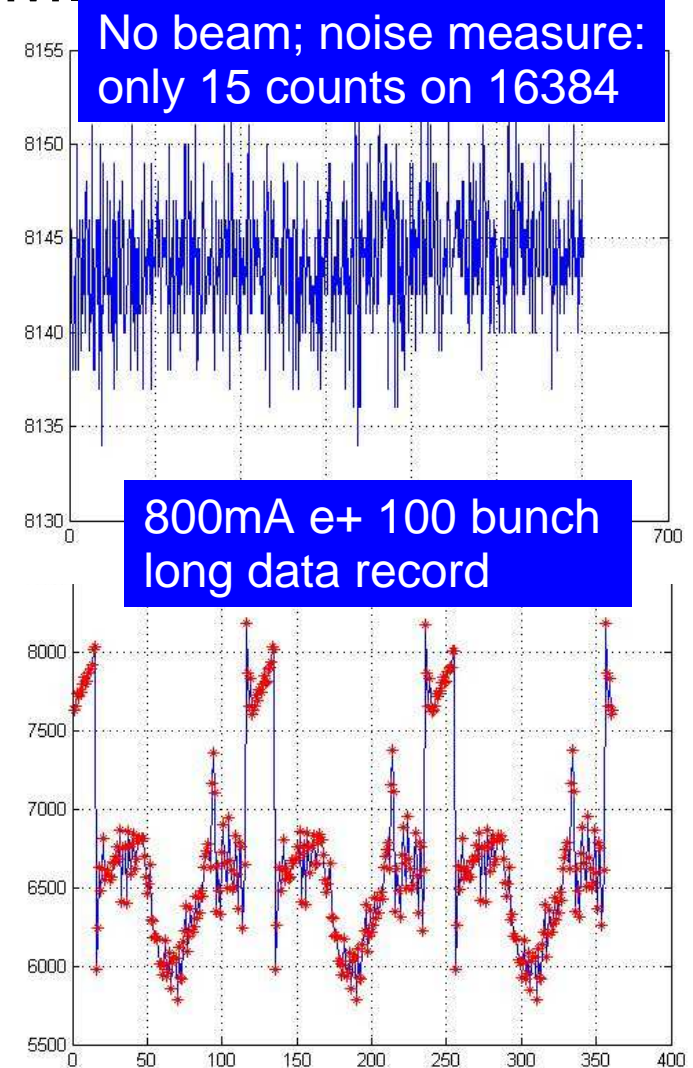
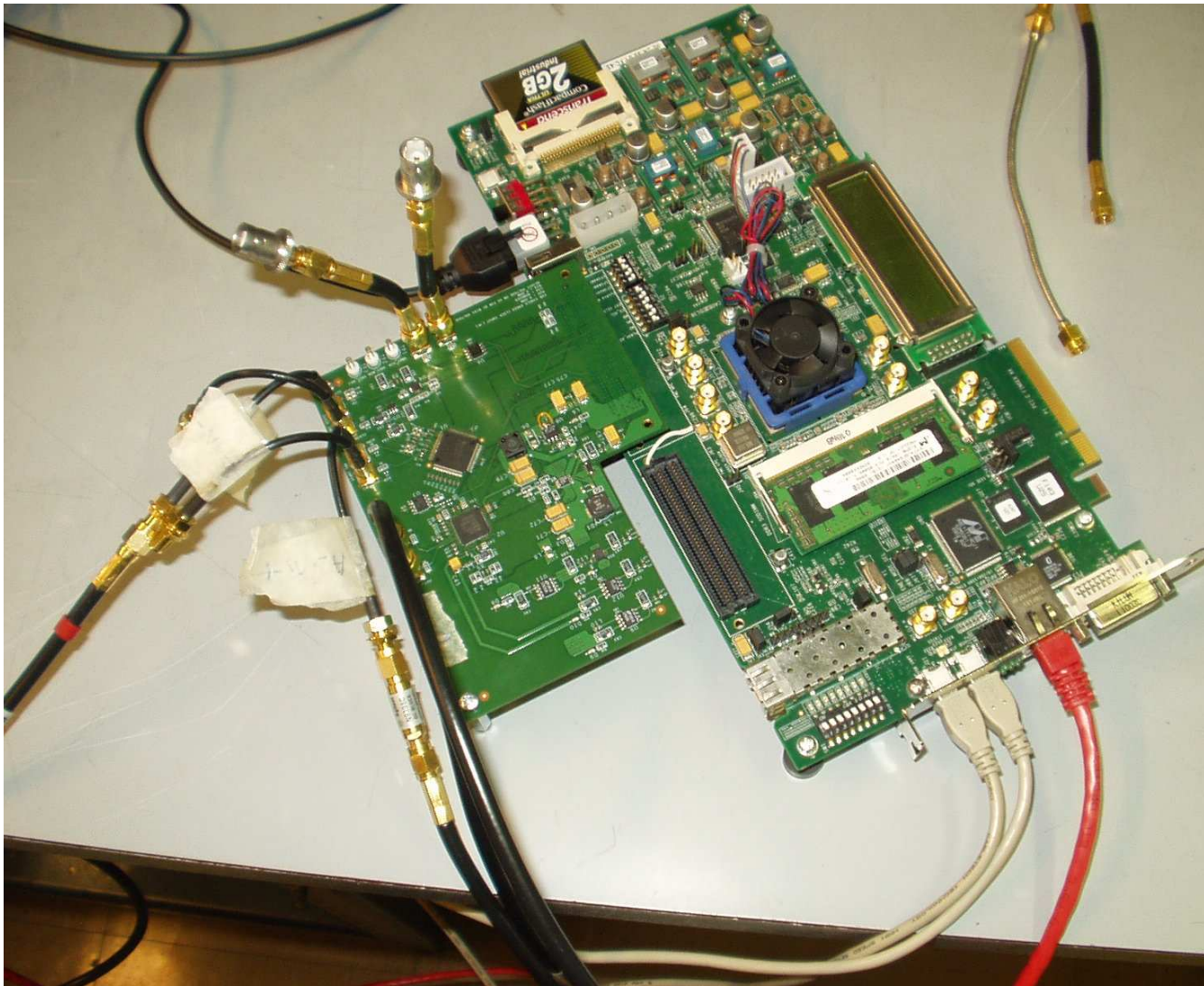




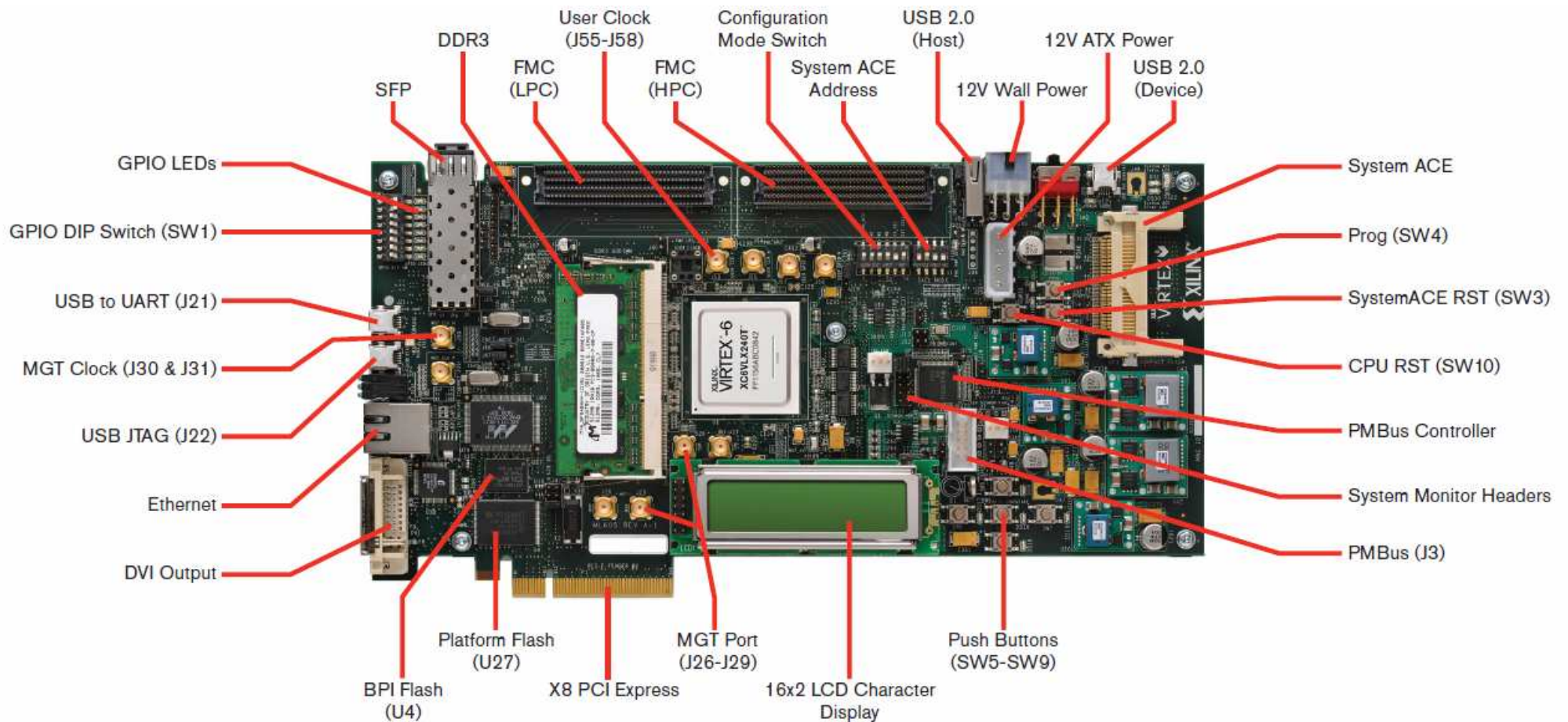
From digital acquisition point of view, this FPGA-based ML605 board by Xilinx has been tested.

It has a custom 14-bit ADC/DAC mezzanine board with FMC i/f (funded by SFEED, CSNV-2010).

The system has been used in May 2012 to acquire DAFNE e+ beam data from a BPM.



ML605 is very complete and powerful module built around a Virtex-6 FPGA with many interfaces ready to be used as ethernet@1Gbit/s, PCI express, USB, Jtag but it is also a low cost module





Home : Products : Boards & Kits : Virtex-6 FPGA ML605 Evaluation Kit

## Virtex-6 FPGA ML605 Evaluation Kit



[Click to Enlarge Image](#)  
[View Partner Profile](#)

~~\$4,995~~  
→ \$1,795

 [Buy from Xilinx](#)

**Lead Time : 2 Weeks**

 [Buy From Avnet](#)

 [Local Distributor](#)

### Part Number:

EK-V6-ML605-G  
EK-V6-ML605-G-J (for Japan)

### Accelerate Your Designs - Right Out of the Box

#### Product Information

The Virtex®-6 FPGA ML605 Evaluation Kit includes all the basic components of hardware, design tools, IP, and a pre-verified reference design for system designs that demand high-performance, serial connectivity and advanced memory interfacing. The included pre-verified reference designs and industry-standard FPGA Mezzanine Connectors (FMC) allow scaling and customization with daughter cards.

#### What's Included

- ML605 XC6VLX240T-1FFG1156 Evaluation Board
- ISE® Design Suite: Logic Edition
  - Device locked to the Virtex-6 LX240T FPGA
- Documentation
  - Hardware Setup Guide
  - Getting Started Guide
  - Hardware Users Guide
  - Reference Design and Example User Guide
  - Schematics and PCB Files
- Reference and Example Designs and Demos
  - Base Reference Designs
  - Base Reference Design Interface and Demo
  - Board Diagnostic Demo
  - PCI Express® Gen2 (x4) Test Design
  - PCI Express Gen 1 (x8) Test Design
  - DDR3 Memory Interface Design
  - ChipScope™ Pro Serial IO Toolkit IBERT Transceiver Test Design
  - MultiBoot Reference Design featuring Fail Safe
- Cables & Power Supply
  - Universal 12V Power Supply
  - 2 USB Cables
  - Ethernet Cable

ML605 price

1795 USD

That is

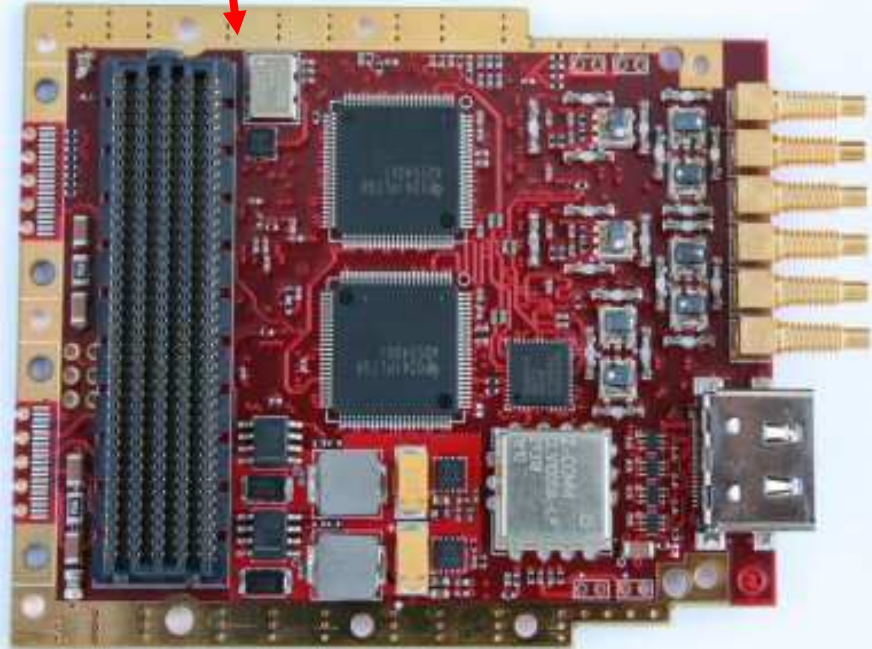
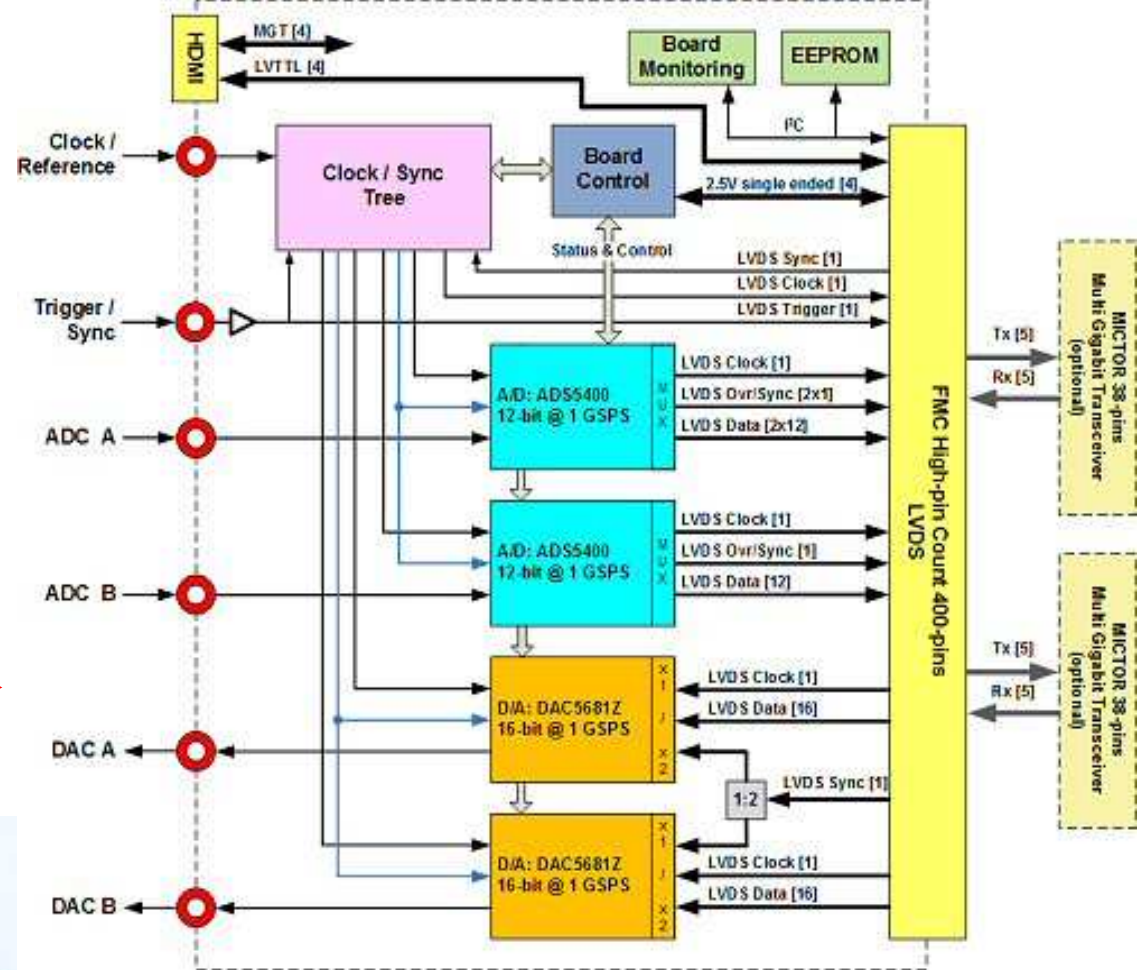
1430 euro

Buying 7  
boards  
gives a

total of

10 k euro

The FMC110 board by 4DSP company is based on FMC (FPGA Mezzanine Card) bus, very recent and innovative form factor.



Coax connectors are SSMC, a type not currently used at LNF. So there is an extra-cost to interface them





Quotation #	Q120612156
Date	June 12, 2012

# Quotation

Attention of:	Alessandro Drago	Sales contact:	Fabio Ancona Fabio.ancona@4dsp.com Tel: +39 3491766760
Company:	INFN, Italy		

We have the pleasure of quoting for the following parts:

Qty	Part number/Description	Lead time	Unit price	Extended price
05	FMCI10-2-1-1-1	3-4 weeks (*)	€ 3.996,00	€ 19.980,00
01	<b>FMC-ML605-BSP-SA</b> Reference design with Ethernet on ML605 (FPGA firmware and host software)	1 week	€ 0,00	€ 0,00
01	<b>FMC-ML605-BSP-PCIE</b> Reference design with PCIe interface on ML605 (FPGA firmware and host software)	1 week	€ 1.200,00	€ 1.200,00
<b>Total quotation value</b>				<b>€ 21.180,00</b>

Notes:

**Please EMAIL the purchase order to [Fabio.ancona@4dsp.com](mailto:Fabio.ancona@4dsp.com)**

(\*) Delivery time: 1-2 weeks if stock available on order date

Prices good for 30 days from date shown, lead time valid for 5 days from date shown. This quotation is subject to our terms and conditions of trading. All prices quoted are exclusive of VAT.

Payment terms are within 30 days of invoice date for customers with approved credit. If you should require further information please contact me at any time.

Carriage charges will be charged at the appropriate rate according to the method of dispatch requested. Where no method is requested 4DSP will select the delivery method.

	Hardware	Software/Firmware
Basic Warranty (Included)	1 year from date of shipment	90 days from date of shipment
Extended Warranty (Optional, 20% of the original price)	2 year from date of shipment	1 year from date of shipment

Fabio Ancona

On behalf of: **4DSP.**

Scheda con due coppie  
 di ADC e DAC  
 Con interfaccia FMC  
 Utilizzabile con scheda  
 Xilinx ML605

Costo 4 keuro (x scheda),  
 X 7 moduli → 28 k euro

Pacchetto sw x utilizzo della  
 Interfaccia PCI express  
 1200 euro

FROM [elvira.papa@vmsgroup.it](mailto:elvira.papa@vmsgroup.it)

Oggetto: Re: Fwd: Re: informazioni PC con slot PCIe

# Low-cost pc motherboard that can accept 7 PCI-express boards on the bus and can be used as main processing unit

Scusi volevo indicarle anche:

**ACER MOD. VERITON M6610G (I7/RAM 4GB/HD1000MB/WIN 7PRO/N.1 PCI/N, 1PCI EXPRESS 16X) EURO 907,00** ←

Saluti  
elvira papa

Il 08/06/2012 14.13, VMS'S Group srl - Elvira Papa ha scritto:

Buongiorno,  
come anticipato Le propongo:

**HP MOD. 8200 (I7/RAM 4GB/HD1000MB/WIN 7PRO/N.3 PCI/N, 2PCI EXPRESS 16X) EURO 1040,00** ←

Il 06/06/2012 15.48, drago ha scritto:

avrei cortesemente bisogno da Lei anche di una quotazione per un altro PC con almeno due slot PCI "standard".  
Se possibile con una CPU tipo i7 o comunque di fascia alta e tutti gli accessori: disco 1 Terabyte, unita' lettura/scrittura DVD, mouse, tastiera, monitor e windows pre-installato con disco diviso in due partizioni.

La ringrazio in anticipo,  
cordiali saluti

Alessandro Drago  
INFN-Frascati

Buongiorno,  
come da accordi di seguito indicazioni pc:

**CABINET ASUS MOD. TA-B12  
SCHEDA MADRE ASUS MOD P6T7-WS SUPERC.  
ALIMENTATORE 500W  
SCHEDA GRAFICA ASUS MOD. EAH5450 A 1GB PCIE  
PROCESSORE CORE I7  
MEM 4GB  
MASTERIZ. ASUS MOD. DRW24B5ST  
HD 1000 TB WESTER DIGITAL  
TASTIERA INGLESE HP MOD DT527A  
MOUSE WIRELESS  
OEM - WINDOWS 7 PROFESSIONAL (VERSIONE INGLESE)**

**COSTO 1.140,00 + IVA** ←

a disposizione per qualunque info  
saluti  
elvira papa

Il 30/05/2012 11.23, Alessandro Drago ha scritto:

Salve,  
come da comunicazione telefonica intercorsa le chiedo informazioni relative ad un personal computer con almeno 5 slot PCIeexpress.  
Le allego la foto della scheda-madre P6T7 della ASUS che ne ha 7. Grazie

Cordiali saluti  
Alessandro Drago





# Timing module

- A 14 channels data acquisition system that works in parallel needs an efficient clock and trigger management.
- A custom module with functionality of distributing and timing the 14 DAS has to be designed & built.
- The goal is to be able to de-skew individually the sampling frequency for each channels and also to interface the start acquisition trigger.
- If programmed adequately, this module can make the data acquisition for the longitudinal or for the transversal signal detection.

# Richieste economiche

Progetto su due anni: primo anno assemblaggio sistema, progetto schede e primo data taking da e- su linea SINBAD (non necessaria remotizzazione e meno rumore perche' posta fuori della sala DAFNE), secondo anno remotizzazione, schermatura e data taking da e+ sulla linea 3+L (posta internamente alla sala DAFNE).

Richieste ai servizi: SELCED (per assistenza progetto/assemblaggio schede)

## Acquisti per il 2013

1)	Computer (2 con PCIe e 1 con PCI standard)	3.32 k euro + IVA
2)	Scheda ML605 (x7)	10 k euro + IVA
3)	Scheda FMC110 (x7)	28 k euro + IVA
4)	Pacchetto software per FMC 110	1.2 k euro + IVA
5)	Connettori tipo SSMC e SMA, cavi	2 k euro + IVA
6)	Realizzazione circuito stampato modulo analogico 16 canali	3 k euro + IVA
7)	Realizzazione circuito stampato del modulo di timing	5 k euro + IVA
8)	Assemblaggio meccanico / movimentazioni	10 k euro + IVA
9)	Componentistica elettronica	5 k euro + IVA
10)	Missioni estero (conferenza e contatti Vigo)	2.5 k euro
11)	Missioni Italia (workshop e contatti Firenze)	2.5 k euro

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**Totale**

**87749,2 (incl. IVA 21%) euro**

**[ 72.52 k euro + IVA]**



# Personale Ricercatore e Tecnologo

Alessandro Drago (Resp.Naz, Primo Tecnologo) 100%

Augusto Marcelli (Primo Ricercatore) 20%

Mariangela Cestelli Guidi (Art.23) 20%

Emanuele Pace (Univ.Firenze / Ass. LNF) 20%

&

Alessio Bocci (CNA - University of Seville, Spain)

**Totale: 1.6 FTE Ricercatore/Tecnologo**

# Bibliography

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- [6] A. Bocci *et al.*, *The Time Resolved Positron Light Emission (3+L) Experiment: A Novel Diagnostics Tool for the DAΦNE Positron Ring*, LNF-09/15(R), 2009.
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