Testing the 16-ch Trigger Module at LNGS

WP5 Meeting - 05/05/2026

- The module is fully assembled, missing only four connections of ‘future use’ IO’s to the front panel.
- Communication with the RaspberryPi board tested and working. Thanks to Stefano.
- Write operations into the configuration registers (now some with 16 bits) tested and working (low level and using the MIDAS control interface).
- Initial tests have been done with the MAJORITY logic and the 16 input channels (using a 2nd FPGA board as a pulse generator).
- The Majority logic works well for 15 input channels.
- CHANNEL_0 input not working properly to generate the *TriggerOut* pulse. Under investigation…
- Next steps:
  - The Signal Tap Logic Analyzer tool, embedded in the Quartus Prime IDE, will be used to verify the signals also inside the FPGA in real time.
  - Perform more tests changing the CHANNEL_0 assigned to different IO pins in the FPGA.