INFN/AExxx, LAL-xxx, SLAC-R-xxx

Super$B$ Detector Technical Design Report

Abstract

This report describes the technical design detector for Super$B$.

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7.1.2 Geometrical Constraints

The Drift Chamber inner radius is constrained by the final focus cooling system and by the Tungsten shield surrounding it to $R_{inner}^{DCH} = 250\,mm$, the outer radius is constrained to $R_{outer}^{DCH} = 805\,mm$ by the DIRC quartz bars. The total length available for the Drift Chamber is of $L^{DCH} = 2700\,\mathrm{mm}$. As the rest of the detector, the drift chamber is shifted by the nominal *BABAR* offset (367 mm) with respect to the interaction point.

Simulation studies performed on several signal samples with both high ($e.g.\, B \to \pi^+\pi^-$), and medium-low ($e.g.\, B \to D^*K$) momentum tracks indicate that:

a) as expected, momentum resolution improves as the minimum drift chamber radius R_{min} decreases, see Fig. 7.1; R_{min} is actually limited by mechanical integration constraints with the cryostats and the radiation shields.

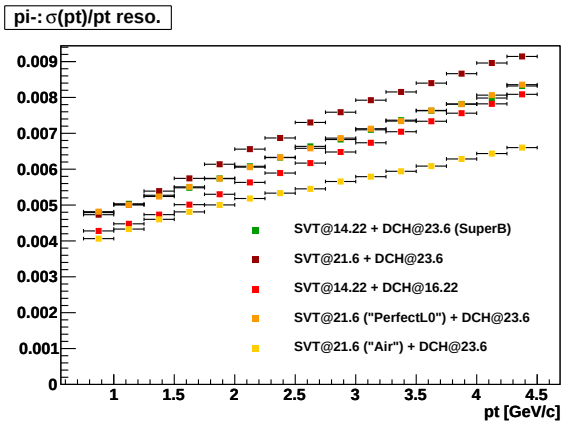

Figure 7.1: Track momentum resolution for different values of the drift chamber inner radius.

b) The momentum and especially the $\mathrm{d}E/\mathrm{d}x$ resolution for tracks going in the forward or backward directions are clearly affected by the change in number of measuring samples when the chamber length is varied by $10 - 30\,\mathrm{cm}$. However the fraction of such tracks is so small that the overall effect is negligible.

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The *BABAR* drift chamber operational record has been quite good, both for what performances and reliability is concerned; however there are possible paths of improvements that we have explored to try and design a drift chamber with performances yet better that the *BABAR* one.

7.2.1 Cluster Counting

A possibility being considered to improve the performances of the gas tracker is the use of the *cluster counting* method. Signals in drift chambers are usually split to an analog chain which integrates the charge, and to a digital chain recording the arrival time of the first electron, discriminated with a given threshold. The *cluster counting* technique consists instead in digitizing the full waveform to count and measure the time of all individual peaks. On the assumption that these peaks can be associated to the primary ionization acts along the track, the energy loss and to some extent the spatial coordinate measurements can be substantially improved. In counting the individual cluster, one indeed removes the sensitivity of the specific energy loss measurement to fluctuations in the amplification gain and in the number of electrons produced in each cluster, fluctuations which significantly limit the intrinsic resolution of conventional $\mathrm{d}E/\mathrm{d}x$ measurements.

The ability to count the individual ionization clusters and measure their drift times strongly depends on the average time separation between them, which is, in general, relatively large in He-based gas mixtures thanks to their low primary yield and slow drift velocity. Other requirements for efficient cluster conting include good signal-to noise ratio but no or limited gas-gain saturation, high preamplifier bandwidth, and digitization of the signal with a sampling speed of the order of 1Gs/sec. Finally, it is necessary to extract online the relevant signal features (*i.e.*the cluster times), because the DAQ system of the experiment would hardly be able to manage the enormous amount of data from the digitized waveforms of the about 10 000 drift chamber channels.

7.2.2 Cell Design and Layer Arrangement

The drift chamber cell design must optimise the homogeneity of the electric field inside the cell; this is particularly relevant with the non-saturated mixture we intend to use. Another critical parameter is the overall wire material, and an optimal use of the drift chamber volume for accommodating as many sense wires as possible.

The design for the Super*B* drift chamber employs small rectangular cells arranged in concentric layers about the axis of the chamber. The z coordinate of the track hits is measured by orienting a subset of the wire layers at a small positive or negative stereo angle, ε, relative to the chamber axis. Such a measurement is performed with precision $\sigma_z \simeq \sigma_{R\phi}/\tan\varepsilon$. As in *BABAR*, four consecutive cell layers are grouped radially into a superlayer (SL). This will allow to keep the same *BABAR* algorithms for track-segment finding, both in the track reconstruction and in the formation of the drift chamber trigger.

The rectangular cell layout ensures the most efficient filling of the drift chamber volume, because the transition between superlayers of opposite stereo angles does not require to leave free radial space, nor layers of field-shaping guard wires. Indeed, the latter are only used at a radius inside the innermost SL and at a radius outside the outermost SL. Such guard wires also serve the purpose to electrostatically contain very low momentum electrons produced from background particles showering in the DCH inner cylinder and in the SVT, or background-related backsplash from detector material just beyond the outer SL.

Simulations[1] have shown that a field:sense wire ratio of 3:1 ensures good homogeneity of the electric field inside the cells. In this config-

uration each sense wire is surrounded by 8 field wires.

The radial positions of the stereo wires in the j-th layer vary with the z coordinate, being larger at the endplates than at the center of the chamber by the "stereo drop" $\delta_j \equiv R_j^{\rm EP} - R_j$. The cell shapes are most uniform when $\delta_j = \delta$ is a constant for all layers: this is obtained by changing the stereo angle with the radius, by the relation $\tan\varepsilon_j = 2\delta/L_j\sqrt{2R_j^{\rm EP}/\delta - 1}$ (L_j is the chamber length at layer j).

Additional constraints used to determine the cell layout include:

a) the number of cells of width w_j on the j-th sense wire layer, $N_j = 2\pi R_j/w_j$, must be an integer number;

b) to keep a fixed periodicity in signal and high voltage distribution, it is convenient that the number of cells per layer is incremented of a fixed quantity ΔN when passing from a SL to the next one. For SL's with k layers of cells h cm high, $\Delta N = 2\pi hk/w$, therefore $w = m\pi$ with m a suitable constant;

c) since the density of both physical tracks and background hits is higher at smaller radii, we choose to have smaller cells in the innermost layers of the drift chamber.

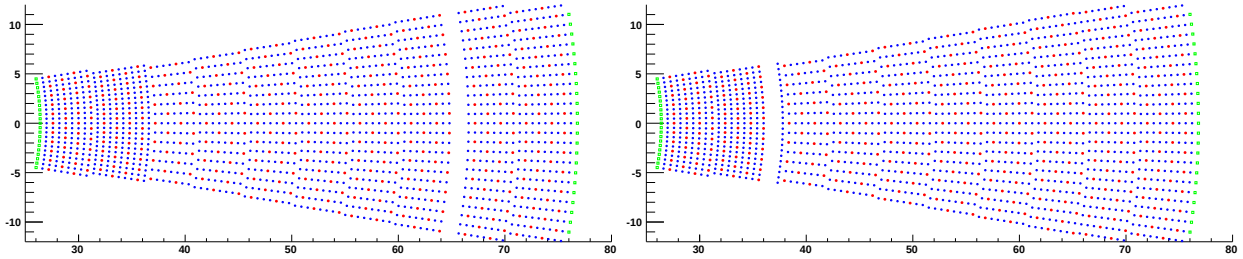
A possible choice for the drift chamber layout, obtained for $h = 12$ mm, $k = 4$, $\delta = 12$ mm, $m_{\rm in} = 3$ for the 2 innermost SLs and $m_{\rm out} = 6$ for the remaining ones is shown in Table 7.1. In this arrangement there are a total of 7392 cells in the drift chamber, and 1600 cells in the two innermost SL's. The first two superlayers have an axial orientation; this minimizes the occupancy from background hits due to low-momentum spiraling electrons which traverse the drift chamber along its axis (see Sec.7.1.3). The two external super layers are also axial. The fact that the innermost and outermost super layers do not exhibit the stereo drop deformation δ matches the axial simmetry of the inner and outer drift chamber cylinders. The six internal SL's have a stereo arrangement, with angles as shown in the Table. The corresponding wire map in the region with angle $|\varphi| < 10°$ is shown in Fig. 7.2 at the center of the chamber (a) and at the endplates (b).

Table 7.1: A possible drift chamber SL structure, specifying the number of cells per layer, the radius at the center of the chamber of the innermost sense wire layer in the SL, the cell widths, and wire stereo angles, which vary over the four layers in a SL as indicated.

SL	$N_{\rm cells}$	R [mm]	width [mm]	Angle [mrad]
1	184	276.0	9.4 – 10.7	0
2	216	324.0	9.4 – 10.5	0
3	124	372.0	18.8 – 20.7	+(78 – 81)
4	140	420.0	18.8 – 20.5	−(82 – 84)
5	156	468.0	18.8 – 20.3	+(85 – 88)
6	172	516.0	18.8 – 20.2	−(89 – 91)
7	188	564.0	18.8 – 20.1	+(92 – 94)
8	204	612.0	18.8 – 20.0	−(94 – 96)
9	224	672.0	18.8 – 19.9	0
10	240	720.0	18.8 – 19.8	0

It is seen that the axial-stereo transition between SL 2 and SL 3 creates some additional radial space close to the endplates, which disappears at the DCH center. The opposite happens at the stereo-axial transition between SL 8 and SL 9. It is clear that the electric field should be as uniform as possible across layers to ease the drift chamber calibration; however, simulation studies have shown that the field distortion at the two transition radii is moderate and does not require to be compensated by layers of guard wires, which would add material and reduce the sensitive volume.

An alternative choice is to have $m_{\rm in} = 4$: in this case there are 1200 cells in the first two SL's, with widths in the range $1.26 - 1.42$ cm; the remaining layers would be identical to the ones shown in Tab. 7.1. Total wire count in this case is therefore 6992 cells.



(a) Cell layout at the drift chamber center.

(b) Cell layout at the drift chamber endplates.

Figure 7.2: A possible cell layout of the Super$B$ drift chamber with $m_{\rm in} = 3$, $m_{\rm out} = 6$. Open green squares: guard wires; open blue circles: field wires; full red circles: sense wires. Note how the boundary regions after the first 8 layers of axially strung wires in the inner part of the chamber and after the following 24 layers of stereo layers map differently at the drift chamber center and at the endplates.

7.2.3 Gas Mixture

The gas mixture for the Super$B$ drift chamber is chosen to allow optimal resolution in the measurement of both momentum and energy loss. It must also be operationally stable (*e.g.*, have a wide high voltage plateau), and be little sensitive to photons with $E \leq 10\,\text{keV}$ to help controlling the rate of background hits (see Sec. 7.1.3). Finally, aging in the chamber should be slow enough to match the projected lifetime of a typical High Energy Physics experiment (about 15 years). These requirements already concurred to the definition of the *BABAR* drift chamber gas mixture, (80%He-20%iC_4H_{10}). Indeed, a high Helium content reduces the gas density and thus the multiple scattering contribution to the momentum resolution. Good spatial resolution calls for high single electron efficiency and for small diffusion coefficient. The effective drift velocity in Helium-based gas mixtures is typically non saturated, therefore it depends on the local electric field, and on the Lorentz angle. This dependences can be taken into account by a proper calibration of the space-time relations and in principle do not pose limits to attaining the required spatial resolution. In practice, a careful choice of the cell shape (see the dicussion in Sec. 7.2.2), and a small value of the Lorentz angle are an advantage.

To match the more stringent requirements on occupancy rates of Super$B$, it could be useful to select a gas mixture with a larger drift velocity in order to reduce ion collection times and so the probability of hits overlapping from unrelated events. The *cluster counting* option would instead call for a gas with low drift velocity and primary ionization. As detailed in Section7.2.4, R&D work is ongoing to optimize the gas mixture.

7.2.4 R&D and Prototype Studies

In order to optimize the gas mixture for the Super$B$ environment, and to asses both the feasibility and the operational improvements for the *cluster counting* technique a complete R&D program has been proposed. The program includes both beam tests and cosmic ray stands to monitor performancs of *ad hoc* built prototypes. While the $\mathrm{d}E/\mathrm{d}x$ resolution gain of the cluster counting method is in principle quite sizeable compared to the traditional total charge collection, the actual capability of the measured number of cluster might not retain the same analyzing power, due to a pletora of experimental effects that should be studied in detail so that the energy loss measurement derating should be assessed and, if possible, cured.

A few prototypes were built and operated to answer the above mentioned questions.

7.2.4.1 Prototype 1

The first one is a small aluminum chamber, 40 cm long, with a geometry resembling the the original *BABAR*drift chamber. It consists of 24 hexagonal cells organized in six layers with four cells each. A frame of guard wires with appropriate high voltage settings surrounds around the cell array to ensure uniformity of the electric field among the cells. The device was operated in a cosmic ray test stand in conjunction with an external telescope, used to extapolate the track trajectories with a precision of 80 μm or better . Different gas mixtures have been tried in the prototype: starting with the original *BABAR* mixture (80%He-20%iC_4H_{10}) used as a calibration point, both different quencher proportions and different quenchers have been tested in order to assess the viability of lighter and possibly faster operating gases.

As an example, the correlation between the extrapolated drift distance and the measured drift time is shown in Fig. 7.3 for a 75%He-25%C_2H_6 gas mixture. The result of a fit to a 5^{th}-order Chebychev polynomial is superimposed to the experimental points. Track-fit

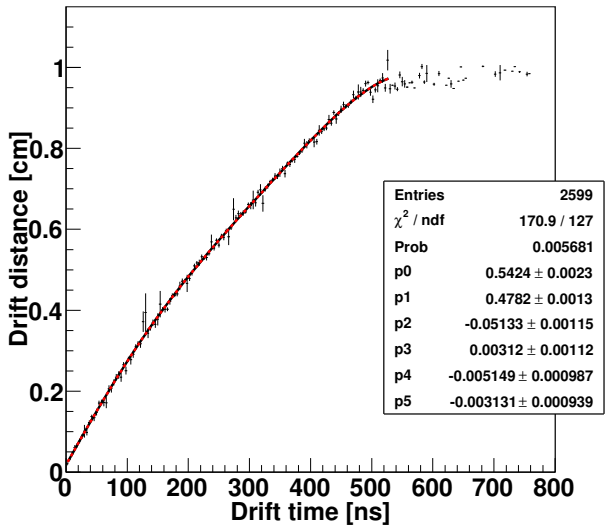


Figure 7.3: Track distance vs. drift time in a cell of the prototype. The line is the result of a fit with a 5^{th}-order Chebychev polynomial.

residuals and spatial resolution as a function of the drift distance for the same gas mixture are show in Fig. 7.4.

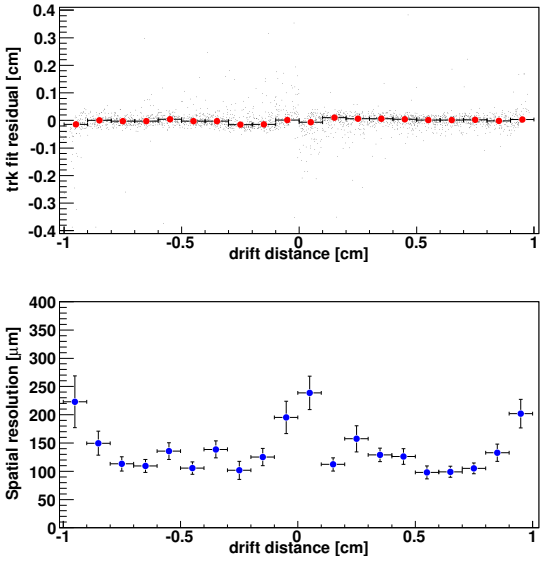


Figure 7.4: Track fit residuals (top) and spatial resolution (bottom) as a function of the drift distance.

7.2.4.2 Prototype 2

A full-length drift chamber prototype was designed, built and commissioned to study *cluster counting* in a realistic environment, including signal distortion and attenuation along 2.5 meter long wires. The prototype, which is also meant to serve as a test bench for the final Front-End electronics and for the drift chamber trigger, is composed by 28 square cells with 1.4 cm side, arranged in eight layers and – as in the final Super$B$ drift chamber – with a field-to-sense wire ratio of 3:1. The eight layers have either 3 or 4 cells each, and are staggered by half a cell side to help reduce the left-right ambiguity. Tracks with angle $|\vartheta| \leq \pm 20°$ cross all the eight layers of the chamber. A set of guard wires surrounds the matrix of 28 cells to obtain a well-behaved field distribution at the boundary of the active detector volume. Most of the cells feature a 25 μm Gold-plated Molybdenum sense wire, while for reference seven cells in two adjacent layers are strung with a 25 μm Gold-plated

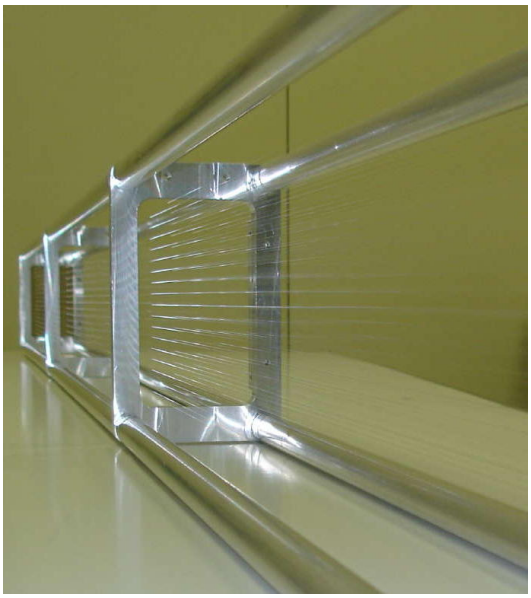


Figure 7.5: Prototype 2: detail of the strung wires.

Tungsten wire, traditionally used in drift chambers. The reason for using the Molybdenum wire is its lower resistivity, therefore smaller dispersion for pulses travelling along the wires. A picture of the chamber after stringing completion is shown in Fig. 7.5. The entire wire structure is enclosed in an Aluminum container 3 mm thick; three pairs of thin windows have been carved in the middle and at the extremities in order to have smaller amount of material in the path of low energy particles measured by the device. Four preamplifier boards are used to extract the cell signals. Each board serves seven channels, each with a transimpedence preamplifier (rise time of about 2.4ns), at a nominal gain of 8mV/fC and a noise of 2200 e rms. Each boards also has a test input, both unipolar and differential outputs (50 Ω– 110 Ω); the latter are used for a test implementation of the Drift Chamber first level trigger. A detail of the Faraday cage housing the FEE boards and of the signal and trigger cables is shown in Fig. 7.6.

The data collected with this prototype are fed into a switch capacitor array digitizer[1], which samples the wire signals at 1 GS/sec with and input BW$\geq$ 500 MHz. The challenge of detecting the ionization clusters in signals with a wide dynamic range and non-zero noise levels is apparent from the two sample waveforms shown in Figg. 7.7, recorded in the cosmic-ray setup. Hits associated to cosmic ray tracks reconstructed in the drift chamber prototype are used to compare the performances in the energy loss measurement of the traditional truncated mean algorithm and of the *cluster counting* method. Preliminary results when 10 samples from a single prototype cell are used to form a 70% truncated mean or to count the average number of clusters are shown in Fig. 7.8. In the experimental conditions of our test, *cluster counting* yields a 40-50% better relative resolution than the truncated mean method. Additional R&D efforts are ongoing to extend this encouraging result to different momentum regions, and study how the $K-\pi$ resolving power in the range of interest of Super$B$ ($|p| \leq 5$ GeV/c) improves with the *cluster counting* technique.

[1] CAEN V1742: http://www.caen.it/csite/CaenProfList.jsp?parent=13&Type=WOCateg

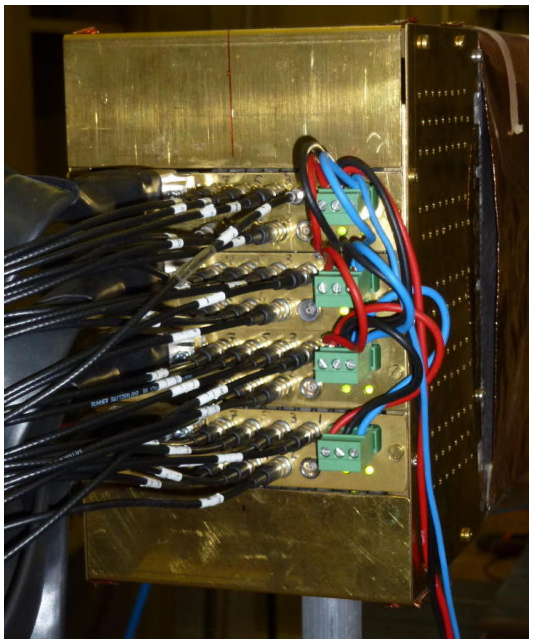
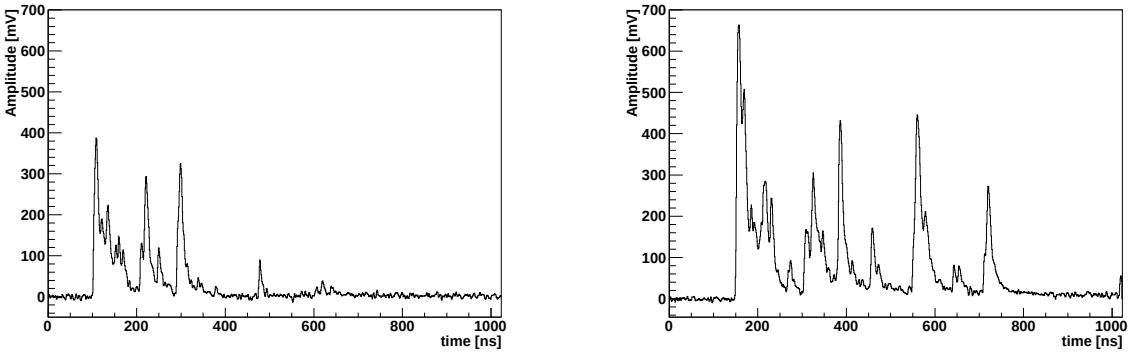


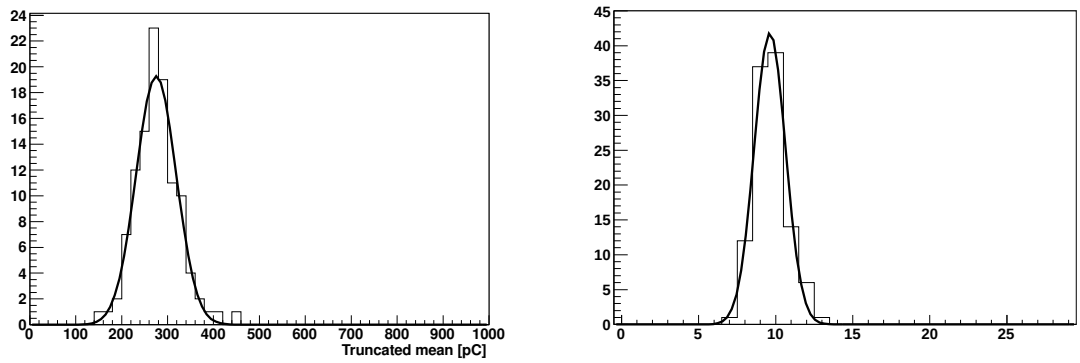
Figure 7.6: Prototype 2: FEE Faraday cage with signal and trigger cables.



(a) Sample waveform n.1

(b) Sample waveform n.2

Figure 7.7: Sample waveforms from two cells of the full-length drift chamber prototype.



(a) Average dE/dx distribution

(b) Average n. of clusters

Figure 7.8: Average dE/dx and number of clusters from 10 samples of a single cell belonging to a track reconstructed in the prototype.

7.2.4.3 Single Cell Prototype(s)

A single cell prototype, SW1, 2.7 m long has also been built. Both Proto 2 and SW1 are at the moment operational and collecting data on cosimc ray stands; both devices have been exposed to test beams, a 500 MeV/c electron beam Proto 2, a variety of pion and/or Kaon beams at various momenta SW1.

7.2.4.4 Aging studies: fields, gas gain

7.2.5 R&D Future Developments

- test beam with different particle species
- on-board feature extraction
- AOB

7.3 Mechanical Design

The drift chamber mechanical structure must sustain the wire load with small deformations, while at the same time minimizing material for the surrounding detectors. The structure is also required to ensure tightness for the gas filling the drift volume. We opted for a structure entirely in Carbon Fiber (CF) composite, with an approximately cylindrical geometry. A side view of the chamber is shown in Fig. 7.9.

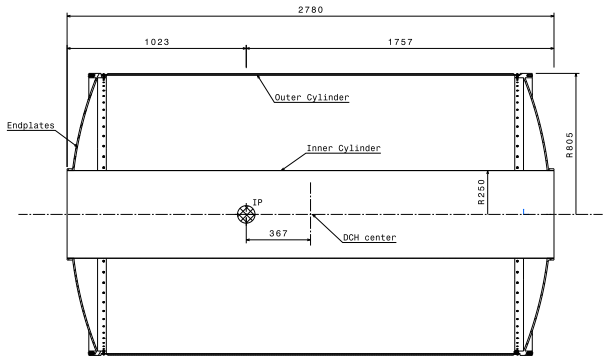


Figure 7.9: Longitudinal section of the DCH with principal dimensions.

7.3.1 Endplates

The wires defining the cell layout are strung between the two endplates, which are required to:

a) sustain the total wire load of XXXX tons (or N) (see sec. **??**) with minimal deformations;

b) be as transparent as possible to avoid degrading the performances of the forward calorimeter.

c) have XXXXX precisely machined holes to allow positioning the crimp feed-throughs with tolerances better than XXXX μm;

The endplates are two identical pieces of 8 mm thick CF composite with inner radius of 250 mm and outer radius of 805 mm. Deformations under load can be minimized using for the endplates a shaped profile. An optimization taking into account different constraints resulted in spherical convex ednplate, with a radius of curvature of 2100 mm. Two CF stiffening rings on the inner and outer rims help preventing radial (axial) deformations. An intermediate modulus carbon fiber (as T300 (XXXX), with a Young modulus of XXXXX) will be used. It is expected that the average material characteristics will be degraded by about 30 % or less after drilling the XXXX holes on the endplates. Detailed studies on this aspect will be performed on custom samples. The maximum displacements on the endplates is calculated to be less than 300 μm (Figure **??**).

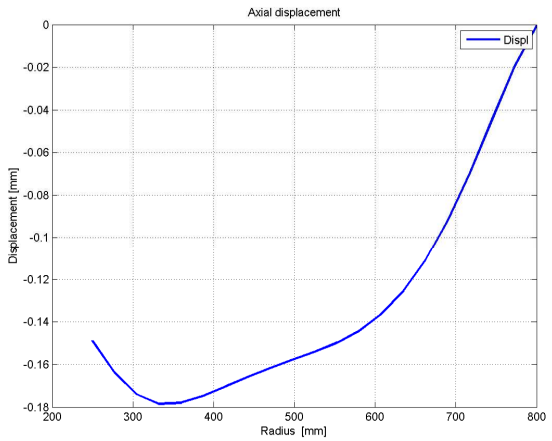


Figure 7.10: Displacement of each endplate due to the wire load.

7.3.2 Inner cylinder

The drift chamber inner cylinder should be as transparent as possible to minimize the multiple scattering degradation to the p_T measurement. For this reason it was designed as a non load-bearing structure: it must only guarantee gas tightness, and sustain possible differential pressures of the order o 10 mbar between the inside and outside of the chamber. It is a thin (200 μm) CF cylinder of 250 mm radius, with a 25 μm aluminum foil glued on it as RF shield. During the stringing phase the inner cylinder will be free to move longitudinally being fixed only to one endplate. Only after stringing, when all endplate deformations are settled, it will be glued to the other endplate.

7.3.3 Outer Cylinder

In addition to guaranteeing gas tightness and withstanding a differential pressure as the inner cylinder, the outer cylinder will also carry the wire load. It will be installed after completion of the wire stringing. To ease the construction and the mounting procedures, the cylinder is longitudinally divided in two half shells. Each shell consists of two 1 mm-thick CF skins laminated on a 6 mm-thick honeycomb core. Two thin alluminium foils, 100 μm on inside surface and 25 μm on outside surface, are glued to the shells to ensure the rf shield. The sandwich structure guarantees a high bendig stiffness and a high safety factor for global buckling.

7.3.4 Choice of wire and electrostatic stability

7.3.5 Feed-through design

7.3.6 Endplate system

7.3.6.1 Supports for on-detector boards

7.3.6.2 Cooling

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7.7.0.3 Gas monitoring system

7.7.0.4 On-line monitor

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7.8.2 Cable supports and routing

7.8.3 Access

7.8.4 Gas system

7.8.5 Off-detector electronics crates

7.8.6 High voltage crates

7.8.7 Installation and alignment

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[2] CLEO reference.

[3] M. Adinolfi *et al.* (KLOE Collaboration), *The tracking detector of the KLOE experiment*, Nucl. Instrum. Methods Phys. Res., Sect. A **488**, 51 (2002).

13 Subdetector Electronics and Infrastructure

Breton/Marconi/Luitz

13.1 Subsystem-specific Electronics

13.1.1 SVT Electronics

The full details of the SVT electronics has been given in chap. **??**. Here we recall the main features relevant for the data collection, trigger distribution, system programming and monitoring.

In the baseline SVT option, the detector will be equipped with double sided silicon strips (or striplets) in all layers. Custom front-end chips will be used to read the detector and transform as soon as possible the analog information of a particle traversing the detector in a digital one, characterized by position (layer, strip), energy deposit (signal time over threshold) and time. At least two different custom chips will be developed to handle separately the first layers (expecially layer 0), characterized by high occupancy and short strips (good signal/noise) and the external layers (layer 4 and layer 5) where the main concern is the length of the strips (worse signal/noise) and not the occupancy. Both front-end chips will have the same digital readout architecture and will present the same interface to the DAQ chain, although with different settings. Possible upgrades of the SVT internal layers might require to move to a pixellated detector, for which a different custom front-end chip will be designed. The digital architecture of the pixel chips, partially already develloped, will be based on the same general readout architecture so that from the point of view of trigger and DAQ system they will share the same interface.

Common characteristics of the chips will be capability to work both in data-push and data-pull mode, the presence of internal buffers to allow for a trigger latency up to 10 μs, the use of a periodic signal to time-tag the recorded hits, the serialized hit output and the chip programmability via (two) digital lines.

The full SVT data chain will therefore be able to provide and distribute all the signals, clocks, triggers, time-tagging signal to all the front-end chips in a system-wide synchronous way.

A sketch of the full data chain is given in Fig. 13.1. Starting from the detector and going to the ROM boards, the chain contains: a) the front-end chips mounted on an HDI placed immediately at the end of the sensor modules; b) wire connections to a transition card (signals in both directions and power lines); c) a transition card, placed about 50 cm from the end of the sensors, hosting the wire-to-optical conversion; d) a bidirectional optical line running above 1 Gbit/s; e) a receiver programmable board (front-end board: FEB).

Each HDI will host from 5 to 14 FE chips servicing a side of the silicon strip module (a so called ROS: Read-Out Section). All the chips will share the same input lines (currently: reset, clock, fastclock, trigger, time-stamp, registerIn) and at least a registerOut line. Programming of the chips can be done individually by addressing

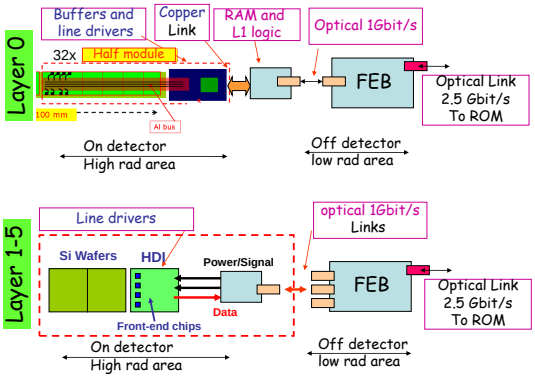

Figure 13.1: SVT Electronics

a sigle chip or via broadcast command sent to all the chips in an HDI. Hits will be serialised on a programmable number of lines (1,2,4 or 6) using the fastclock signal. Each HDI will have a maximum number of 16 output lines running at the fastclock rate.

The role of the transition card is threefold: a) it will distribute the power to the HDI, b) it will receive all the input signals for the front-end chips via the optical line connected to the programmable board and c) it will ship the data to the programmable board for data acquisition. For the inner layers (0-3) there will be a transition card for each HDI. For the outer layers (4-5) it will be possible to group the data of the two HDIs servicing the two sides of the same silicon sensor into the same transition card, reducing in this way the total number of optical links needed.

The received programmable board (FEB) will handle all the comunications with the front-end chips, the FTCS, the ECS and the upper DAQ systems. Each FEB board will be connected to a variable number of transition cards (up to 12 in the current design). Important and critical roles of this board are the clock distribution, the trigger handling and the data collection. The clock-like signals, such as an experiment clock (about 60 MHz), a fast clock (120-180 MHz) and a time-stamping clock (up to 30 MHz), have to be distributed in a system-wide synchronous manner. Special care will be taken to measure at each power-up the latencies of all the serializers and deserializers in the signal and DAQ chain so that the sent signals can be suitably adjusted in phase in order to have a system synchronous at the sensor (or front-end) level. The time-stamping clock will be used to time-tag the hits and can be different for the inner layers, where the high track rate requires short signal shaping times and short daq time windows and outer layers where the long strips and lower track rates allow for a longer shaping times (800 ns - 1 μs) and longer DAQ windows. The estimation of data volumes have been performed assuming a time-stamping of 30 ns period in the inner and outer layers. The acquisition window will be defined in a time window centered around the L1 trigger window and lasting at least 10 time-stamps (300 ns) for the inner layers and 33 time-stamps (990 ns) or more for the outer layers. The trigger request will be sent to the chips via the optical links. The most important function of the board is to collect the data coming out of the front-end chips both for monitoring and for the final daq. The data will be deserialized in the board and the redundant information will be stripped. A possible further data compression can be envisaged in order to reduce the final data volume. Finally the data will be sent-out via an optical link to a ROM module.

Data volumes. As discussed in the SVT chapter, the data rates and volumes are dominated by the background. In the design of the SVT front-end chips and DAQ chain, the latest background Bruno simulations have been considered at the nominal luminosity and a safety factor of 5 has been applied on the simulation results (design inputs). Due to the strong non-uniformity of the particle rate on the sensors, the front-end chip characteristics have been adapted to the peak hit rates, while the data volumes have been extracted from the mean rates for each layer. To evaluate the data rate a 150 kHz trigger rate with 10 μs of maximum latency and 100 ns of time jitter has been considered. An hit size of 16 bits is used as the FE chip output in the calculation that becomes 20 bits during serialization due to the 8b/10b protocol. The bandwidth needed by a layer0 ROS in a data-push configuration is of the order of 20 Gbit/s/ROS. A difficult-to-handle rate that moved us to consider a fully triggered SVT. In table 13.1 for each layer type the mean expected data load is shown.

For events accepted by the L1 trigger, the bandwidth requirement is only 1 Gbit/s and data from each ROS can be transferred on optical links to the front-end boards (FEB) and then to ROMs through the >8 Gbit/s optical readout links.

In total, the SVT electronics requires 18 FEBs and 18 ROMs, 18 optical links at 10 Gbit/s, 172 links at 1 Gbit/s (radiation

Table 13.1: Electronic load on each layer, Readout section and optical link.

Layer	Layer type	chips/ ROS	available channels	Backgnd (MHz/cm^2)	Gbits/trig (per GROS)	FE Boards	Event Size (kB)
0	striplet u	6	768	151	0.99	4	5.3
0	striplet v	6	768	151	0.99	4	5.3
1	strip z	7	896	14.0	0.56	1	2.2
1	strip phi	7	896	16.0	0.64	1	2.6
2	strip z	7	896	9.6	0.54	1	2.2
2	strip phi	7	896	10.3	0.58	1	2.3
3	strip z	10	1280	4.2	0.50	1	2.0
3	strip phi	6	768	3.0	0.36	1	1.5
4a	strip z	5	640	0.28	0.26	1	1.4
4a	strip phi	4	512	0.43	0.38	1	2.0
4b	strip z	5	640	0.28	0.26	1	1.4
4b	strip phi	4	512	0.43	0.40	1	2.1
5a	strip z	5	640	0.15	0.17	1	1.0
5a	strip phi	4	512	0.22	0.24	1	1.5
5b	strip z	5	640	0.15	0.17	1	1.0
5b	strip phi	4	512	0.22	0.24	1	1.5

hard). The average SVT event size is 88 kB, 30% coming only from the layer0.

13.1.2 DCH Electronics

13.1.2.1 Design Goals

The Super$B$ Drift Chamber (DCH) front-end electronics is designed to extract and process the about 8000 sense wire signals to:

- measure the electrons' drift times to the sense wires for the purpose of tracking (momentum of charged particles)
- measure the energy loss of particles per unit of length, dE/dx (particle identification)
- provide hits information to the trigger system (trigger primitives)

Concerning the energy loss measurement two options will be considered. The first one foresees the measurement of the sense wires integrated charge, discarding the highest values to remove the Landau tails (Standard Readout), while the second one is based on primary electron clusters counting (Sampled Waveforms). Because the front-end requirements for the two options are quite different each option will be discussed in a dedicated section.

13.1.2.2 Standard Readout - charge measurements specifications

The method is based on integrated charge measurements thus allowing the use of (relatively) low bandwidth preamplifiers. This makes the front-end chain less sensitive to noise pickup and instabilities, a plus condition in a system with a large number of channels.
The three main specification for charge measurement are: resolution, dynamic range and linearity.

Resolution Charge measurements for particle identification aims to measure, with a precision of the order of 7.5%, the particle most probable energy loss, despite the large fluctuations involved in single measurement.
The goal can be achieved by sampling many

times the collected charge and applying the "truncated mean" method to resolve the distribution peak value to several percent.
Because the Super$B$ DCH design parameters and foreseen working conditions aim to an overall single cell resolution (σ_E) of about 35% and σ_E is mainly driven by the detector contribution, we can set a limit of 15% for the front-end electronics contribution (i.e. $\sigma_{EL} \sim 5\%$) then making it negligible ($\sqrt{\sigma_E^2 + \sigma_{EL}^2} \sim \sigma_E$).
Finally, if we assume that the charge collection due to a m.i.p. crossing orthogonally the cell is about 50 fC ($\sim 2fC/e$ @ 10^5 nominal gas gain) we can infer a limit of the Equivalent Noise Charge (ENC) for the single front-end channel of about 50 $fC \cdot 0.05 \simeq 2.5$ fC.

Dynamic range With 8 bits ADCs the dynamic is $2.5 - 500$ fC, actually even more then system requirements.

Linearity As stated above, the single cell energy resolution is about 35%, therfore a linearity of the order of 2% largely satisfies the system requirements.

13.1.2.3 Standard Readout - time measurements specifications

As for charge measurements we have three main specifications: resolution, dynamic range and linearity.

Resolution One of the Super$B$ DCH requirements is charged particle tracks reconstruction. The measure is carried out by acquiring the first ionized electron arrival time to the sense wire with a negligible error with respect to the quoted value of σ_S ($\sim 110\mu m$).
Limits to spatial resolution are due to primary ionization statistics, electrons diffusion and time measurement accuracy.
Assuming an intrinsic chamber resolution (σ_{SC}) of about 100 μm **(ref DCH)** the upper limit for electronic contribution can be quoted to be $\sigma_{EL} \leq \sqrt{\sigma_S^2 - \sigma_{SC}^2} \simeq 50$ μm. As helium based gas mixtures are characterized by a non saturated drift velocity up to high fields, [1] electrons drift velocity rapidly increase approaching sense wire, thus a 2.5 $cm/\mu s$ (25 $\mu m/ns$) [2] has been used to evaluate the maximum acceptable error in time measurement, that is $\sigma_t \leq 50[\mu m]/25[\mu m/ns] \simeq 2$ ns.
Discarding the bunch length contribution (tenths of ps) there are two main error sources in time measurements: the discriminator jitter (different signals cross a fixed threshold at different times) and the TDC resolution (digitization noise). Signal jitter, in turn, has two main contribution: signal noise and time-walk.
Signal noise contribution is generally small and can be evaluated according to $\Delta t = \sigma_{noise}/(dV/dt) \simeq \sigma_{noise} \cdot \tau/V_{max}$ where τ is the preamplifier-shaper peaking time.
Assuming that a single electron cluster generates a signal of ~ 20 mV, and that noise and peaking time associated to the signal are, respectively, $\sigma_{noise} \sim 3$ $mV(rms)$ and $\tau \sim 5$ ns we get a noise contribution to time resolution of about *0.8 ns*.
The time-walk effect is caused by signal amplitude variation. With a peaking time around 5 ns, a time-walk contribution for a low-threshold leading-edge discriminator of about $1.5ns$ can be estimated.
Finally, the digitization noise is a function of the digitization unit according to $\sigma = \Delta/\sqrt{(12)}$ where Δ is the quantization unit, using $\Delta \simeq 1.5$ ns a digitizing noise of about 0.45 ns is obtained.
Summarizing, without corrections, the time resolution is dominated by the signal time walk and can be estimated to be about 1.8 ns including all contributions. Nevertheless corrections can be applied using digitized signals to minimize time-slewing effects then reducing the time walk contribution (see Front End Boards - Digitization Section).

Dynamic Range The TDC range depends on the drift velocity and on the cell size. A maximum drift time of about 600 ns has been foreseen for Super$B$ DCH cells. Providing some safety factor, a TDC range of about 1 μs is adequate.

Linearity A linearity of the order of 1% fully satisfies time measurement requirements.

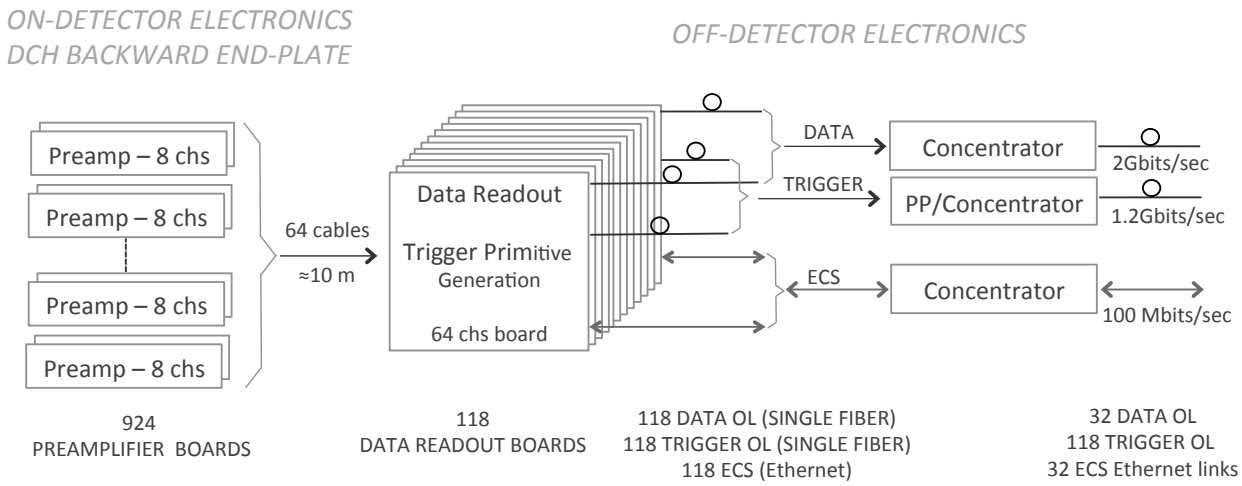

Figure 13.2: DCH front-end block diagram

13.1.2.4 Standard Readout - DCH Front-end system (block diagram)

The DCH FE chain (fig.13.2) is split in two blocks:

- ON-DETECTOR electronics: HV distribution and preamplifier boards located on the backward end-plate to preserve sense wire signal Signal to Noise Ratio (SNR).
- OFF-DETECTOR electronics: Data Readout and Concentrator Boards located on the top-side of the experiment. Trigger primitives are generated on these boards as well.

The connection between ON-DETECTOR and OFF-DETECTOR boards will be implemented by means of micro (mini) coaxial or twisted pairs cables while OFF-DETECTOR Boards output connections will depend on the data path. DAQ chain and Trigger chain data path will use optical links while ECS will use copper links **(see ECS section)**.
In the following paragraphs we will refer to the preamplifier boards as Very Front End Boards (VFEB) to distinguish them from Front End Boards (FEB) containing the digitization and buffer sections located far from the detector.

13.1.2.5 Standard Readout - ON-DETECTOR electronics

Very Front End Boards Very Front End Boards will contain HV blocking capacitors, protection networks, preamplifiers and (possibly) shapers-amplifiers. Because of the small cell dimensions more cells must be grouped in a single, eight-channel preamplifier-shaper board. Output and power supply cables will be connected to the boards by means of suitable connectors.
Besides the requirements on SNR, preamplifier should be characterized by enough bandwidth to preserve signal time information and low power requirement, not more than 20-30 mW per channel, to limit the total power dissipation on the backward end-plate to $160 \div 240\ W$ then allowing the use of simpler and safer forced air cooling system (no risk of leak).

Table 13.2: Preamplifier main specifications

Linearity	$< \%(1 - 100fC)$
Output Signal Umbalance	$< \%(1 - 100fC)$
Gain (Differential)	$\sim$ 5.2 mV/fC
Z_{IN}	110 Ω
Z_{OUT}	50 Ω
Rise time	$\sim$ 2 ns ($C_D = 24pF$)
Fall time	$\sim$ 13 ns ($C_D = 24pF$)
Noise	1350 erms ($C_D = 24pF$)
V_{SUPPLY}	4V
P_D	$\sim$ 30mW

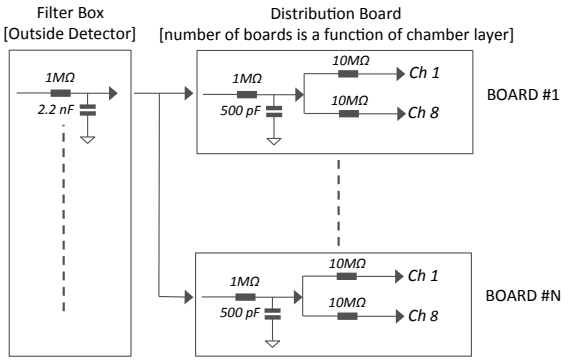

Figure 13.4: Standard Readout High Voltage distribution network

Concerning the circuit implementation, since the channel density is quite low and simple circuit topology can be used, an approach based on SMT technology can be adopted then avoiding dedicated (and expensive) development (ASIC). As an example, a simulation of a three stages

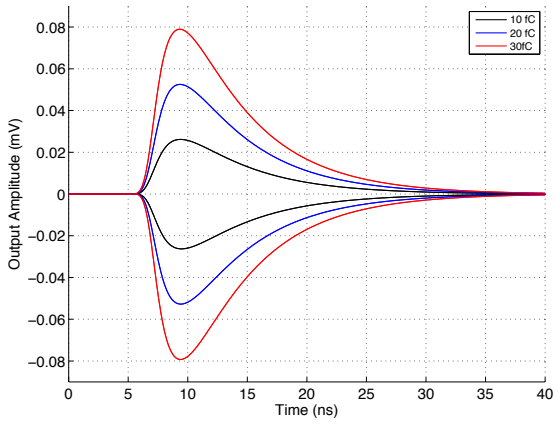

Figure 13.3: Preamplifier output for 10, 20 and 30 fC test pulse ($C_{DET} = 24pF$)

transimpedance preamplifier based on SiGe transistors has been carried out. The first stage dominant pole is around 26 MHz while other stages have been designed with wider bandwidth then obtaining a good separation in terms of cutoff frequencies.
Simulation results are shown in table 13.2 while fig. 13.3 shows the (simulated) output waveforms for 3 different input charges (10, 20 and 30 fC) injected through the test input.

HV distribution boards The high voltage distribution network (fig. 13.4) will be located on the forward end-plate. The distribution board modularity will match the preamplifier modularity while the number of distribution boards connected to a single HV channel will depend on the distance from the DCH inner radius (example: inner layers = 2 boards, outer layers = 5 boards).

13.1.2.6 Standard Readout - OFF DETECTOR electronics

Front End Boards - Block Diagram Front End Boards will host up to 64 channels and will be made of three stages as shown in fig.13.5. The first one receives signals from preamplifiers and generates outputs for digitizing and trigger primitives sections while the second stage provides digitization for charge and time measurements. Digitization stage includes the logic for trigger primitives generation as well. Finally, the third stage contains the Latency and Readout buffers and the dedicated control logic. Boards include an ECS section as well (not shown in the block diagram) for parameters setting/sensing and system test.

Front-End-Boards - Receiver Section Details of the receiving section are shown in fig. 13.6. The preamplifier output signal is amplified and split to feed an anti-aliasing 14 MHz low-pass filter (charge measurements) and a leading edge discriminator (time measurements). Fig. 13.7 shows the simulated analog chain response to a Garfield simulated signal. In the simulations Spice models have been used for both active components and the 10 m twisted pairs cable.

Front-End-Boards - Digitization Section The 14 MHz filter output signal is routed to an eight bits and (about) 28 MSPS FADC whose outputs feed a section of the system Latency Buffer implemented in a FPGA. Thirty-two FADC output samples (corresponding to about 1.14 μs,

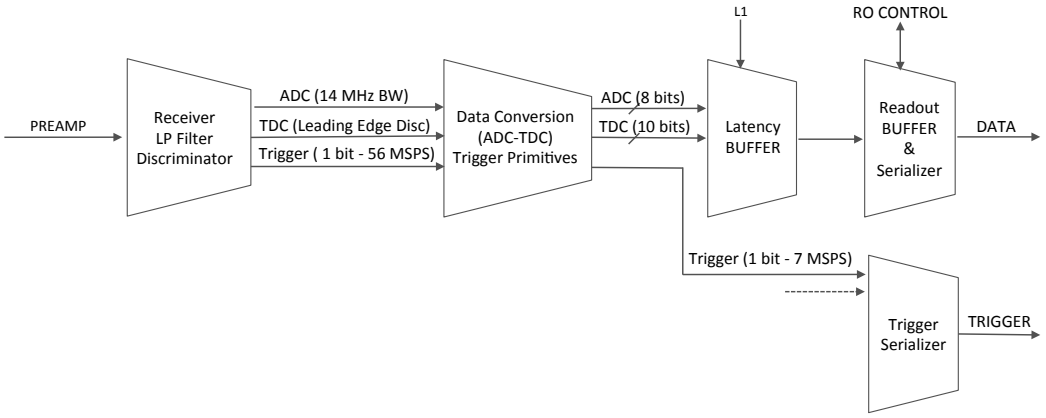

Figure 13.5: Front End Board Block Diagram

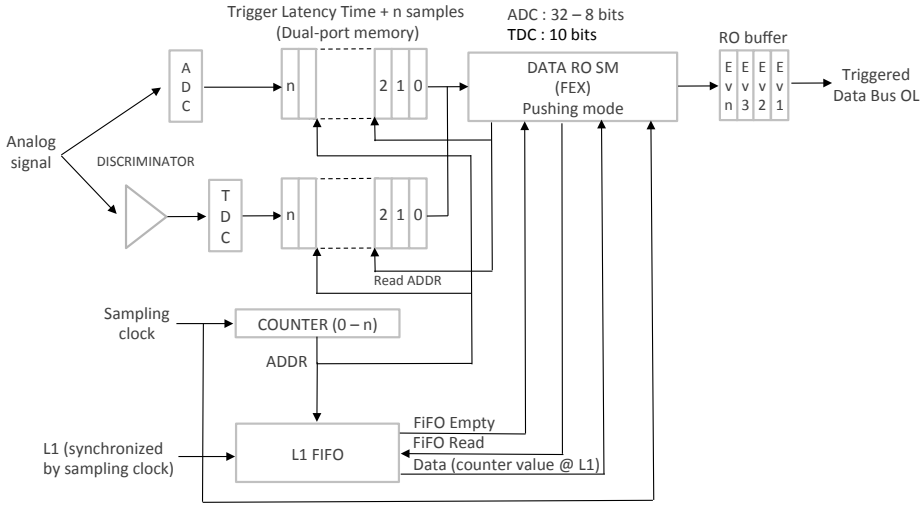

Figure 13.8: Digitization chain block diagram

enough to span the full signal development) will be Read-Out in presence of a Level 1 (L1) trigger and, eventually, stored in a Read-Out Buffer. The comparator output is also routed to the FPGA, where it is spit in two paths. The first one is sent to a TDC (implemented in the FPGA itself using the oversampling method) for arrival time measurement. The TDC outputs feed the second section of the Latency Buffer that, again, will be Read-Out in presence of a L1 trigger signal (fig 13.8). The second one, synchronized with the system clock and conveniently stretched to remove redundant informations is sent to the DCH Trigger Segment Finding modules **(see Trigger Section)**.

The data structure will not have a fixed length as L1 triggers spaced less than single event Read-Out time will extend the time window to include the new event. Nevertheless, the board structure will be also compatible with local Feature EXtraction (FEX) implementation, i.e. the extraction of relevant information from the digitized data. In case of FEX implementation the transferred data stream would have a fixed length; the structure could be similar to that shown in table 13.3.

Table 13.3: FEX based data stream (fixed length structure)

Data stream example
Digitizer Module Address (2 bytes)
Flag (1 byte)
Trigger Tag (1 byte)
Counter (1 byte)
Charge (2 bytes)
Time (2 Bytes)
1st ADC sample (different from baseline) for time walk correction (1 byte)

13.1.2.7 Sampled Waveforms - specifications

The Cluster Counting technique is very powerful as it improves DCH particle identification. The technique is based on primary ionization measurement and, to fully exploit the technique, individual clusters must be identified.
On the other hand the front-end requirements are quite onerous as, despite the use of slow drift velocity ($\sim$1 $\mu s/cm$), high sampling frequency digitizers (at least 1 GSPS) and fast processing (data throughput must sustain the Super$B$ expected 150 kHz average trigger rate) are required. These requirements, at the state of art of technology, result in a huge power requirement and, as a consequence in a low FEB modularity.
As also on the VFEB side fast amplifiers must be used, then power requirements will be higher than in the "Standard Readout" scenario thus envisaging the use of a local liquid cooling system. Moreover the wide bandwidth requirement has also an impact on the type of cable used to interconnect on-detector and off-detector electronics and on the full system noise pick-up sensitivity.
Finally, to apply the cluster counting technique correctly, signal reflection on the sense wires must be avoided by means of termination resistors, and this, unavoidably, sets a lower limit on the system intrinsic noise.
Concerning tracking requirements, if we assume that full efficiency in single electron cluster detection is achieved, Cluster Counting dE/dx measurement already includes information for tracking purpose (it is just required to store clusters arrival time instead of simply counting them).
Specifications for the Sampled Waveforms measurement are the same we defined for the Standard Readout that is: resolution, dynamic range and linearity.

Resolution Digitizers resolution is a function of both the lowest signal amplitude to be digitized and the system noise. Assuming an average delivered signal of $\sim 6fC/e$ @ $3 \cdot 10^5$ gas gain, a preamplifier-shaper gain of $10mV/fC$ and a safety factor of 2 for gas gain fluctuations we get an (average) minimum signal of about 30 mV (single electron cluster).
Preamplifier ENC estimation at the moment it is difficult, nevertheless we can do an estimation of the dominating noise source, that is the termination resistor. Assuming a CR-RC shaping circuit and a 3 ns peaking time we get about $\sim$ 0.2 fC, that is about 2 mV rms for a preamplifier gain of 10 mV/fC.
Thus a LSB of about 2 mV allows good control of system noise and cluster signal reconstruction.

Dynamic range Cluster Counting method requires to find the peaks (corresponding to the clusters) contained in the digitized signals. The expected dynamic range (discarding gas fluctuation) is driven by the cluster size (i.e. the number of primary ionization electrons contained in a single cluster). Signal dynamic range can be,

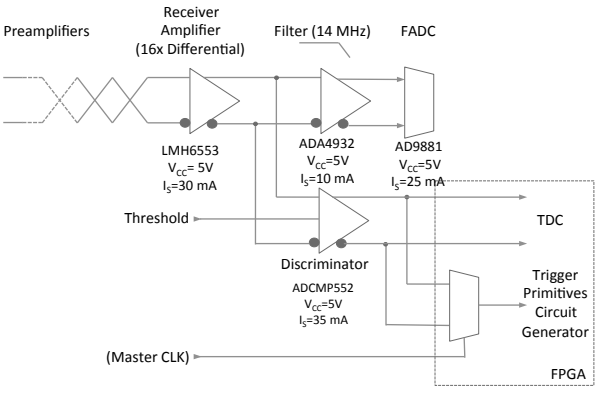

Figure 13.6: Readout board: Analog Section block diagram (40mA@5V/35 mA@3.3 V)

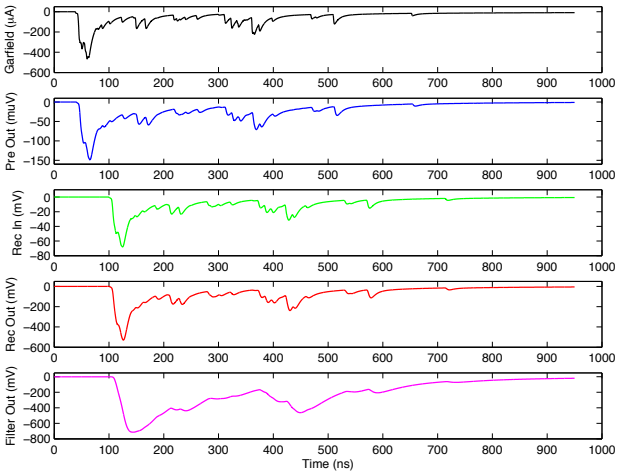

Figure 13.7: Readout board: Analog Chain Response - Garfield output (black), Preamplifier output (blue), Receiver input (green), comparator input (red), FADC input (Cyan)

then, defined (as an upper limit) by the expected total ionization.
Helium based gas mixture have already been well characterized [3]; assuming a 1.2 *cm* square cell and a 90/10 He/Iso gas mixture we expect about 26 electrons for a m.i.p crossing the cell orthogonally, thus an 8 bits ADC dynamic range is fully adequate for CC measurement.

Linearity As we are interested on finding (and tagging) signal peaks, a resolution of 2% fully satisfies the requirements.

13.1.2.8 Sampled Waveforms - DCH front-end system (block diagram)

The Sampled Waveforms DCH front-end chain block diagram is similar to the diagram shown in fig.13.5; also in this scenario we will have ON-DETECTOR and OFF-DETECTOR electronics connected by means of mini coaxial cables, but, because of the lower board modularity both the number of crates and boards will increases significantly (see table 13.4).

13.1.2.9 Sampled Waveforms - ON DETECTOR electronics

Very Front End Boards Because Very Front End Boards will host high bandwidth (500 MHz) preamplifiers both layout and assembly are more tricky with respect to the Standard Readout scenario. In particular special attention must be devoted to ground loops in such a way to minimize both instabilities and external noise pickup.

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Something about preamplifier .....
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HV distribution boards Most of the remarks shown before also apply for Sampled Waveforms scenario. Anyway, because of the sense wire termination resistor the boards layout will be slightly different and, moreover, high quality grounding is required. The HV distribution network is shown in fig 13.9.

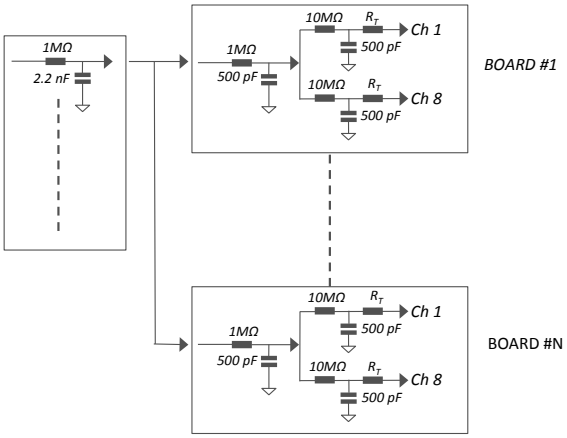

Figure 13.9: Sampled Waveforms High Voltage distribution network

13.1.2.10 Sampled Waveforms - OFF DETECTOR electronics

Front End Boards Front End Boards will be based on high sampling rate ($\geq$ 1 GSPS) digitizer, then a limited number of channels can be packaged on a single board, mainly because of power requirements. At present, up to 8 channels working at 1 GSPS have been packaged in a single VME 6U board. Nevertheless, in the

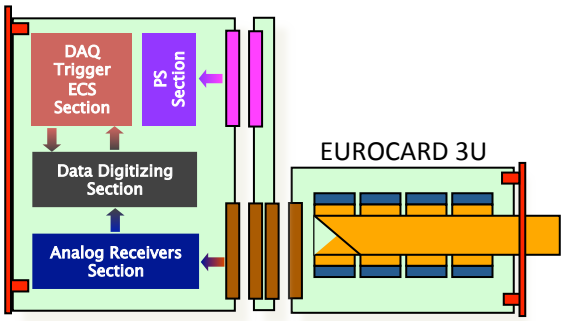

Figure 13.10: VFEB - FEB connections (FEB board - Custom Backplane - Interconnection Board

next future, board modularity could increase to 16 (or 24) still maintaining the current 8 channels board power requirements.
The circuit structure is very close to the block diagram shown in 13.5. Differences arise in digitizing section as no TDC is required for time measurements and also Trigger signals are generated starting from the FADC outputs.
A sensitive issue concerns the FEX. Because of the large amount of data per channel (about 1 thousand of bytes) we can not transfer raw data to the DAQ thus FEX must be implemented in the FEB itself. That is, when an L1 accept is raised all the event samples must be scanned to identify clusters. The time required to implement the procedure is still compatible with the average trigger rate foreseen at the nominal luminosity ($\sim 150\ kHz$), but it could be a limit if the luminosity increases.
Another issue concerns the radiation background, as high performances RAM based FPGA must be used in the design.

13.1.2.11 Front End Crates

Each Front End Crate will host up to 16 FEB, a Power Supply board for VFEB, Data Concentrators and, eventually, Trigger Patch Panel o Trigger Concentrator. Custom backplanes will be designed to distribute power and common signals to FEBs, to allow the use of Interconnection Boards to collect low modularity VFEB cables (fig 13.10) and to route some of the trigger signals to the neighbors boards **(see Trigger Section)**.

13.1.2.12 Number of crates and links

Table 13.4 shows the estimate of the number of links, boards and crates required for both DAQ and Trigger front-end chains (each crate is supposed to host up to 16 FEB). As shown in the table the number of Trigger OL do not change despite the different FEB number the two scenarios. This is because the Sampled Waveform scenario foresees a Concentrator board also for the trigger chain because of the lower modularity. The board will collect Trigger OL coming from several FEBs and will deliver a single OL to the TFS modules.
The estimate has been based on the following assumptions: 150 kHz L1 trigger rate, 7392 sense wires (subdivided in 10 super-layers), 10% chamber occupancy in 1 μs time window and 48 bytes per channel data transfer. Single link bandwidth is 2 Gbits/sec for DAQ data path and 1.2 Gbits/sec for Trigger data path.

Table 13.4: Number of links (Data, ECS, Trig), FEBs and crates for 64 (Standard Readout) and 16 (Sampled Waveforms) channels board modularity

	Mod	Data	ECS	Trig	Boards	Crates
SR	64	32	32	118	118	8
SW	16	32	32	118	462	29

13.1.2.13 ECS

Each FEB will host a mezzanine board to manage ECS communication. Besides the control of the board, ECS mezzanine should provide the capability of data buffer readout for debugging propose. Detail can be found in the ECS section.

13.1.2.14 Cabling

Because the large number of channels involved, DCH cable layout must be carefully designed. The main requirement concerns the possibility of changing, in case of failure, a VFEB without disconnecting output cables from too many boards. Thus, signal and HV cables should leave

the chamber from the outermost layer then minimizing cables overlap. Table 13.5 shows the foreseen number of cables and a rough estimation of cable size. Signal twisted pairs cables are commercially available also with flat shielded assembly (size 16x3 mm^2 for 8 pairs).

Table 13.5: Estimation of the number and dimension of DCH cables (7392 sense wires - VFEB modularity = 8 channels)

	LVPS	HV	Signal (coax)	Signal (twisted)
Quantity	118	32	7392	924
N of cores	16	25	1	16
Cond. area (mm^2)	0.5	0.07		
Overall diam. (mm)	12	12	1.8	6.5

13.1.2.15 Power Requirements

A very preliminary power requirement estimation is shown in table 13.6. The estimation for ON-DETECTOR electronics is based on preamplifier simulation and prototype test, while estimation for OFF-DETECTOR electronics come from the state of art of digitizing board available at the moment. Local (VFEB) voltage regulation is supposed to be implemented by means of linear low-voltage drop hard-rad regulator.

Table 13.6: Power requirement estimation for bot Standard Readout (SR) and Sampled Waveform (SW)

	Channel	Board	Overall
SR VFEB	30 mW		250 W
SW VFEB	150 mW		1.2 kW
SR FEB		40 W	5 kW
SW FEB		40 W	19 kW
SR & CC Data Conc.		30 W	240 W
SW Trig Conc.		30 W	870 W

13.1.2.16 Grounding

As a general rule grounding is supposed to be included in a system/equipment only for safety purpose. Thus, detector equipment should be designed in such a way it should work also without GND connection (GND is not a current return path).
LV power supply should have isolation transformer (AC input/output terminal should be electrically isolated for low frequencies). If the output terminal of HV power supply is not floating a resistor should be connected between GND and the common of HV distribution system to avoid ground loops.

13.1.3 PID Electronics

The electronics for the FDIRC can be seen as an upgrade of the electronics of the *BABAR* DIRC. The new requirements of the experiment (Trigger rate, background, radiation environment) and FDIRC specific requirements (resolution, number of channels and topology) have led to a similar but new design of the electronics chain.

The electronics will equip the 18,432 channels of the 12 sectors of the FDIRC. The electronics chain is based on a high resolution / high count rate TDC, a time associated charge measurement on 12 bits and an event data packing sending event data frames to the data acquisition system (DAQ). The target performance of the overall electronics chain is a time resolution of 100 ps rms. This chain has to deal with a count rate per channel of 100 kHz, a trigger rate up to 150 KHz and a minimum spacing between triggers of about 50 ns.

The estimate radiation level is expected to be less than 100 rads per year. The use of radiation tolerant components or off the shelves radiation-qualified components is mandatory. However, the expected energy of the particles may make the latch-up effect almost impossible. Thus, the design has to take into account only Single Event Upsets. We selected the Actel family FPGA components for their non-volatile flash technology configuration memories, which are well adapted to radiation environment.

Several architectures have been considered which can be summarized as follows:

- All electronics directly mounted on the FBLOCK.
- All electronics mounted next to the detector and linked to the PMTs by cables.
- A part of it on the detector (the Front-end boards) and the other part, called crate concentrator, situated close to the detector, (this board is in charge of interfacing

with the Front-end, reading out event data, packing and sending it to the DAQ.

The first solution has been chosen as baseline for the TDR for two main reasons:

- The cost of the cables (PM to Front-end boards) is estimated to be close to 200 kEuros (1/3 of the price of the overall electronics cost), making this solution too expensive. Moreover, the possible option to have pre-amps on the PMT bases doesn't prevent from having electronics and power supplies on the detector.
- The large amount of data per channel leads to have the L0 derandomizer and buffer on the Front-end boards. The FCTS receiver could be individually located on each Front-end board but the number of cables needed pushes to distribute all the control signals on a backplane. Consequently the board dedicated to receiving and transmitting FCTS signals on the backplane naturally tends to also become the event data concentrator and the link to the DAQ.

The baseline design assumes a 16-channel TDC ASIC offering the required precision of 70 ps rms- embedding an analog pipeline in order to provide an amplitude measurement transmitted with the hit time. Thanks to a 12-bit ADC, the charge measurement will be used for electronics calibration, monitoring and survey purposes. The Front end board FPGA synchronizes the process, associates the time and charge information and finally packs them into a data frame which is sent via the backplane to the FBLOCK control board (FBC). The FBC is in charge of distributing signals coming from the FCTS and ECS, packing the data received from the FE boards to a n-event frame including control bits and transferring it to the DAQ.

13.1.3.1 The TDC chip

A former TDC chip offering the requested performances of resolution has already been designed for the SuperNemo experiment. It provides a time measurement with both a high resolution 200 ps step (70 ps RMS) and a large dynamic range (53 bits). The architecture of this chip is based on the association of Delay Locked Loops (DLLs) with a digital counter, all of these components being synchronized to a 160 MHz external clock.

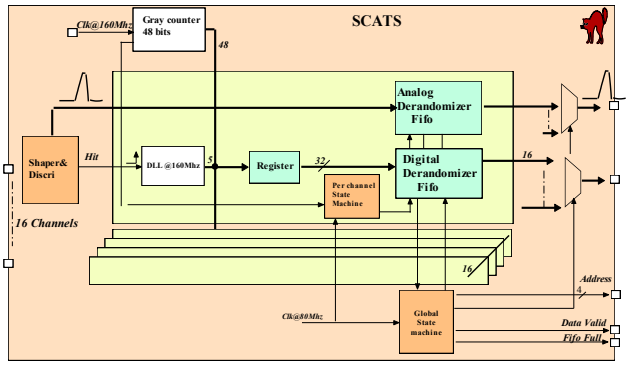

Figure 13.11: Block diagram of the Super*B* FDIRC TDC chip — SCATS —

The Super*B* chip (SCATS, Fig. 13.11) will keep the same philosophy but the high input rate requirement lead to a complete re-design of the readout part, in order to minimize the dead time per channel. Instead of registers and multiplexer which are the bottlenecks of the SuperNemo chip readout, it makes use of an individual FIFO memory per channel in order to derandomize the high frequency bursts of input data

With this architecture, data from the DLLs and the coarse counters are transferred into the FIFO memory within two clock cycles. When the transfer is complete, the channel is automatically reset and ready for the next hit. Simulations of the readout state machine showed an output FIFO data rate capability of 80 MHz. Time ranges for the DLLs and the coarse counter can be easily customized by adjusting the output data format (16, 32, 48 or 64 bits). Therefore, the chip is suitable for various applications with either high count rate and short integration time or low count rate and long integration time.

A FIFO depth of 8 words has been selected after simulation with a exponential distribution

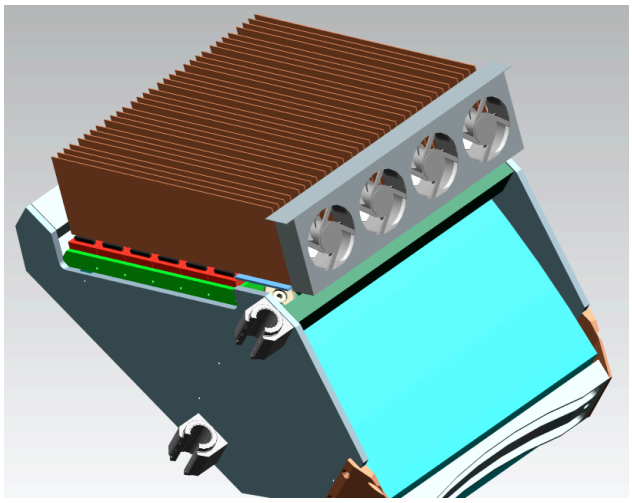

Figure 13.13: The FBLOCK equipped with the boards and fan tray

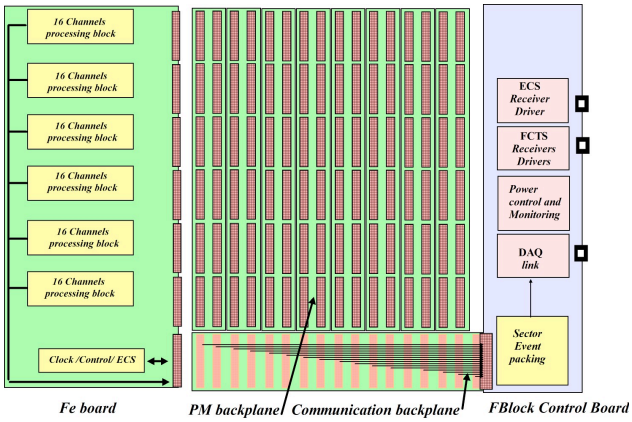

Figure 13.14: The Frontend Crate

model of delta time between hits (mean rate of about 1MHz) applied to inputs. Thus the simulation gives a dead time of approximately 1% with 500 kHz input rate on each channel.

To design this FIFO a full custom RAM has been developed. It permits reducing the size of the chip and consequently its cost. The chip is designed using known and proved mitigation techniques to face single event upset (SEU) issues due to the low-level radiation environment.A first version of the chip without the analog FIFO and the discriminator has been submitted in November 2011 and the test are ... Note: something is missing here.

We plan to submit in 2012 one chip PIF dedicated to the currently missing parts:

- A low walk (approx. 50 ps) discriminator based on a CFD like design.
- A track/peak detector to be able to sample the maximum of the signal.
- An analog pipeline synchronized with the digital FIFO and providing analog output for charge measurement.

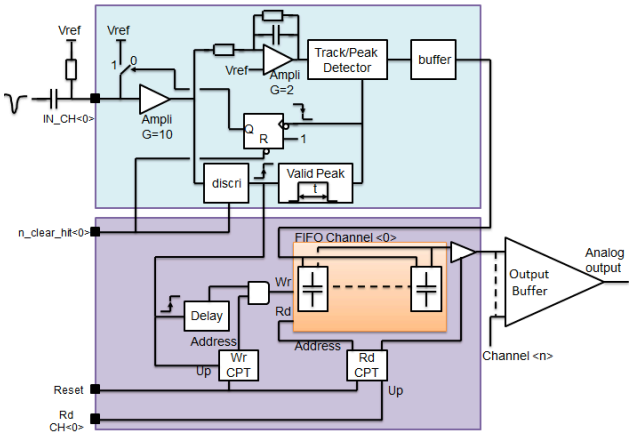

Figure 13.12: PIF One Channel

After testing and validation, it is foreseen to be included in the final version of SCATS taking benefit of sharing the FIFO pointers of the analog and digital parts. The chip will be assembled and submitted end of 2013.

13.1.3.2 The Front-end Crate

The board input will fit the topological distribution of the PM on the FBLOCK. The PMs are arranged as a matrix of 6 in vertical direction by 8 in horizontal direction. Each column of 6 PMs will fit to one FE board. One vertical backplane (PM Backplane) will interface between the 4 connectors of each PM base to one connector of FE board. The PM Backplane is also in charge of distributing the High Voltage, thus avoiding HV cables to pass over the electronics. The FB crate will use as much as possible the elements of a commercial crate, in order to avoid the design of too many specific elements like board guides.

13.1.3.3 The Communication Backplane

Distributes the ECS and FCTS signals from the FBC to the 8 FE boards thanks to point to point LVDS links. Connects each FE board to the FBC for data transfer. A serial protocol will be used between FE board and the FBC in order to reduce the number of wires and consequently ameliorate the reliability. It will also distribute JTAG signal for FPGA board reprogramming and all signals for monitoring and control of the crate.

13.1.3.4 The PMT Backplane

It is an assembly of 8 motherboards, each one corresponding to a column of 6 PMTs. One motherboard receives 2 Fe-board. The 64 channels from 4 connectors per each PMT are merged on the motherboard into two connectors to get into the Front end board to get 16 channels per half PMT, i.e., 6 PMTs correspond to 96 channels per FE-board. It also insures the ground continuity between FE-boards — crate — FBLOCK.

13.1.3.5 Cooling and power supply

The electronics is located on the detector in a place enclosed by the doors. There are 2 major consequences: one is the problem of the cooling which must be carefully studied in terms of reliability and capability and the second is that the location is naturally shielded. Consequently the use of magnetic sensitive components as coils or fan trays is possible.

An estimation of the overall electronics consumption lead to approximately 6 kW, not including the external power supplies. This can be broken down to individual contribution as follows:

- Electronics: 0.325W/channel, 500 W/sector and 6 kW/system.
- HV resistor chain: 0.19W/tube, 9.1W/sector, and 109 W/system.

The cooling system must be designed in order to maintain the electronics located inside at a constant temperature close to the optimum of 30 degrees. The air inside the volume must be extracted while the dry, clean temperature controlled air will be flowing inside. Each FB crate will have its own fan tray like in a commercial crate. Targeting a difference of 10 degrees between inside and outside temperature drives to a rough estimate value of $300m^3/h$ per crate, $4000m^3/h$ can be considered as the baseline value for the whole detector.

13.1.3.6 The front-end board

One Front-end board is constituted of 6 channel-processing blocks handling the 96 channels. The channel-processing block is constituted by one SCATS chip, one ADC, one Actel FPGA and the associated glue logics.

The FPGA receives event data from the TDC and the converted associated charge from the ADC. From one 16 bit bus of the 16 channels coming from the TDC, it de-serializes to 16 data path where events are keeping in a buffer until they are thrown away if there are too old (relatively to the trigger) or sent upon its reception.

The PGA master receives event data from the 6 channel processing blocks and packs the event.The FE board transfers the event frame in differential LVDS to the FBC via the communication backplane.

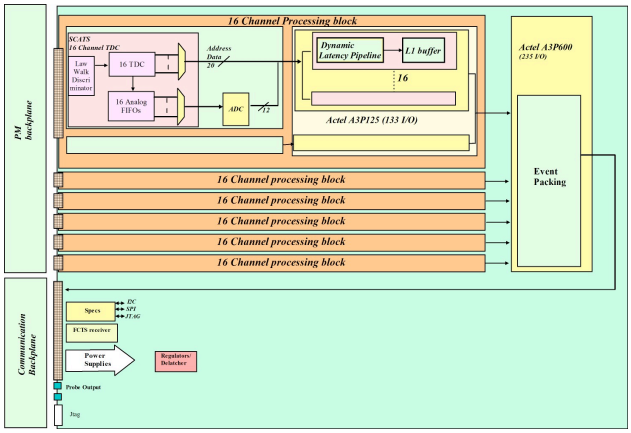

Figure 13.15: PID Front-end Board

13.1.3.7 The crate controller board (FBC)

The FBC is the board which gathers the front-end data, control and monitors the crate. There is one board per crate. The board handles several functionalities:

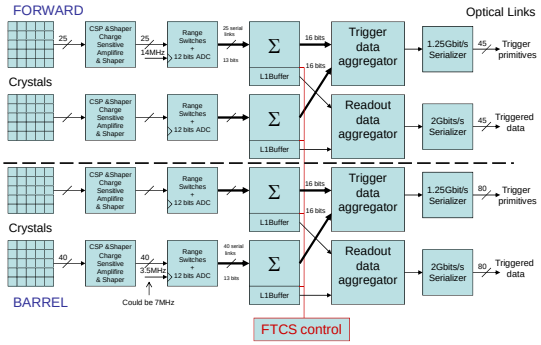

Figure 13.16: EMC Electronics

- Receive the event data from the Front-end boards via the communication backplane, constitutes and event data fram for the DAQ
- Spy data building for monitoring and commissioning purposes
- Distributes the ECS (SPECS) signals to the front end. Distributes the JTAG.
- Deserialize clock and control signals from FCTS.
- Monitor the crate; temperature, power supplies, fans.

13.1.4 EMC Electronics

This is still the version from the Whitepaper!!!

Two options have been considered for the EMC system design—a *BABAR*-like push architecture where all calorimeter data are sent over synchronous optical 1 Gbit/s links to L1 latency buffers residing in the trigger system, or a "triggered" pull architecture where the trigger system receives only sums of crystals (via synchronous 1 Gbit/s links), and only events accepted by the trigger are sent to the ROMs through standard 2 Gbit/s optical links.

The triggered option, shown in Fig. 13.16, requires a much smaller number of links and has been chosen as the baseline implementation. The reasons for this choice and the implications are discussed in more detail below.

To support the activated liquid-source calibration, where no central trigger can be provided, both the barrel and the end-cap readout systems need to support a free running "self-triggered" mode where only samples with an actual pulse are sent to the ROM. Pulse detection may require digital signal processing to suppress noisy channels.

Forward Calorimeter The 4500 crystals are read out with PIN or APD photodiodes. A charge preamplifier translates the charge into voltage and the shaper uses a 100 ns shaping time to provide a pulse with a FWHM of 240 ns.

The shaped signal is amplified with two gains ($\times 1$ and $\times 64$). At the end of the analog chain, an auto-range circuit decides which gain will be digitized by a 12 bit pipeline ADC running at 14 MHz. The 12 bits of the ADC plus one bit for the range thus cover the full scale from 10 MeV to 10 GeV with a resolution better than 1%. A gain is set during calibration using a programmable gain amplifier in order to optimize the scale used during calibration with a neutron-activated liquid-source system providing gamma photons around 6 MeV.

Following the *BABAR* detector design, a push architecture with a full granularity readout scheme was first explored. In this approach, the information from 4 channels is grouped, using copper serial links, reaching an aggregate rate of 0.832 Gbit/s per link to use up most of the synchronous optical link's 1 Gbit/s bandwidth. A total of 1125 links are required. The main advantage of this architecture is the flexibility of the trigger algorithm that can be implemented off-detector using state of the art FPGAs without constraining their radiation resistance. The main drawback is the large cost due to the huge number of links.

The number of links can be reduced by summing channels together on the detector side, and only sending the sums to the trigger. The natural granularity of the forward detector is a module which is composed of 25 crystals. In this case, data coming from 25 crystals is summed together, forming a word of 16 bits. Then the sums coming from 4 modules are aggregated together to produce a payload of 0.896 Gbit/s. In

this case, the number of synchronous links toward the trigger is only 45. The same number of links would be sufficient to send the full detector data with a 500 ns trigger window. This architecture limits the trigger granularity, and implies more complex electronics on the detector side, but reduces the number of links by a large factor (from 1125 down to 90). However, it cannot be excluded that a faster chipset will appear on the market which could significantly reduce this implied benefit.

Barrel Calorimeter The EMC barrel reuses the 5760 crystals and PIN diodes from *BABAR*, with, however, the shaping time reduced from 1 μs to 500 ns and the sampling rate doubled from 3.5 MHz to 7MHz. The same considerations about serial links discussed above for the forward EMC apply to the barrel EMC. If full granularity data were pushed synchronously to the trigger, about 520 optical links would be necessary.

The number of synchronous trigger links can be drastically reduced by performing sums of 4×3 cells on the detector side, so that 6 such energy sums could be continuously transmitted through a single optical serial link. This permits a reduction in the number of trigger links so as to match the topology of the calorimeter electronics boxes, which are split into 40 ϕ sectors on both sides of the detector. Therefore, the total number of links would be 80 both for the trigger and the data readout toward the ROMs, including a substantial safety margin (> 1.5).

13.1.5 IFR Electronics

draft 0.3, May 16 2012, A. Cotta Ramusino

13.1.5.1 Introduction

This section describes first the features of the IFR detector which drive the design of the readout system. It presents then an estimation of the number of electronic channels, of the event size and the data bandwidth at the nominal Super*B* trigger rate. The design constraints determined by the expected background radiation are then reviewed, along with the results of irradiation tests on existing ASICs and off-the-shelf devices suited for the implementation of some functional blocks of the readout chain. This chapter describes, finally, the baseline IFR readout system going from the basic requirements of a dedicated IFR readout ASIC to the proposed locations of the IFR electronics system to the services required in the detector hall.

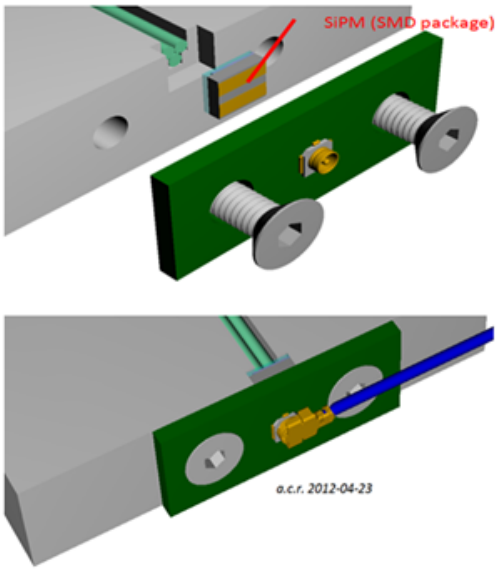

Figure 13.17: details of the three WLS fibers and the PCB for the SiPM

13.1.5.2 Basic features of the IFR detector

The basic IFR detector element exploits an extruded plastic scintillator with WLS fibers applied in machined grooves and "Silicon Photomultipliers" (SiPM) installed as shown in Fig. 13.17. The scintillator bars, fitted with the SiPM carrier PCBs and the signal cables, will be enclosed in boxes made of sheet aluminum which will shield the assembly from the ambient light and will provide it with the necessary mechanical rigidity; the detector assemblies are, in the following, referred to as "modules". The modules will be inserted in the gap between the two steel plates delimiting an "active" layer; nine active layers will be instrumented in the barrel section of the IFR and also nine layer will be "active" in the endcaps. Fig. 13.18 shows a few modules, installed in the barrel section of the IFR, with the aluminum "envelope" removed to show the scintillator orientation. The

LAYER WIDTH	LAYER	No. Modules per layer	LAYER ENABLE	PHI ASSUMING 50MM BARS	ZETA ASSUMING 106MM BARS
1963	1	6	1	13	17
1987	2	6	1	13	17
2050	3	6	1	13	17
2113	4	6		14	17
2176	5	6		14	17
2240	6	6		14	17
2304	7	6	1	15	17
2367	8	6		15	17
2431	9	8		12	17
2494	10	8		12	17
2569	11	8	1	12	17
2641	12	8		13	17
2712	13	8		13	17
2784	14	8	1	13	17
2879	15	8		14	17
2973	16	8	1	14	17
3068	17	8		15	17
3144	18	8	1	15	15
3296	19	8	1	16	15
NUMBER OF MODULES per sextant:		64		TOTAL PER SEXTANT	1940
TOTAL NUMBER OF MODULES	384			TOTAL CHANNELS PER BARREL	11640

Figure 13.19: estimation of the electronics channel count for the IFR barrel

ENDCAP		
top section	horizontal bars per module:	37
	vertical bars per module:	51
center section	horizontal bars per module:	36
	vertical bars per module:	64
bottom section	horizontal bars per module:	37
	vertical bars per module:	51
AVERAGE channel count per module:		92
NO_OF_MOD_PER_LAYER_EC:		3
horizontal bars per layer		110
vertical bars per layer		166
NUMBER OF LAYER PER DOOR		9
NUMBER OF DOORS IN ENDCAPS		4
TOTAL NUMBER OF MODULES IN ENDCAPS:		108
horizontal bars per door:		990
vertical bars per door:		1494
TOTAL HORIZONTAL BARS:		3960
TOTAL VERTICAL BARS:		5976
TOTAL CHANNELS IN ENDCAPS:		9936

Figure 13.20: estimation of the electronics channel count for the IFR endcaps

choice of tightly coupling the SiPM to the WLS fibers is driven by the need of maximizing the number of converted photoelectrons; this choice determines in turn that the coupling between the SiPMs and the first stage of the signal processing chain must be done through coaxial cables and connectors.

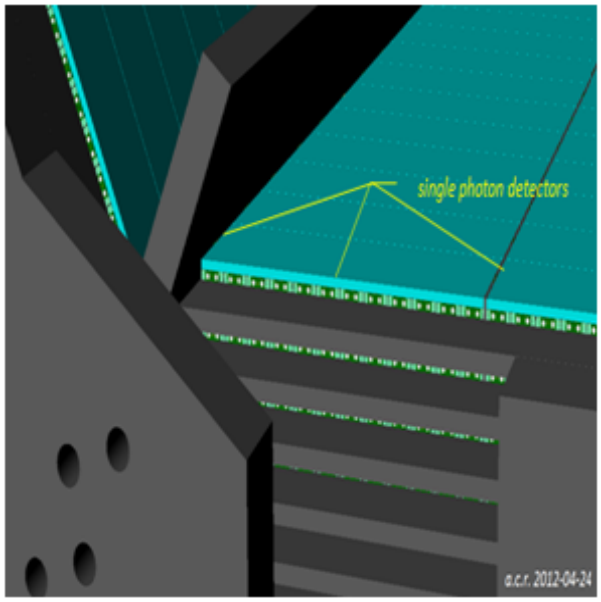

Figure 13.18: detector modules (with the metal enclosure removed) of IFR barrel, layer 0

13.1.5.3 IFR channel count estimation

The active layers of the IFR detectors are equipped with modules in which the detector bars (of different widths for the PHY and the Z views in the barrel) are assembled in two orthogonal layers.

Not all gaps of the flux return steel are equipped with detectors; the "LAYER ENABLE" column in Fig. 13.19 shows the current active layer assignment and the resulting total channel count of 11604 for the IFR barrel.

Fig. 13.20 recalls the distribution of the scintillator bars in an active layer of one endcap door. The total channel count for both forward and backward endcaps amounts to 9540 for 9 equipped gaps.

13.1.5.4 Estimations of the IFR event size and data bandwidth

The IFR detector will be read out in what has been dubbed "binary mode": the output of each SiPM device will be amplified, shaped and compared against a threshold; digitizer modules will sample and buffer the comparators outputs at a rate multiple of the Super$B$ clock and then extract from the latency memories the data selected by the FCTS trigger command. The IFR channels will be processed by functional blocks with a modularity of 32

BARREL		ENDCAP	
Max. channel count per module:	32	Avg. channel count per module	92
Number of MOD32 processing units per module	1	Number of MOD32 processing units per module	3
TOTAL NO. OF MODULES IN THE BARREL SECTION	384	TOTAL NO. OF MODULES IN THE ENDCAPS	108
Total Number of modulo 32 processing units	384	Total Number of modulo 32 processing units	324
Sampling period = 1 / FCTS_clock (ns)	17,86	Sampling period = 1 / FCTS_clock (ns)	17,86
Number of samples in the trigger matching window	10	Number of samples in the trigger matching window	10
BARREL EVENT SIZE (kB)	**15,36**	**ENDCAP EVENT SIZE (kB)**	**12,96**
TRIGGER RATE (kHz)	**150**	**TRIGGER RATE (kHz)**	**150**
TOTAL BANDWIDTH (Gbps) (including 8b/10b overhead)	**23,04**	**TOTAL BANDWIDTH (Gbps)** (including 8b/10b overhead)	**19,44**
Number of data links	24	Number of data links	16
Bandwidth per link (Gbps)	0,96	Bandwidth per link (Gbps)	1,215

Figure 13.22: estimations of the IFR event size and data bandwidth

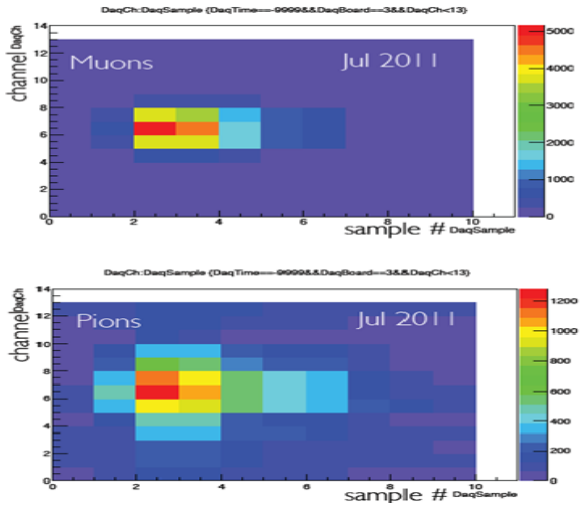

Figure 13.21: time evolution of muon and pions evaluated across the 10 samples taken for each "binary mode" event (plots from [4]). Sampling period was 12.5 ns)

Such a straightforward scheme has been successfully applied to the IFR prototype, which has been tested with cosmic muons and with the beam provided by the Muon Testing Facility of the Fermi National Accelerator Laboratory [4], [5]: the beam tests have shown that the time window for the extraction of data matched to a trigger should be about 120 ns wide (see Fig. 13.21), in order to recover the entire signal from the shower initiated in the detector by an impinging hadron.

The real IFR detector will be read out in the "binary mode" outlined above and the table in Fig. 13.22 reports the expected IFR event size and data bandwidth at the nominal Super$B$ trigger rate.

13.1.5.5 Background radiation and electronics design constraints

The current knowledge on the radiation environment at and around the flux return steel is presented in [6]. This work analyzes the known sources of radiation background in Super$B$ and evaluates the doses in Si at the locations of the SiPMs and at the locations of the front end electronics. The highest fraction of the total dose absorbed by the IFR electronics is deposited by neutrons deriving from the radiative BhaBha and the Touschek processes. The neutron energy spectrum shown in Fig. 13.23 above is quite wide-spread and so different types of interaction processes will have to be considered to assess the effect on the performances of the sensors and of the IFR readout chain. The highest neutron rate, about 5 kHz/ cm^2, is found, according to the plot in the lower left corner, at small radius at the forward endcap; the resulting neutron fluence over 10 years (considering the standard year of 10^7s) would be of about $5*10^{11}$ n/ cm^2.

Fig. 13.24 gives information on the dose (in Si) absorbed at the different locations in evidence. The highest dose is found at the C2 locations of the forward endcap and it is about 140krad/year. Electronics devices and systems which must reliably and durably operate under these radiation conditions must be designed or selected according to guidelines which have already been drawn, among others, by the LHC community; Electronics devices and systems which must reliably and durably operate under these radiation conditions must be designed or selected according to guidelines which have already been drawn, among others, by the LHC community. As an example one could refer to the "ATLAS Policy on Radiation Tolerant Electronics: ATLAS Radiation Tolerance Criteria"

[9] to see that the neutron fluence expected for the Super*B* IFR is of the same order of magnitude simulated for the MDT muon spectrometer. We could then, if not exploiting exactly the same technical solutions adopted there, at least follow the design guidelines established by the cited and by similar documents. A more general approach to the subject of radiation effects in silicon devices is described in other works referenced below [7, 8, 10, 26]. The R&D activity propaedeutic to the TDR has included the evaluation of the radiation effects on SiPM [11, 12, 13, 14, 15] and on electronic devices used to implement the basic functions of the readout system. An irradiation test was performed at the CN facility of the INFN Laboratori Nazionali di Legnaro (LNL) on a sample of the "EASIROC" ASIC developed by the Omega group of the LAL, Orsay, France [16, 17], an ACTEL FPGA and a few samples of low power current feedback operational amplifiers. The CN facility of the LNL has a beam line delivering 4 MeV ^{2}H+ ions to a beryllium target; the energy spectra of the neutrons produced in the ^{9}Be(d,n)^{10}B reaction are shown in Fig. 13.25 where the 4.2 MeV curve is highlighted for convenience.

Fig. 13.25 shows instead the stack of boards carrying the ASIC, the FPGA and the op-amps installed right in front the beampipe, and the thermally isolated SiPM box located right after, at about 4 cm from the beam pipe. Some results of the irradiation tests are presented in the table of Fig. 13.27 below. The OMEGA EASIROC, manufactured in the 0.35 μm SiGe technology of Austria Micro Systems, was exposed to an estimated total of 1.7*10^{11} neutrons, equivalent to a few year's exposition to the Super*B* IFR operating conditions.

The outcome of the test showed that, as expected, while the FPGA configuration memory contents was not corrupted, the on-chip SRAM blocks and the registers in the FPGA fabric were subject to upsets. It follows that any critical part of the FPGA design should include suitable SEU protection functions.

It is worth noticing that no SEU afflicted the EASIROC configuration registers, that no latch-up occurred and finally that no evidence of TID damage was found while comparing the current consumption and the analog performances before and after the irradiation test [15].The op amps to be tested had been fastened to the top of the FPGA and have thus been irradiated with a fluence of the order of 10^{12}neutrons/ cm^2 with no noticeable effect on their current consumption or DC offset.

The results of the preliminary irradiation tests supported the decision on how to build and where to install the front end stages of the IFR readout system. As more neutron irradiation tests on SiPM are planned to assess the radiation tolerance of the latest generation devices, there will be more occasion to test, at the same time, more sample of ASICs built in the AMS 0.35 μm technology at different neutron energies and with different beam orientations w.r.t. to the device under test.

The 0.35 μm CMOS technology from AMS is being tested because it represents the preferred choice for the development of a dedicated ASIC, as described in the next chapter.

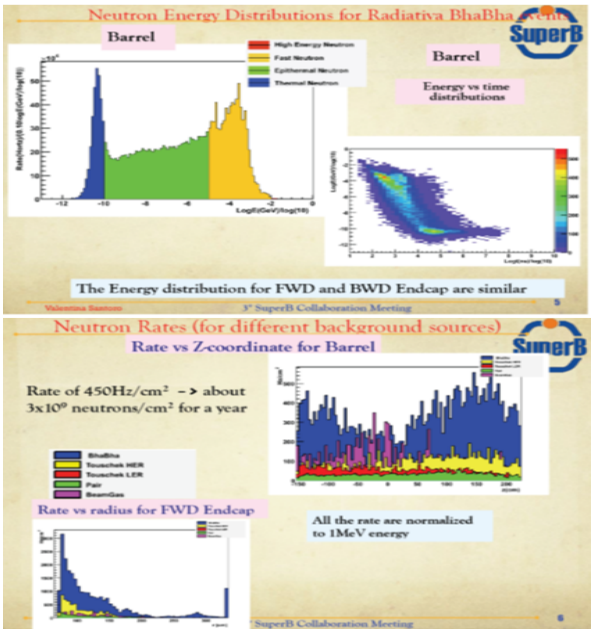

Figure 13.23: background neutrons: energy spectrum and rates (normalized to 1 MeV)

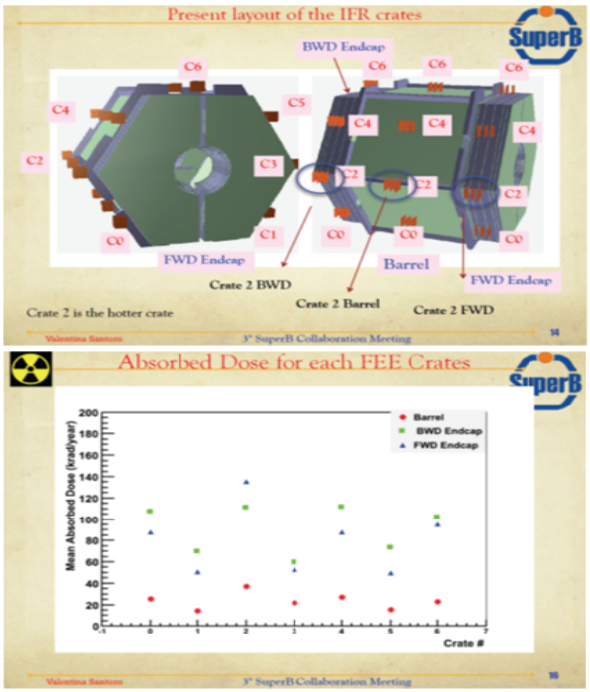

Figure 13.24: background neutrons flux: doses (krad/year) measured at some relevant locations around the detector

13.1.5.6 The IFR readout system

IFR readout basics: outline of the IFR prototype readout The basic principles informing the design of the IFR readout system have been tested with the IFR prototype, which was readout in the "binary" mode described above. For the prototype readout a dedicated front end board, the "ABCD", was built from off-the-shelf components (COTS); Fig. 13.28 shows the "ABCD" block diagram.

The main functions which were implemented on the 32 channel "ABCD" board are:

- individual "high side" regulation (with 12 bit resolution) of the SiPM bias voltage; bias voltage and SiPM signal are carried by the inner conductor of the coaxial cable, whose outer conductor is at true ground potential
- wideband (1,5GHz 3dB frequency) amplification of theSiPM signal
- discrimination of each SiPM signal against an individually programmable (with 12 bit resolution) threshold voltages; the discriminators (two per channel) used A.C. coupled feedback to stretch the output pulse to a width of about 20 ns
- sampling and buffering of the discriminators outputs pending the trigger signal from the experimental trigger system; an ALTERA Cyclone III FPGA was used to sample the discriminated SiPM signals and store them in an internal latency pipeline running at 80MHz.
- trigger processing: with each trigger a set of 10 samples was extracted from the latency pipeline and transferred to an output buffer (along with suitable framing words) from where they reached the "BiRO_TLU Interface board" [19] acting as a crate_wide data-collector and interface to the DAQ PC and to the experiment's TLU (Trigger Logic Unit).
- The DAQ system developed for the IFR prototype readout also performed functions

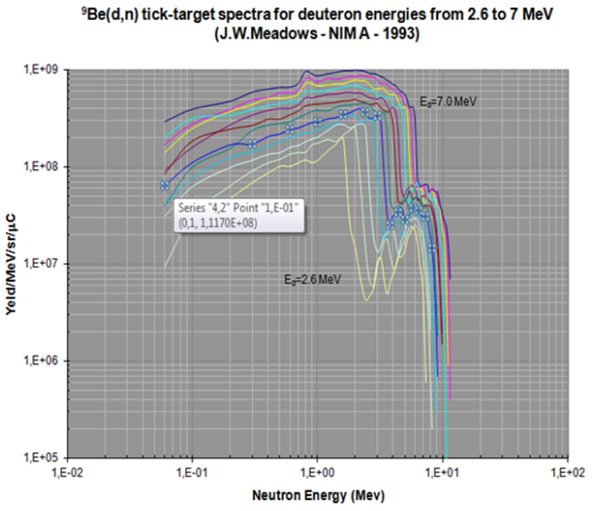

Figure 13.25: energy spectra of the neutron beam delivered by the CN line of the INFN-LNL) measured at some meaningful locations around the detector

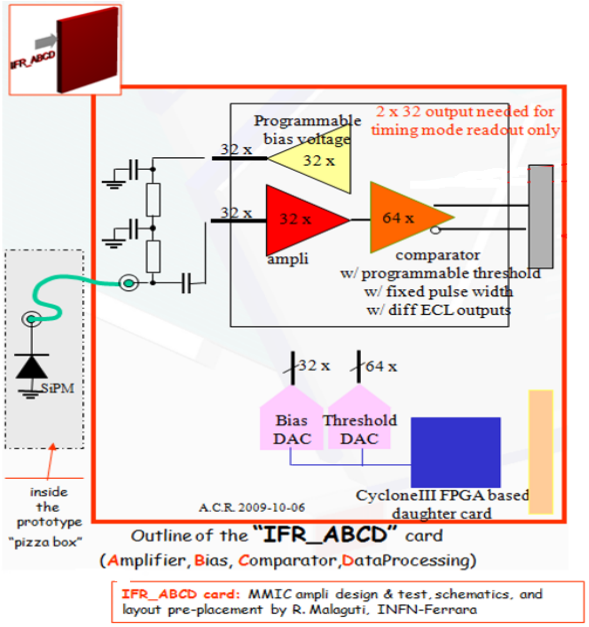

Figure 13.28: basic features of the "ABCD" card designed for the IFR prototype readout

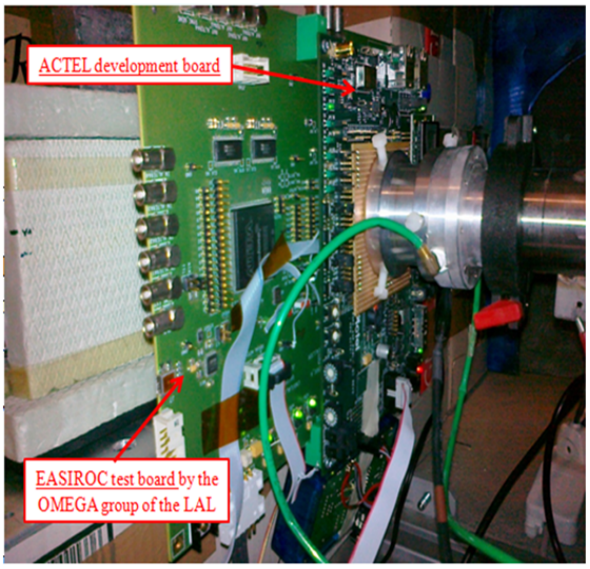

Figure 13.26: irradiation test setup at the CN facility of the INFN Laboratori Nazionali di Legnaro

which would, in Super$B$, be performed by the Experiment Control System (ECS): ambient temperature acquisition, calculation and download to the ABCD DACs of new set points for the bias voltages to stabilize the SiPM gain against the operating temperature variation [4].

- The Fermilab beam tests of the IFR prototype have demonstrated, among other things, that connecting the SiPMs to the front end cards by means of long (4m) coaxial cables, although not optimal, was possible and resulted in a reliably operating system.

total integration time (sec)	60683			
total charge (uC)	4104			
^{9}Be(d,n) thick target yield at 0 angle (YIELD/sr/uC) (ref. 13.5.1_r15)	1,017E+09			
	ACTEL A3PE250-PQ208			EASIROC
distance from source (mm)	7			20
total fluence at the target (neutrons/cm^2)	6,118E+12			1,033E+12
total fluence at the DUT (neutrons)	**4,955E+12**			**1,694E+11**
	CONFIGURATION MEMORY BITS	SRAM BITS	FLIP FLOP	FLIP FLOP
total memory element monitored	N.A.	32768	5824	456
number of SEU detected	**0**	**752**	**26**	**0**
number of SEL detected	**0**			**0**

Figure 13.27: results of the irradiation tests at the CN of the INFN Laboratori Nazionali di Legnaro

- This result supported the current baseline choice of locating the SiPMs near the scintillator bars and far from the front end cards, so that these last can be installed at more convenient locations.

An ASIC based front end readout

The COTS-based design of the "ABCD" card met goals such as short development time and flexibility (especially needed for tuning the parameters of the channels to be read out in the "timing" mode, cfr. the "white book", [20]) but it wouldn't be convenient for large volume production.

A search for existing ASICs suited for "binary mode" processing of SiPM signals was started and a good candidate was found in the "*Extended Analogue Silicon pm Integrated Read Out Chip*" or EASIROC which had many features already suited for the IFR readout application ([16], [17]); Fig. 13.29 shows a block diagram extracted from the EASIROC datasheet. The

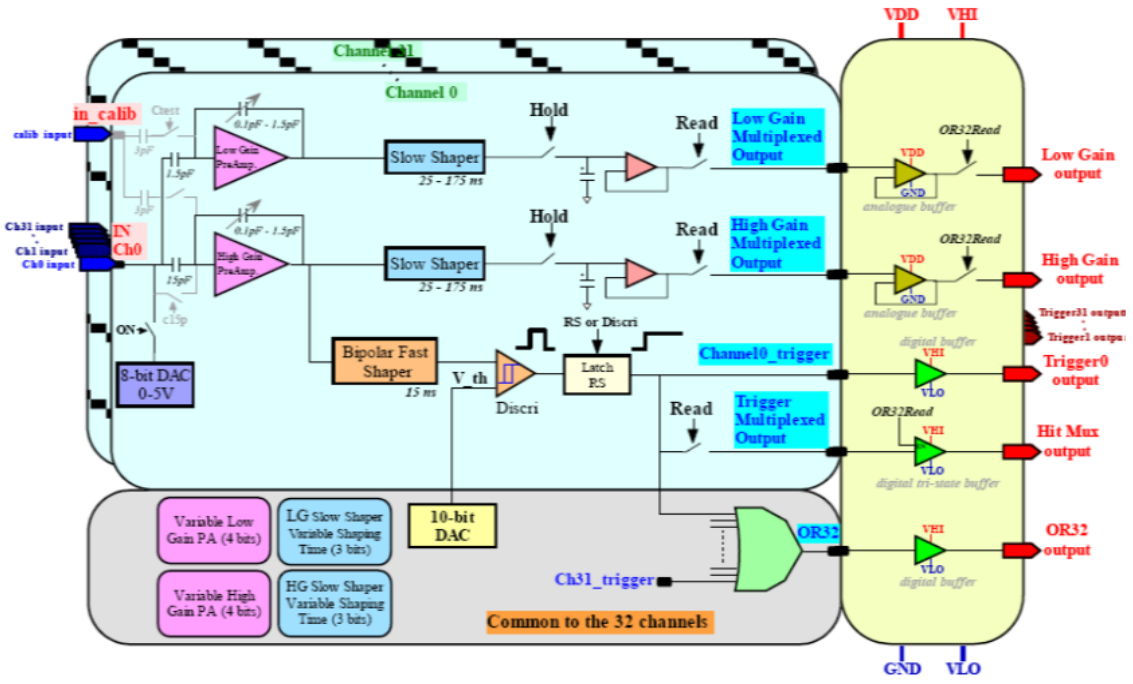

Figure 13.29: EASIROC block diagram developed by the OMEGA group of the LAL, Orsay, France

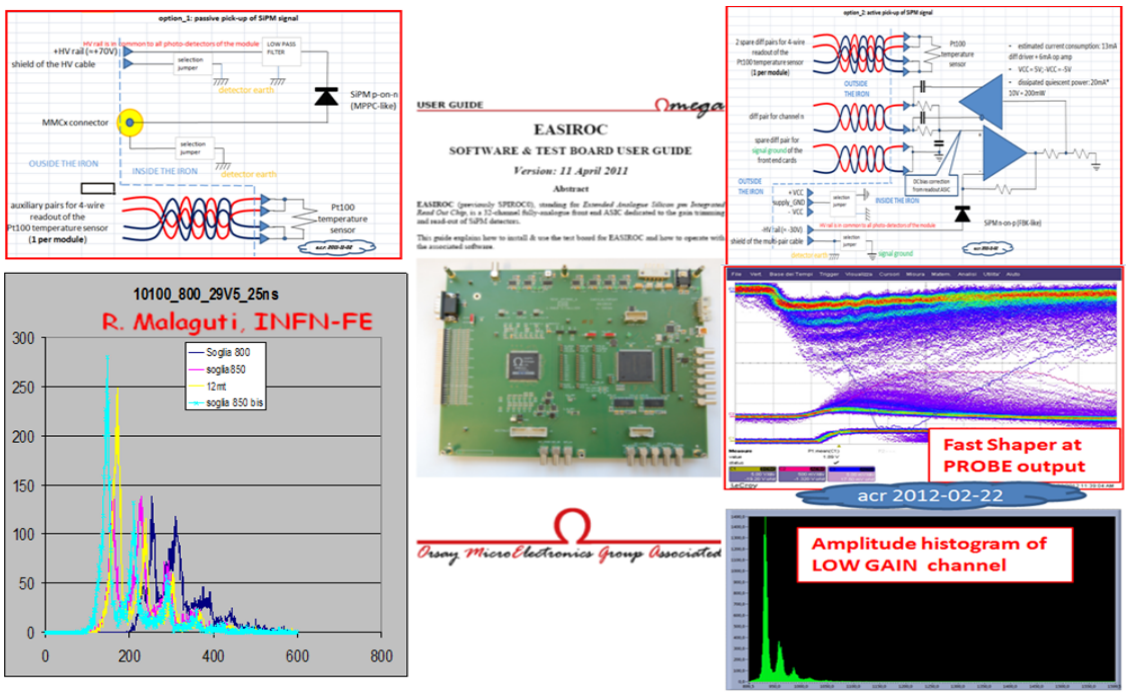

Figure 13.30: Amplitude histograms of signals processed by the EASIROC; SiPM connected with coaxial cables up to 12 m (left option) and with one differential pair of a high density cable 8 m long (right option)

EASIROC has been used, thanks to the test board and utilities provided by the OMEGA group, to test different SiPM technologies and coupling schemes [21]; Fig. 13.30 shows, for instance, pulse height histograms obtained from a 1 mm^2 SensL SiPM connected to the EASIROC via:

- different lengths of coaxial cables, up to 12m (left option)
- one differential pair of a high density, double shielded, multi twisted pair cable 8m long (right option)

The features of the EASIROC which would suite the IFR readout application are:

- the integration of 8 bit DACs, one per channel, for "low side" adjusting the bias voltage of the SiPM
- one fast (15 ns peaking time) shaper stage for each channel driving the "trigger" comparators
- the integration of a 10 bit DAC, common to all channels, for setting the threshold of the fast "trigger" comparators
- the availability of all 32 "trigger" outputs at the I/O pins (with single ended LV-TTL level) of the EASIROC
- low power consumption
- no sign of performance degradation or SEE detected during or after the irradiation tests descried above

The suitable specifications listed above are partially counterbalanced by others features which make the EASIROC not quite usable as it is, the most important of which being the 15ns peaking time of the fast shaper: a lower value is necessary to cope with the increasing dark count rate for SiPMs operating in the Super$B$ radiation environment.

As the IFR collaboration has been growing in the last year to include groups experienced in VLSI design ([22], [23], [24], [25], [26], [28], [29]), the development of an ASIC implementing the front end stages of the IFR readout system has become within reach; the EASIROC and an auxiliary flash based FPGA could still be considered as building blocks for a backup solution.

The new IFR front end ASIC should implement a set of basic features:

- a preamplifier and shaper chain suited for positive and negative input signals characterized by a linear response up to about 100 times the peak amplitude of the signal from a single photoelectron and a peaking time not larger than 10ns to minimize the pulse pile-up effects at high input rates
- individual DACs to set, with a few mV resolution, the DC level of each input and thus the "low side" bias voltage for the DC coupled SiPM; the current drive of the DAC should be designed considering the increase in dark current of irradiated SiPMs
- a fast comparator design, possibly differential to reduce the switching noise; some of the digital outputs should be routed to I/O pads
- one threshold setting DAC with a resolution of at least $\frac{1}{4}$ of the single p.e. signal and a linear range not larger than $\frac{1}{4}$ of the linear dynamic range
- a configurable test pulse injection circuits
- a slow control interface logic: a simple serial protocol should be implemented in order to perform write and non destructive readback to/from all register controlling the ASIC's programmable features
- a clock interface unit: to avoid the need of on-chip PLLs the ASIC will receive an LVDS clock with a frequency multiple of the experiment clock to derive all on-board timing signals; a suitable reset signal should also be foreseen
- a trigger primitives generator: a LUT based block driving two trigger outputs

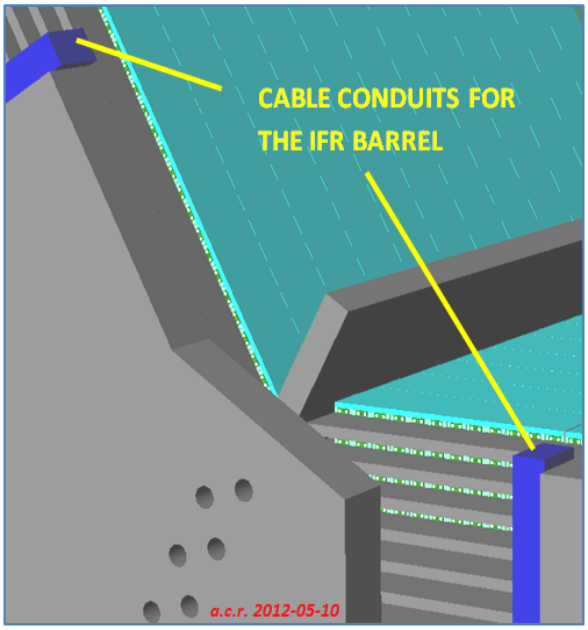

Figure 13.32: The IFR cable conduits for 2 sextants

- SEU protection through TMR or Hamming coding for all key registers and state machines in the ASIC

and a set of application specific features such as:

- a configurable latency buffer: a dual ported memory whose width would be equal to the number of channels and whose depth would be determined by the trigger latency time interval. The constant (but configurable) offset between the write pointer and the read pointer would equal the trigger latency time expressed in terms of clock periods
- a trigger interface: a trigger matching logic would detect a trigger pulse from the experiment, wait for the relevant data to be extracted from the latency buffer and subsequently forward it to the output serializer
- a set of low power serializers clocked by the input clock (which has a pace multiple of the experiment clock) needed to transfer the trigger matched data to the downstream "data collector" units. Serial output data could be 8b/10b encoded to allow the usage of DC-balanced AC coupled transmission links

The features listed above are differentiated into a first set, mainly analog, and a mainly digital second set to point out that it might be convenient to implement the two lists of functions in two different ASICs, to increase the flexibility of the overall system. Fig. 13.31 presents a block diagram of the new IFR readout ASIC and its connection to the SiPMs in the detector module; an IFR ASIC with a modularity of 32 channels would be able to readout all SiPMs in one module of the barrel. As shown in the inlay of Fig. 13.31 a ribbon-coaxial cable, mass terminated to a high density connector, could be used to carry the signals from the sensors to the IFR readout ASICs and the ancillary components on the IFR front end cards. At the right side of the IFR ASIC diagram one can find the input and output ports which would connect the IFR ASIC to the downstream "data merger" cards.

Location of the front end stages of the IFR readout system The SiPMs would be installed, in the baseline design, directly on the scintillator bars and thus distributed at different locations inside the modules. The baseline design foresees, instead, to install the ASIC-based front end stages outside the modules, at close but accessible locations. The reason behind this choice is that even if we were to install the front end ASICs inside the modules we would not still be able to directly connect (in order to minimize the signal/noise ratio) the SiPMs to the ASICs but, in turn, we would make it more difficult to remove the heat dissipated by the front end and we would make it impossible to access the front end cards, to replace faulty ones for instance, without disassembling large parts of the IFR structure. Fig. 13.32 is a detail of the IFR barrel which shows the position of two of the 5" x 3" conduits through which the IFR detector signal and power cables are routed.

The printed circuit board featuring the front end stages of the IFR signal processing chain could be located in these cable conduits; they

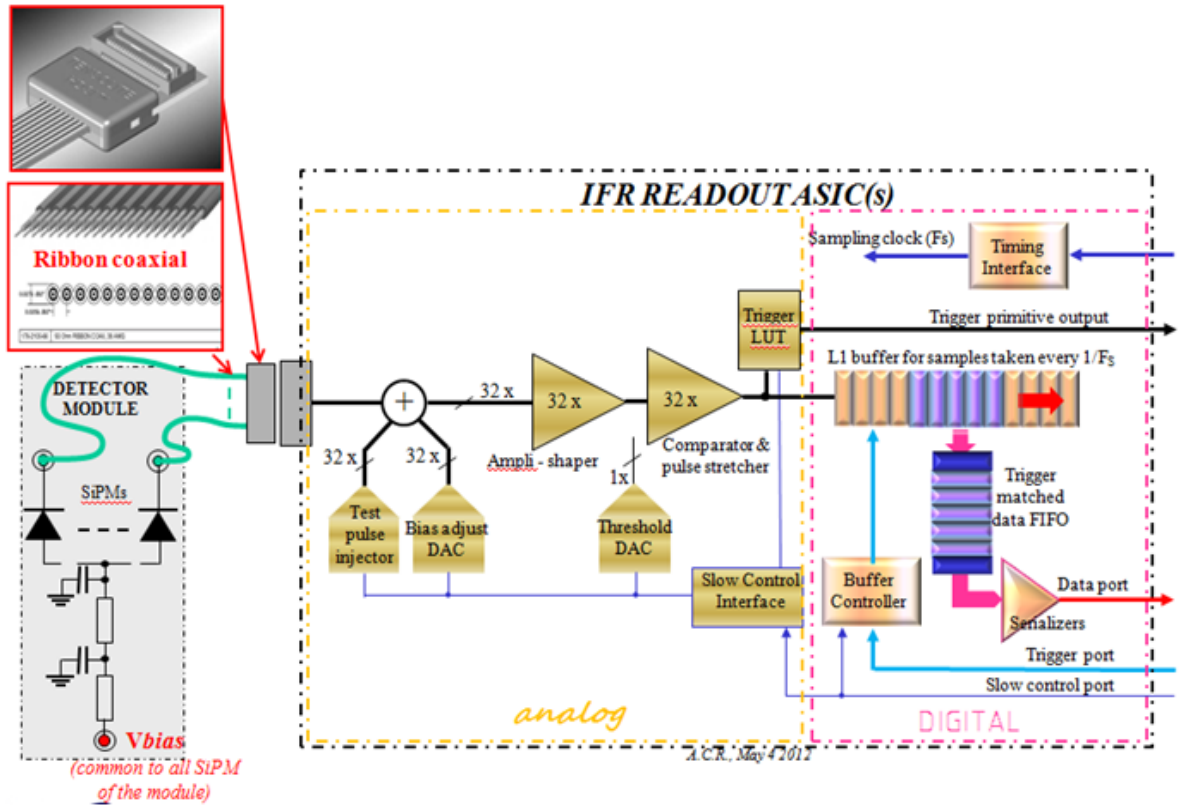

Figure 13.31: Block diagram of the IFR readout ASIC

would be accessible, if needed, without removing structural elements of the IFR magnetic flux return. Fig. 13.33 shows a section of one IFR cable conduit with a stack of 4 boards in evidence. Each IFR front end board could host 2 ASICs with 32 input channels each and since the IFR modules in the barrel are equipped with 32 SiPM at most, a stack of 3 to 4 IFR front end cards can handle all SiPMs installed in an active layer; 9 active layers are foreseen in the IFR detector.

All signals to and from the 2 front end ASICs on a board are coming from the "data merger" cards downstream, physically located as close as possible to the end of the cable conduit emerging from the Super$B$ spectrometer, as illustrated in the next paragraph. The interconnection cables are shown on the right side of the figure: they are double shielded, 17 pair, Amphenol SpectraStrip part number 425-3006-034 fitted with connectors by KEL (part no. KEL 8825E-034-175D); the mating connectors on the front end and the data merger PCBs are KEL 8831E-034-170LD. Not shown in Fig. 13.33 are the power cables for the SiPM bias (one common bias voltage per detector module) and the front end card voltage supply.

The section of the cable conduit can accommodate all boards and cables needed for the 9 active layers of each barrel sextant. Not shown in the picture are also the copper pillars which are foreseen to build a thermal conduction path from the IFR front end card to the IFR steel to which the cable conduit is fastened. In alternative to using ribbonized coaxial cables, the individual coaxial cables carrying the SiPM signals from one module are soldered onto a suitable interface PCB as shown in Fig. 13.34. The multi coaxial assembly shown in this 3D drawing features a SAMTEC QSE-20-01-F-D high density connector which mates to a QTE-020-01-F-D installed on the IFR front end PCB.

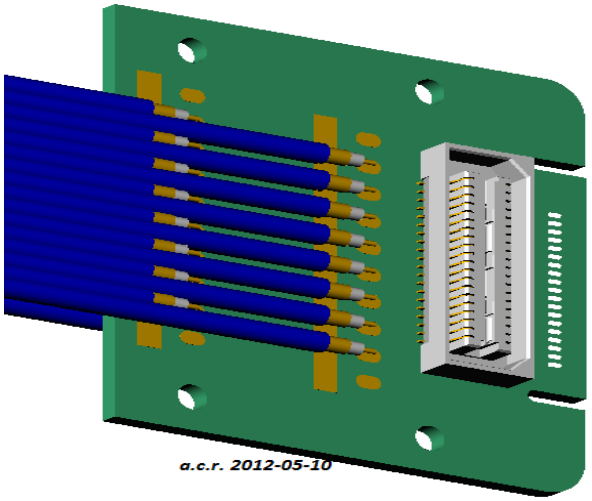

Figure 13.34: Detail of the multi coaxial connector assembly

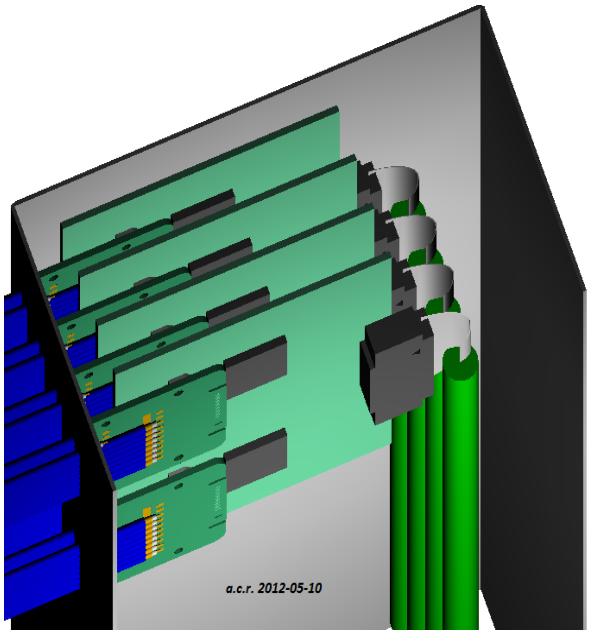

Figure 13.33: Detail of front end cards installed in the IFR cable conduit

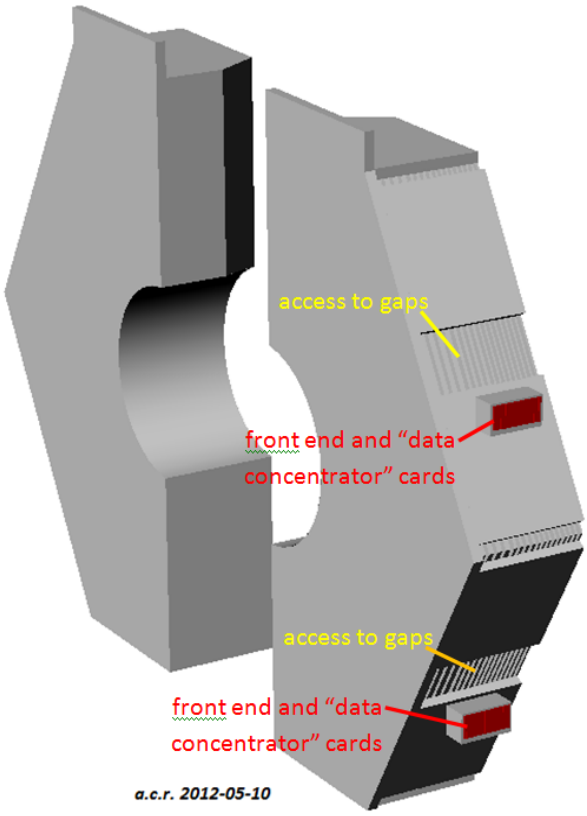

Figure 13.35: Perspective view of IFR endcaps

The description above concerns the instrumentation of the barrel section of the IFR detector. Fig. 13.35 below shows the perspective view of a pair of endcaps: the yellow callouts indicate the openings in the side lining steel through which the signal and power cables for the IFR modules can be routed. The signal emerging from these openings are routed to the crates indicated by the red callouts. For the endcap section of the IFR, the front end cards carrying the IFR read out ASIC could be installed directly in the crate and connected to the "data merger" cards through the crate's backplane interconnections.

The IFR "data merger" crates The IFR front end cards are linked to the "data merger" cards from which they receive the timing and trigger signals and to which they confer the trigger matched data. Fig. 13.36 shows the main functions performed by the units installed in a data-merger crate:

- FCTS interface: the key element of this functional unit is the FCTS receiver module which is linked via optical fiber to the Super*B* Fast Control and Timing System (FCTS). The FCTS interface unit fans out to the IFR front end cards the timing (clock and reset) and the trigger commands decoded by the FCTS protocol receiver

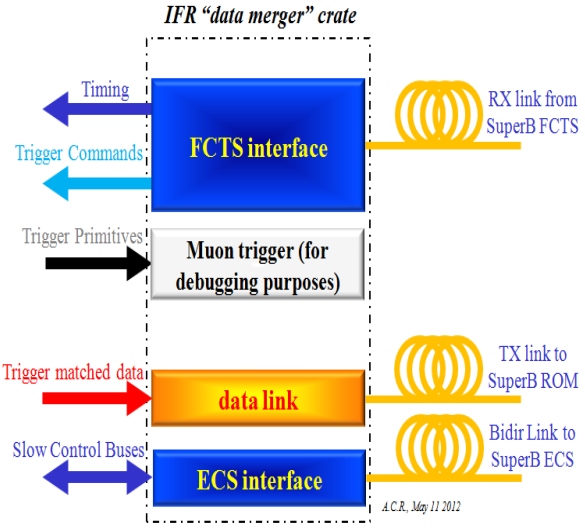

Figure 13.36: Main functions performed by the electronic units in the data-merger crate

- Muon trigger module: this unit receives the trigger primitives generated by the IFR front end cards and combines them to generate a muon trigger for local debugging purposes
- data link: each data-merger crate is supposed, according to the baseline design, to drive a suitable number of data links (4 for the barrel section, 2 for the endcap ones) to the ReadOut Modules (ROM). The data forwarded to the ROMs results from the merging of the trigger-matched data streams produced by the front end cards. A suitable modularity could be of 2 ouput data link per concentrator board; this functional unit will rely on the common TX link driver module to reliably forward data to the ROM even in the radiation environment of Super*B*
- ECS interface: the key element of this functional unit is the ECS receiver module which is linked via optical fiber to the Super*B* Experiment Control System (FCTS). The ECS interface unit controls the whole tree of slow control slave nodes implemented in the front end cards

For the endcap section of the IFR the physical links between the front end and the data merger boards consist of the differential lines provided by the backplane in which the front end and the data-merger units are installed. An ATCA or Micro-TCA crate [26] provide a large number of such interconnection resources and the IFR data merger crates will most likely conform to one of the two above mentioned TCA specifications.

Because of the Super*B* radiation environment it is likely that in the IFR data merger crates the standard "intelligent platform management" controller will be replaced by some ad-hoc interface card hooked to the Super*B* ECS. The power supply units of the IFR data merger crate would have to be radiation tolerant or simply be installed at a larger distance from the crates; the xTCA crates integrated "power entry modules" are fit to both options. The xTCA fans will have to be tested for operation in a radiation environment or replaced with qualified units; the convection cooling specification could be somewhat relaxed, on the other hand, since the data merger crates will most likely dissipate much less than the allowed 150W/200W per slot. Fig. 13.37 shows the proposed location for one of the barrel data-merger crates.

Two other such crates would be placed at 120° on the forward end of the barrel while three crates will be located in a similar arrangement at the backward end of the barrel. Each data-merger crate serves two sextants.

Services needed for the IFR readout in the experimental hall The elements of the IFR readout system, from the detector on, need to be properly powered, monitored and cooled. This paragraph summarizes the main requirements for a readout system built according to the baseline design (which have been described in more detail in the "Super*B* integration questionnaire"):

- SiPM supply voltage: all the SiPMs of a detector module are connected to an ASIC

input with one terminal and to a common bias voltage bus with the other. A total of 492 power supply channels are then needed for biasing the SiPMs; the channel should feature a programmable output voltage ranging from 0 to 100V (value and polarity depend on the final SiPM technology chosen) and should have a compliance of 25mA. The power dissipated by the SiPMs in the whole IFR under nominal operating conditions is of the order of a few tens of Watts

- IFR front end cards: a very coarse estimation of the power consumption for the IFR front end cards could be of 2W at 3.3V. Lower core voltages for the ASIC could be derived from on-board by means of low-drop out regulators; the radiation tolerance of suitable LDO regulators is being characterized. The number of modulo-32 processing units necessary to readout the IFR detector is **384 for the barrel** and **324 for the endcaps**. In the baseline design each front end card carries 2 ASICs in the barrel and, possibly, 4 ASICs in the endcaps, so the number of individually programmable power supply channels would be **192 for the barrel** and **81 for the endcaps** The compliance of these channels should be at least 1A.
- barrel cooling: the power dissipated by the SiPMs and the front end cards in the barrel could be in the order of 700W. Assuming that a cooling system like that designed for the *BABAR* flux return system will also be foreseen for the Super*B* detector, the power dissipated by the front end stages in the IFR steel should be taken into account for properly dimensioning the chiller system

13.2 Electronics Infrastructure

13.2.1 Power supplies, grounding and cabling

Gianluigi Pessina

13.2.1.1 Power Supply to the Front-end:

The voltage supply system is normally composed by a cascade of AC/DC, DC/DC and linear regulators. Depending on the power dissipation and noise requirements some of the above elements can be avoided. The supply system of an accelerator-based experiment has known additional constraints to be satisfied. The large particle fluence and the presence of a strong magnetic field can have an impact on the aging and behavior of the electronic equipment. The first constraint is addressed only by adopting radiation hardened (rad-hard) technology and using suitable layout recipes for the monolithic circuits. This is common to all the devices that sit in the detector area. Magnetic field has generally less impact except for AC/DC and DC/DC converters that need to use inductances and/or transformers, having ferromagnetic cores.

Power Supply outside the detector area: In the following we will describe our solution, able to face the above constraints. The strategy we

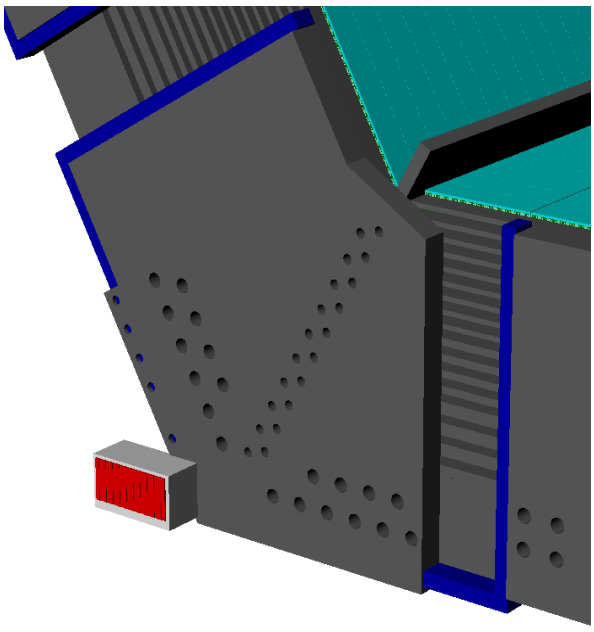

Figure 13.37: The location of one of the 6 data merger crates for the barrel

would adopt is to minimize the number of regulators in the detector area. The distance between the regulators and the front-end can be a few tens of meters. The energy the cable is able to store in its inductive component can be large and attention must be adopted to protect the connected electronic equipment in case of accidental short circuit to ground. Fig. 13.39 shows an example of the recovery from a short circuit of $50\,m$ cable with $4\,mm^2$ section. The short circuit current was limited to $20\,A$. A N-MOS, IPP50CN10NG, with $50\,m\Omega$ ON resistance simulated the short circuit and it breaks down above about $100\,V$ when in open state, that explains the reason of the clipping. The measurement has been taken in the worst condition of no applied load. It is clear from this that an accidental short circuit is very critical in producing possibly destructive damaging.

We have found that most of the cables with 3 or 4 poles and cross-section between $1.5\,mm^2$ and $4\,mm^2$ have an inductance per unit length, L_M, of the order of $0.7\,\mu H/m$, from DC to few hundred of KHz. Calling I_{short} the maximum delivering current available from the power supply and l the cable length, then:

$$E_{nergy} = \frac{1}{2} L_M l I_{short}^2 \qquad (13.1)$$

is the available energy driven to the load in case of accidental short circuit. To limit the voltage at a safe level our straightforward solution is to add in parallel to the load a capacitance able to store such released energy. This can be done if we satisfy that:

$$\frac{1}{2} C_{lim} V_{over}^2 = \frac{1}{2} L_M l I_{short}^2 \qquad (13.2)$$

where V_{over} is the maximum voltage that must not be exceeded and C_{lim} is the capacitance whose value must be chosen to satisfy the eq. with the given voltage V_{over}. As an instance, with $50\,m$ of cable length, $I_{short} = 20\,A$ and $C_{lim} = 160\,\mu F$ the maximum over voltage excursion would be less than $9.5\,V$.

Adopting the introduced technique a hub with a distribution to several shorter cables can be implemented as shown in Fig. 13.40. A large value capacitance, C_H, is at the end of the cable that connects the DC/DC regulators from the outside to the inside of the detector area. In our example we continue with considering $50\,m$ of cable length and $C_H = 160\,\mu F$. From this point several shorter cables, or stubs, connect the various parts of the detector or sub-detector front-end. To save space, the sections of these last cables can be smaller since they have each to manage a smaller current. At the end of each of these stubs, $5\,m$ in our present example, a smaller value capacitance, C_{Fx}, $(33\,\mu F)$ is connected. In case of short at the end of a stub all the current flows into it. But as soon as the short is opened capacitance C_H absorbs the energy of the longer cable, while the energy of the shorted stub is managed by the corresponding capacitance C_{Fx}. Fig. 13.41 shows that the signal at the end of the $50\,m$ cable has an over voltage of only about $10\,\%$. The maximum current was $20\,A$ and it can be seen that the baseline before the short is released is about $2\,V$, the dropout generated by the $20\,A$ current across about $0.1\,\Omega$ given by the sum of the stub (as a

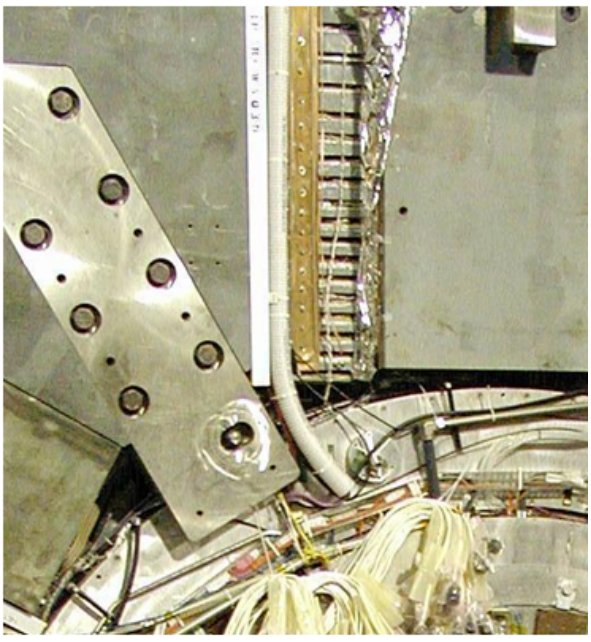

Figure 13.38: A picture from *BABAR* showing one of the elements of the cooling system for the IFR steel

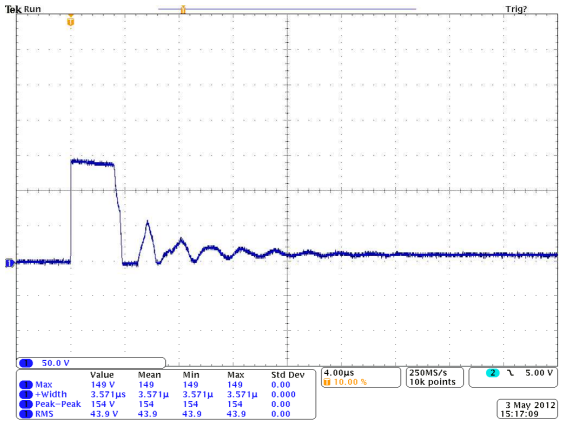

Figure 13.39: Signal at the end of a 50 m cable after a short circuit. The clipping at 150 V is due to the breakdown of the MOS switch used.

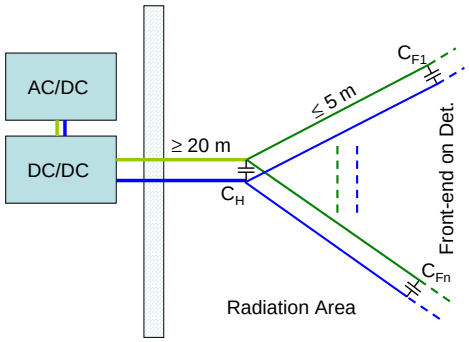

Figure 13.40: Possible layout for a sub-detector for what concerns voltage supply.

reference a section of $1\,mm^2$ has an impedance of about $16\,\Omega/Km$) and the ON resistance of the N-MOS. Fig. 13.42 shows the over voltage present at the stub end where the short is generated and released; again the over voltage is contained within about 10 %. As it can be appreciated, the baseline that precedes the release of the short is about $1\,V$, namely $20\,A$ developed across the about $50\,m\Omega$ ON resistance of the N-MOS. In the test setup of the laboratory we implemented 2 stubs and Fig. 13.43 is the signal at the stub end where the short circuit was not present. Again the over voltage is respecting the safety conditions. The principle applies well also if a low regulated voltage is considered and Fig. 13.44 is an example of release from a short of more than $25\,A$ on a $5\,m$ cable ($2.5\,mm^2$ of cross-section) loaded with $160\,\mu F$ capacitance.

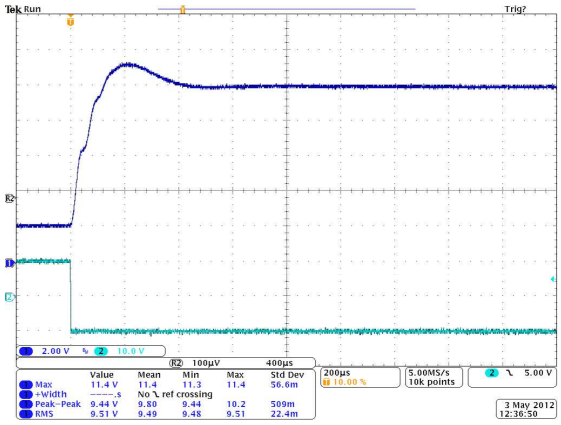

Figure 13.41: Signal at the end of a $50\,m$ cable (blue line) after that a short circuit is generated at one end of a stub. The $50\,m$ cable is loaded with a $160\,\mu F$ capacitor and the short current is $20\,A$; the supply voltage is $10\,V$. Every stub is loaded with $33\,\mu F$. The green line is the voltage driver at the gate of the switched N-MOS.

The suppression capacitance must show a very small series resistance and inductance. Capacitors with plastic dielectric such as Metalized Polypropylene Film satisfy this condition. As an example the $160\,\mu F$ we have adopted for the test has only $2.2\,m\Omega$ of series resistance, but, being big in volume, it shows a series inductance of a few tens of nH. To compensate for this last effect a smaller value (and volume) capacitance ($1\,\mu F$) is put in parallel, able to account for the fast part of the rising signal. Metalized Polypropylene Film capacitances have a range of values limited to a few hundreds of μF. As a consequence, a limited value of current per cable, $10\,A$ to $20\,A$, results in a good compromise. Many commercial regulators, also in the form of the so called bricks and half-bricks layouts, are available on the shelf at low cost. This strategy is particularly usefully for minimizing the

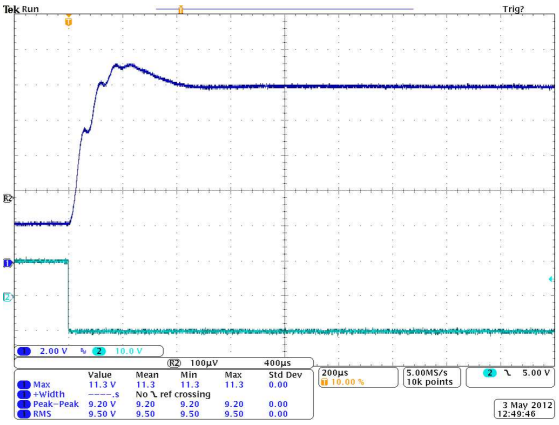

Figure 13.43: Signal at the end of a stub of Fig. 13.40 after a short circuit (blue line) happened at another stub. Two stubs were present in the test setup. C_H is $160\,\mu F$, the C_{Fx} are $33\,\mu F$ and the short current is $20\,A$; the supply voltage is $10\,V$. The green line is the voltage driver at the gate of the switched N-MOS.

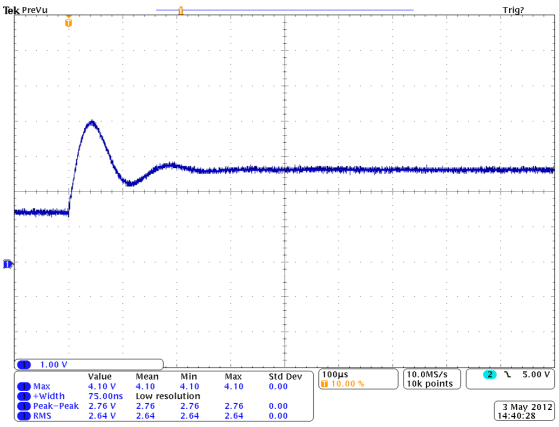

Figure 13.44: Short circuit release on a $5\,m$ cable with $2.5\,mm^2$ cross-section.

dropout along the cable and it is of particular concern when a low voltage is needed.

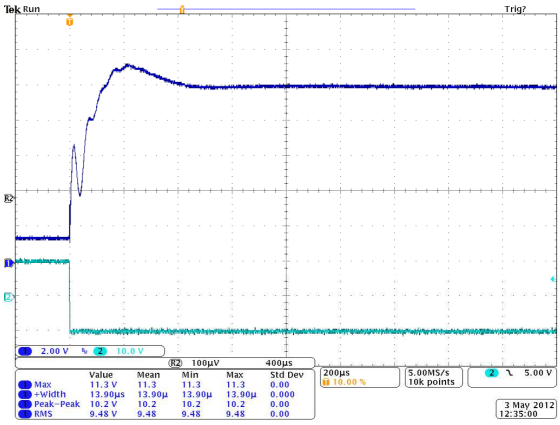

Figure 13.42: Signal at the end of a stub of Fig. 13.40 after a short circuit (blue line). Two stubs were present in the test setup. C_H is $160\,\mu F$, the C_{Fx} are $33\,\mu F$ and the short current is $20\,A$; the supply voltage is $10\,V$. The green line is the voltage driver at the gate of the switched N-MOS.

We cannot forget that an over-voltage can happen due to a possible malfunctioning of the regulator. To reject rapidly and with good precision this effect a stack of fast diodes is a good choice. For instance with a voltage supply of $10\,V$ the series connection of about 20 diodes allows to maintain the safe operating condition provided that they are in contact with a heat sink in case the problem persists for a while. The location of the stack of diodes can be close to the regulator and space occupation would not constitute a problem.

Noise cabling and shielding: The combination of the inductance component of the wires and the suppression capacitance has a twofold utility as it behaves also as a low pass filter. Fig. 13.45 shows the noise at the end of the $50\,m$ cable plus $2 \times 5\,m$ stubs when $160\,\mu F$ plus $2 \times 33\,\mu F$ capacitances load the combination. The applied supply voltage was $10\,V$ and the load $3.3\,\Omega$. In this case a standard commercial regulator has been used. Very low noise DC/DC regulators have been designed [30] and Fig. 13.46 shows the noise performance under the same conditions. Even better performances can be obtained by cascading the DC/DC to a linear regulator of very good quality [31].

Low noise results are obtained if care is considered on the type of cables adopted. In all the measurements described so far cables used

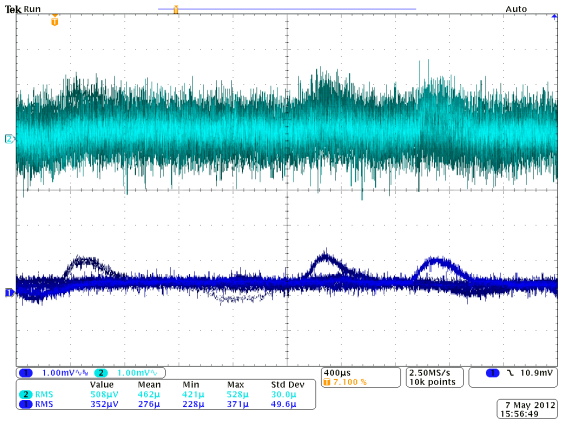

Figure 13.45: Noise after $50\,m$ cable loaded with $160 + 2 \times 33\,\mu F$ capacitance at $10\,V$ and with $3.3\,\Omega$ load. Upper noise is with the full $350\,MHz$ bandwidth of the oscilloscope, Lower noise has the scope bandwidth limited to $20\,MHz$.

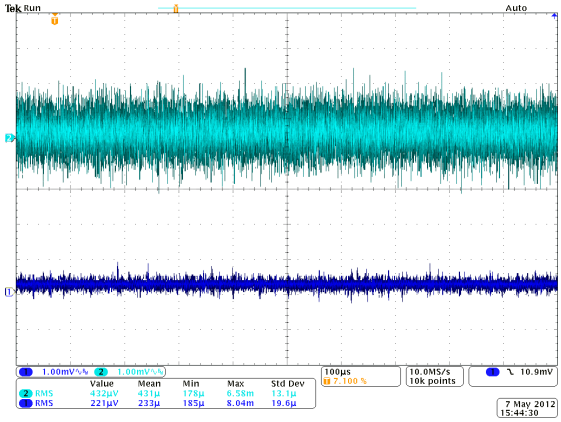

Figure 13.46: Very low noise DC/DC regulator [30]. Measurements condition and setup as for Fig. 13.45

were all armored. This precaution allows to shield the supply voltage from outside disturbances but also to avoid to create disturbances to the outside world. We intend to adopt this kind of layout solution for the final experimental setup. In addition, where needed, we intend to add a double shield by inserting the cables inside a tubular copper mesh.

The connection scheme of Fig. 13.40 is, in a natural way, suitable to route ground. Let's suppose that the ground of every detector or sub-detector to which the cables are routed have their ground isolated. Then, we can route a tinned copper wire (or a copper bar) very close to the power supply cables so as to suppress area sensitive to EMI interferences. Such a routing scheme allows a 'star' connection with only one ground contact node (we remember that AC/DC and DC/DC regulators are floating), that is the standard requirement.

Shielding is considered for whose region were the electric or magnetic field can affect the performances. The shields can be considered for the whole sub-detector or individually on a channel by channel basis. This is particularly true with the effect of magnetic field on those detectors that extend on a large volume, such as photomultiplier tubes (PMTs). Past experience showed that in these cases a local shield implemented with mu-metal around every PMT is essential.

Power Supply in the detector area: We are considering the opportunity to use both DC/DC and linear regulators inside the detector area. Inductances and transformers cannot be based on a ferromagnetic coil. As a consequence they are limited in range of values and the switching speed of the DC/DC must be very large. This is the case for the monolithic DC/DC regulator we are considering [32], developed in $0.35\,\mu m$ CMOS technology based on rad-hard layout and components, and having a switching frequency of the modulator of a few MHz, which allows the use of a coil-free inductance. Based on the same technology a linear regulator is also available [33].

13.2.1.2 High Voltage Power Supply to the Detectors:

High voltage power supplies suffer of similar problems as AC/DC and DC/DC regulators. As a consequence these regulators must be located outside the detector, sub-detector area (we do not know about any commercial rad-hard high voltage regulator). The energy released to the load in case of accidental short circuit would be not an issue thanks to the fact the, normally, such regulators have their driving current lim-

ited to a few hundred of μA. As an instance, if we load the line with a $1\,nF$ high voltage capacitor and considering $1\,A$ the short circuit current we expect an over-voltage of about $0.2\,V$. Finally, commercial over-voltage protectors based on gas discharge tubes are very efficient and fast.

13.2.2 Grounding and Shielding

This section has been incorporated in the Power Supply section

13.2.3 Cable Plant

This section has been incorporated in the Power Supply section

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