The upgrade of the VerTeX detector of the Belle II experiment

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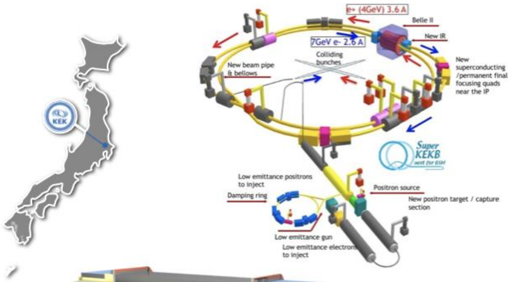
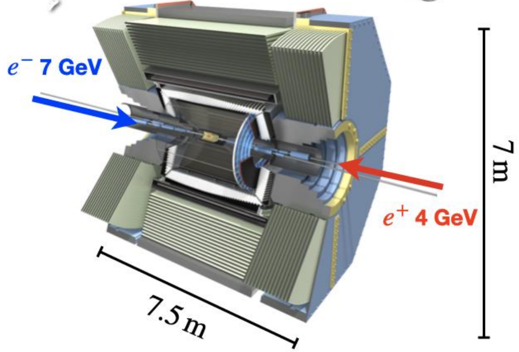
The Belle II experiment

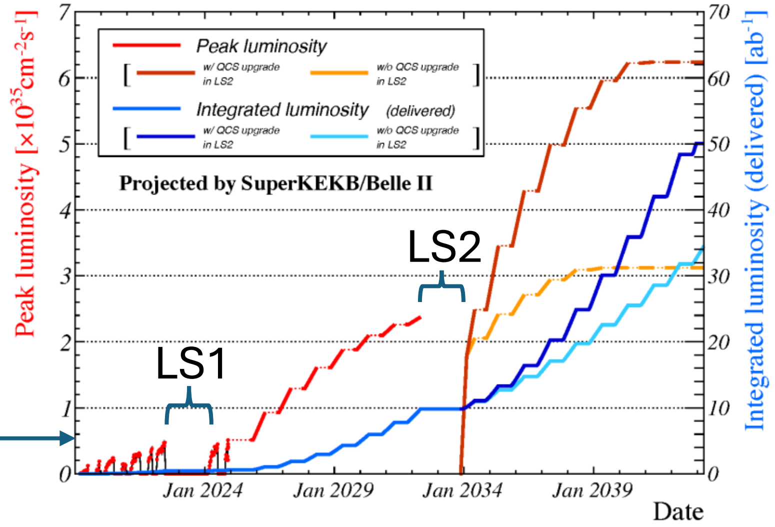
- Belle II searches for new physics at the luminosity frontier.
- Operates at the SuperKEKB collider (KEK, Japan):
  - Asymmetric e^+e^- collisions @$\Upsilon(4S)$ resonance (10.58 GeV)
- Belle II integrated luminosity goal: 50 ab^{-1} in 2042
- SuperKEKB exp. peak luminosity: $\mathcal{L} = 6\ \times 10^{35}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ (>× 10 current value)
- Present VerteX Detector (VXD) has excellent performance for current occupancy (< 2%)
- Limited safety margin and performance degradation in high background scenario at target luminosity
- **Belle II upgrade project** still to be approved, TDR in 2027
- New VerTeX detector (**VTX**) ⇒ high granularity, low material budget, operated at room temperature
  - 5 layers of pixelated sensors
    ⇒ new chip under submission (OBELIX)

Belle II & SuperKEKB





We are here
(5.2×10^{34}, world record)

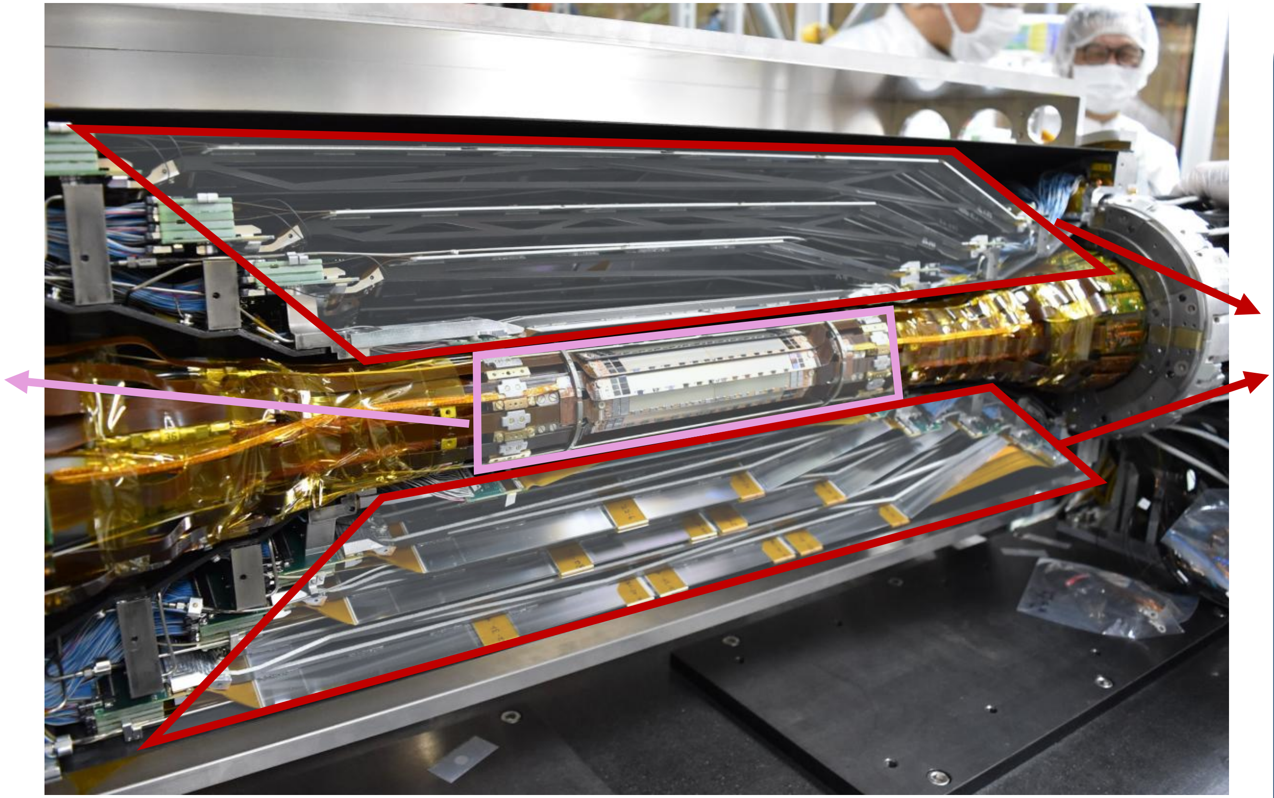


Current VerteX Detector (VXD)

Pixel Detector (PXD)

- 2 layers of DEPFET sensors
- 75 µm thick ($0.25\%\ X/X_0$)
- Long integration time (20 µs)

PXD damaged after major beam loss in 2024
⇒ kept off until machine operation stabilizes

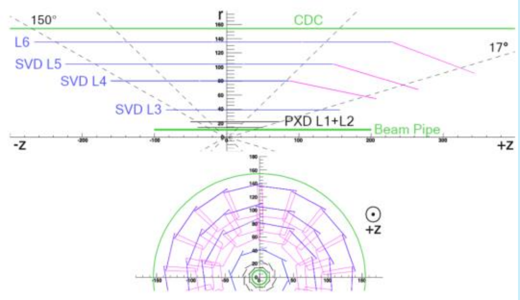


Cooling

- PXD matrix ⇒ N_2
- PXD electronics and SVD ⇒ CO_2 @-25 °C

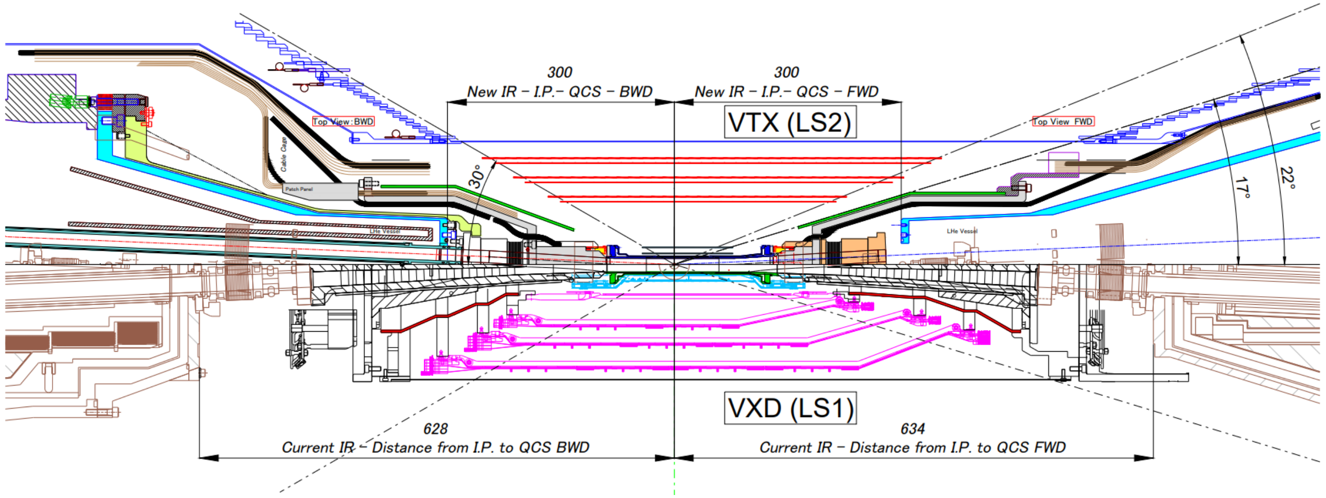
Silicon Vertex Detector (SVD)

- 4 layers of double sided silicon strip detectors (DSSDs)
- 300 µm thick ($0.7\ \%\ X/X_0$)
- Good time resolution (2 ns)
- Overall stable operation



New interaction region

- Luminosity goals require new interaction region (IR)
  - Current one can only arrive to 1/3 of target luminosity
- VTX geometry strongly constrained by **IR design**
- Closer magnets ⇒ less space for VTX ladders and services
- Acceptance reduction (17°-150° ⇒ 22°-150°)



VTX baseline

iVTX
- 2 silicon ladders layers
- High hit rate
- Low material budget
- Passive cooling

VTX requirements (from CDR)

- **Hit rate** up to 120 MHz/cm^2
- Fast time stamping (50-100 ns)
- **Resolution** < 15 μm ⇒ pitch of 30-40 μm
- Power consumption ~ 200 mW/cm^2
- Operation simplicity and reduced services ⇒ cooling @ room temperature
- **Radiation tolerance**:
  - TID ~ 100 Mrad
  - NIEL ~ 5×10^{14} 1 MeV n_{eq}/cm^2
- Light material budget
- **Depleted Monolithic Active Pixel Sensor** (DMAPS) technology chosen

oVTX
- taggered ladders layers
- ICE ITS2 inspired
- llenge: long ladders
- h low material budget
- ter cooling

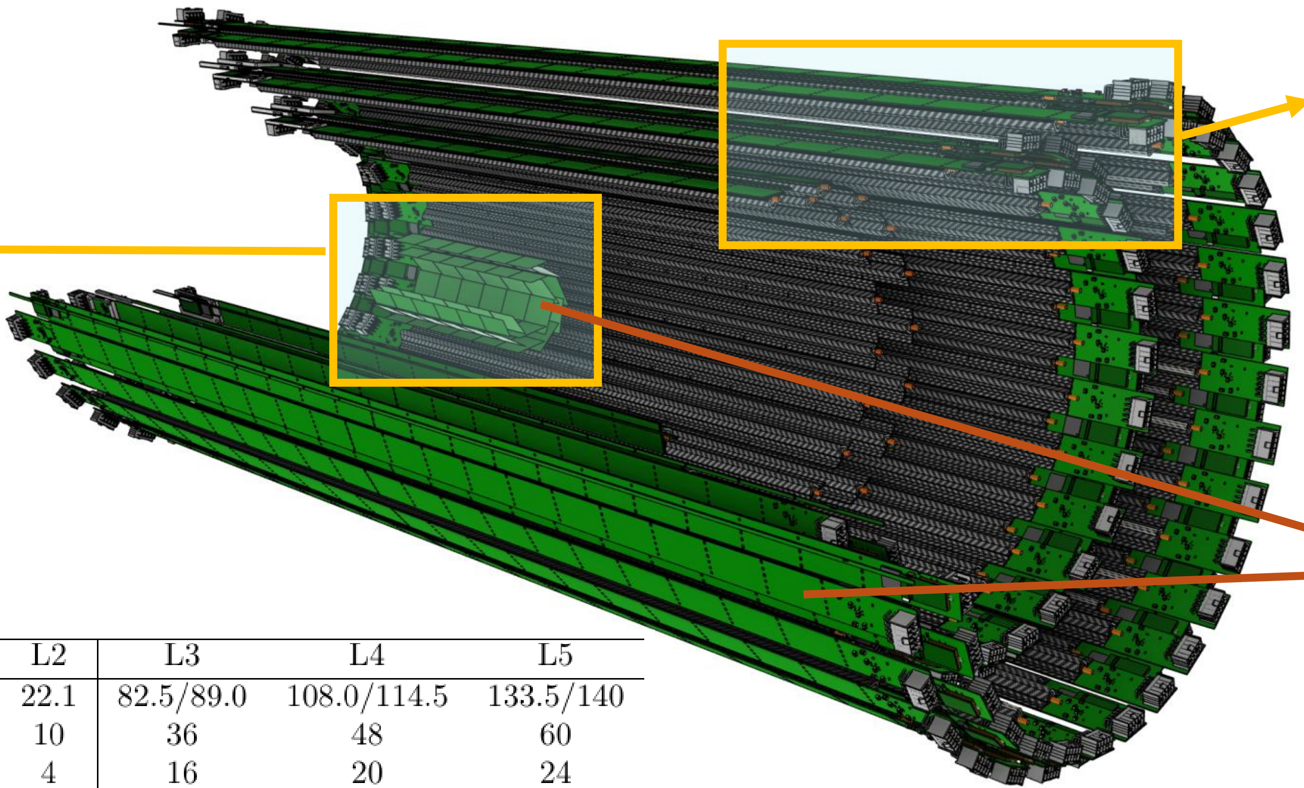
OBELIX
- Same CMOS DMAPS ilicon sensor used in all he 5 layers
- Developed according to Belle II requirements

	L1	L2
Radii [mm]	14.1	22.
# Ladders	6	10
# Sensors per Ladder	4	4
Exp. hit rate [$MHz\,cm^{-2}$]	34.0	16.
Material budget [% X_0]	0.3	0.3

2026 | 2027 | 2034

OBELIX-1 | TDR ⟶ Approval | OBELIX-2 | Start production | LS2 | Restart operations

VTX baseline



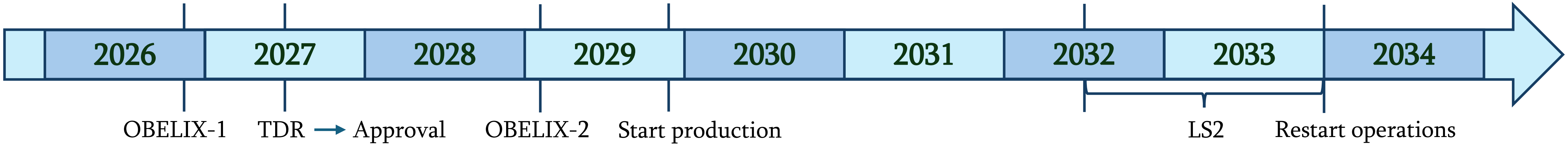
iVTX
- 2 silicon ladders layers
- High hit rate
- Low material budget
- Passive cooling

oVTX
- 3 staggered ladders layers
- ALICE ITS2 inspired
- Challenge: long ladders with low material budget
- Water cooling

OBELIX
- Same CMOS DMAPS silicon sensor used in all the 5 layers
- Developed according to Belle II requirements

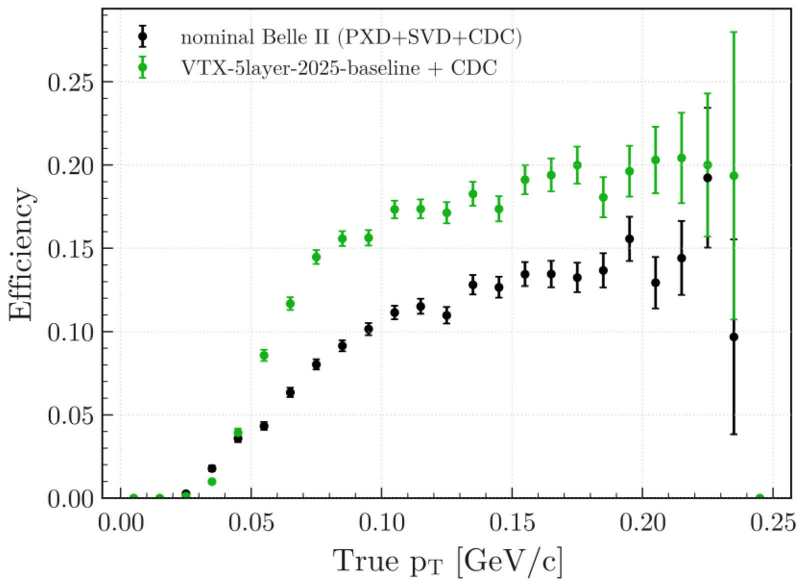
	L1	L2	L3	L4	L5
Radii [mm]	14.1	22.1	82.5/89.0	108.0/114.5	133.5/140
# Ladders	6	10	36	48	60
# Sensors per Ladder	4	4	16	20	24
Exp. hit rate [$\mathrm{MHz\,cm^{-2}}$]	34.0	16.2	0.76	0.40	0.26
Material budget [% X_0]	0.3	0.3	0.8	0.8	0.8

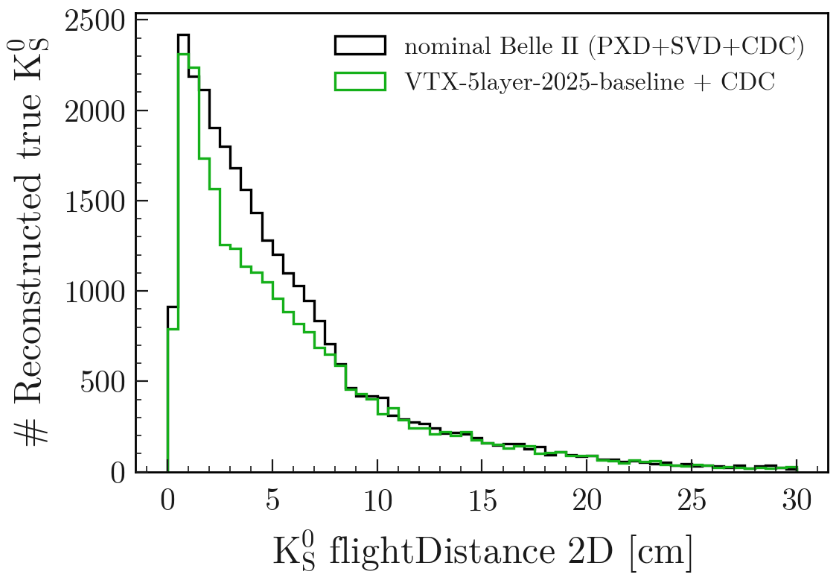
Specs ×4 max expected hit rate



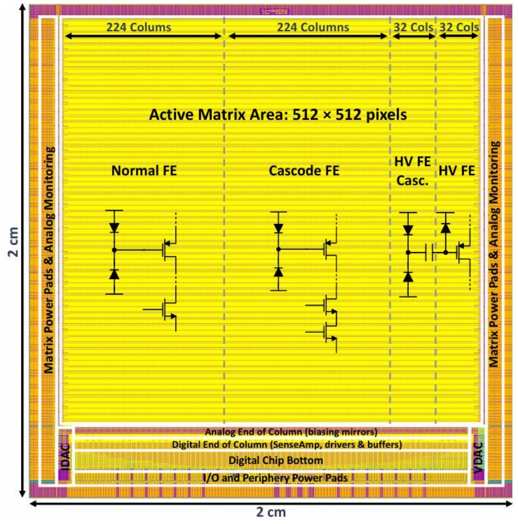
VTX performance

- Good performance despite IR constraints
- Significantly improved π_{soft} detection efficiency
- $\sim$30% better B vertex resolution:
  - 25 μm ⇒ 17 μm in conservative background
- But $\sim$15% lower K_S^0 efficiency:
  - Most affected by geometry changes due to space constraints
- Studies ongoing on performance with other post-LS2 detectors

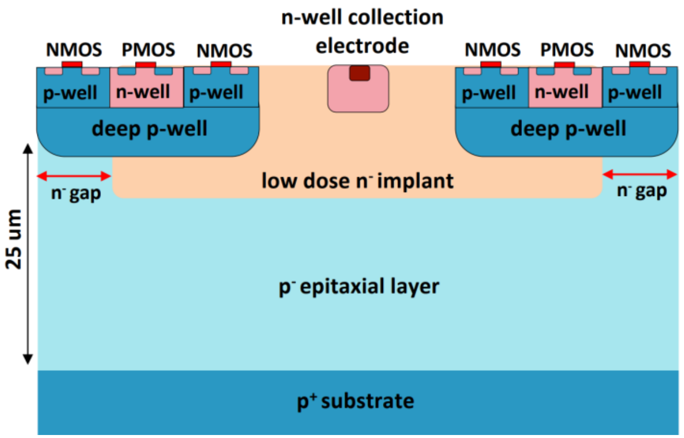




TJ-Monopix 2



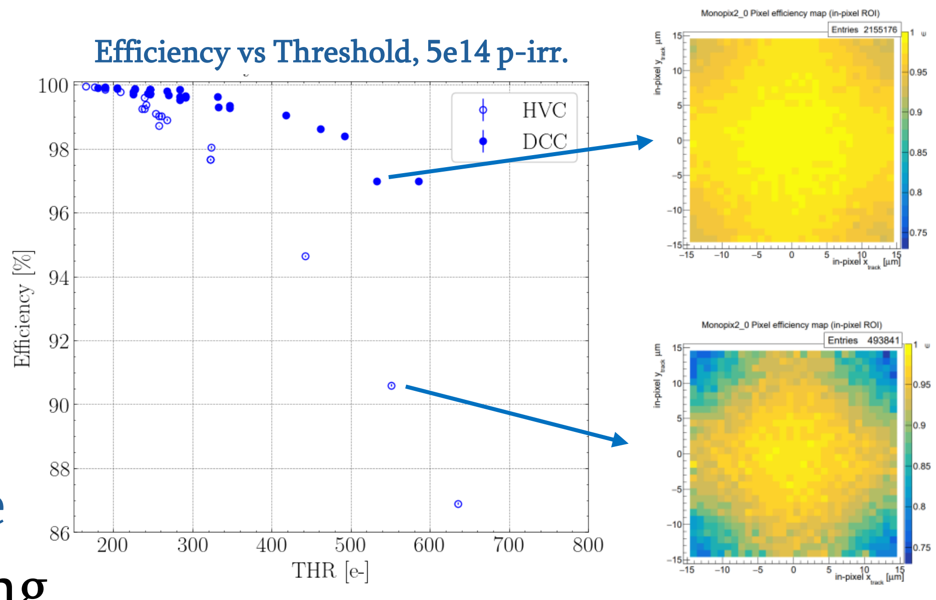
- TJ-Monopix 2 CMOS DMAPS prototype of OBELIX
- Developed for ATLAS ITk in TowerJazz 180 nm process
- Modified process to increase radiation resistance
- Square matrix of 33 μm pixels ($512 \times 512 \Rightarrow 2 \times 2\ cm^2$)
- Column-drain readout, 25 ns timestamping
- R&D chip with **4 front-end flavors**
  - Different biasing mechanisms and coupling (DC, AC) between sensor and amplifier



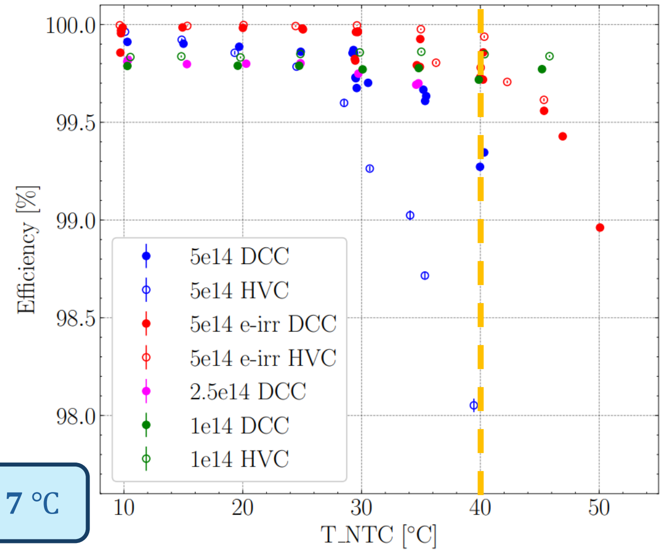
TJ-Monopix 2 testing

- Recent Belle II focus on irradiated sensors (up to NIEL 5×10^{14} 1 MeV n_{eq}/cm^2)
  - ⇒ Study performance at expected integrated fluence
  - ⇒ Needed to choose OBELIX front-end and operating temperature
- Extensively tested in laboratory and with e^- beams
- Results on irradiated sensors :
  - Better performance of **DC-coupled front-end (DCC)** compared to AC-coupled front-end (HVC) ⇒ chosen for OBELIX
  - High detection efficiency (>99%) up to 40 °C ⇒ operating temperature for cooling design

Efficiency vs Threshold, 5e14 p-irr.

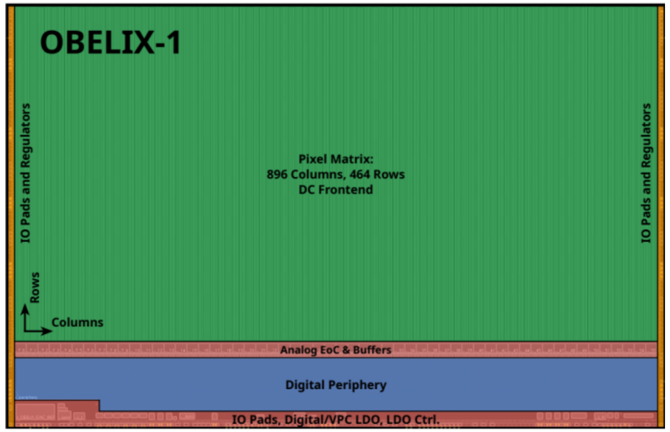


Efficiency vs Temperature, both FEs



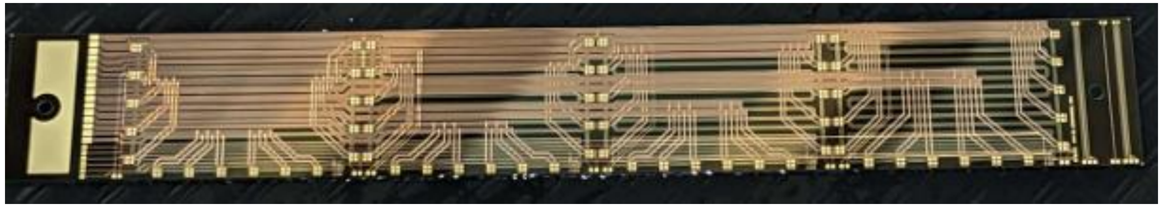
T_Chip ~ T_NTC + 7 °C

OBELIX design

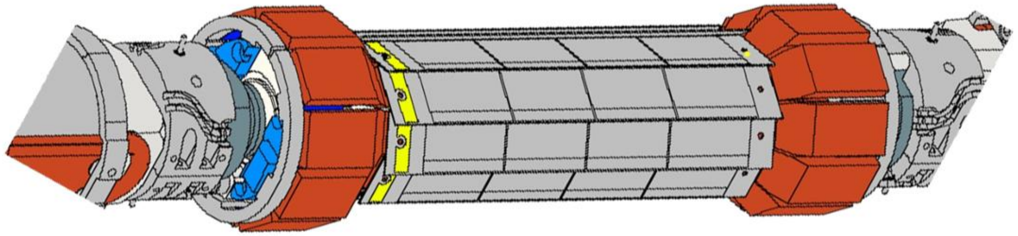


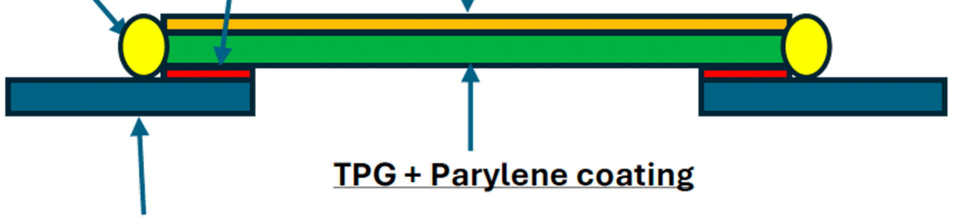
- OBELIX pixel matrix inherited from TJ-Monopix 2 but larger ($464 \times 896 \Rightarrow 2.96 \times 1.53$ cm^2)
- Only DC coupled frontend, 47 ns timestamping
- Column-drain readout with new digital periphery for **triggered operation**:
  - Higher hit rate tolerance (up to 120 MHz/cm^2), 10 μs trigger latency
  - Trigger logic for Belle II
  - Mitigated TJ-Monopix 2 flaws discovered during testing
- Currently under submission ⇒ available from late Summer '26

iVTX design

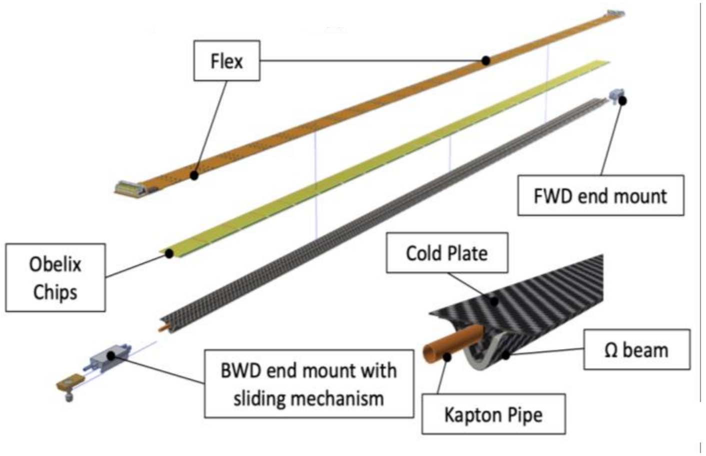


- Silicon ladders:
  - Power and data transfer via **redistribution layer** (RDL) on sensor sensible side
  - RDL done in post-processing phase, under development with in-house process
- Passive cooling with high heat-conductance material (TPG)
  ⇒ radiation hardness confirmed by recent studies
  - Chip power consumption ~300 mW/cm^2 considered for iVTX prototypes
  - Upcoming tests on prototypes

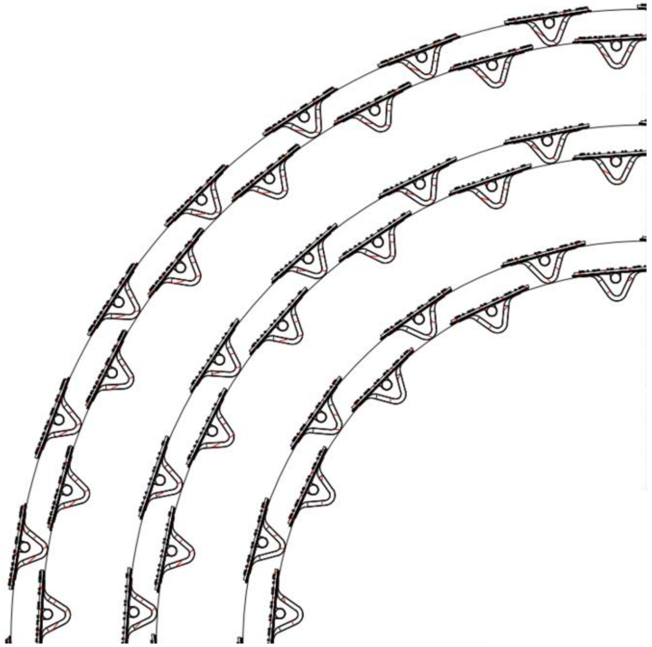




oVTX design



- **Staggered ladders** ⇒ overlap between adjacent ladders
- Ladders inspired by ALICE ITS2 but 4-5× more power consumption
    - Carbon-fiber structure
    - Water cooling ⇒ cold plate
    - OBELIX sensors glued on top of the cold plate
    - Al flex for readout and power distribution
- Great effort to keep material budget <0.8% X/X_0 per layer
- Longest ladder (70 cm) prototype tested
- Still challenges in the integration with other IR elements



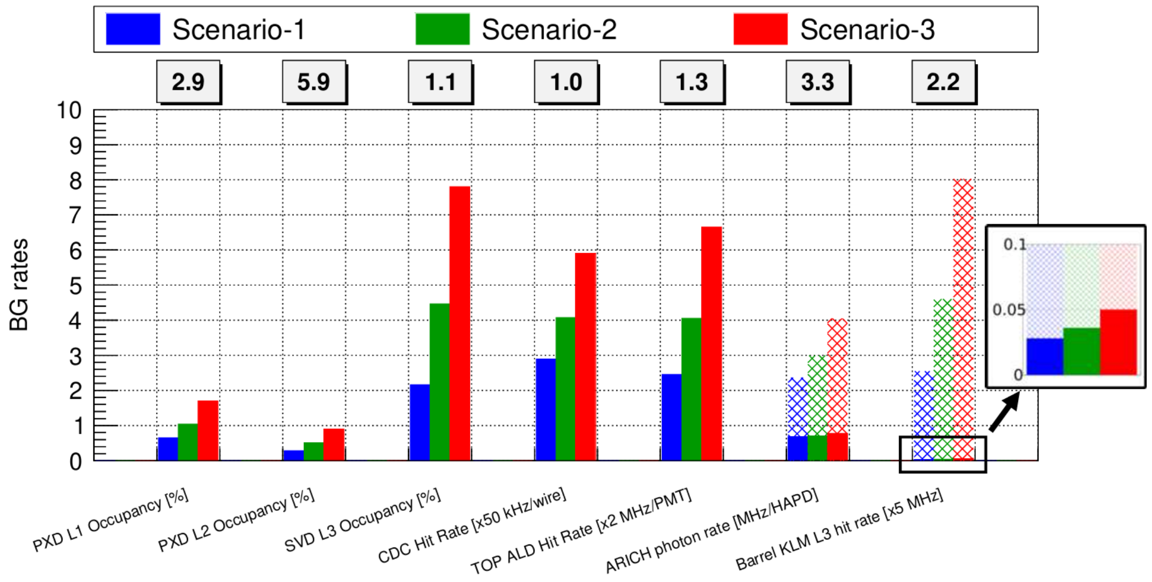
Conclusions

- SuperKEKB upgrade to reach target luminosity $\mathcal{L} = 6 \times 10^{35} cm^{-2} s^{-1}$
  - Redesign of the Interaction Region ⇒ **new VerTeX detector** (VTX)
- Significant space constraints due to new IR design
- Fully pixelated VTX with CMOS DMAPS OBELIX sensor
  - First OBELIX submission ongoing
- 5 layers with different ladder concepts:
  - Inner 2 layers (iVTX): silicon ladders, passive cooling
  - Outer 3 layers (oVTX): ALICE ITS2 inspired ladders, water cooling
- Exciting challenges until 2032!

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

Background

- Background simulation after LS2 difficult due to not-so-easily-simulated evolution
- Three scenarios considered:
  1. Optimistic (× **2**, simple scaling of the background before LS2 to the target beam parameters);
  2. Intermediate (× **5**);
  3. Conservative (× **10**, scaling of an order of magnitude)



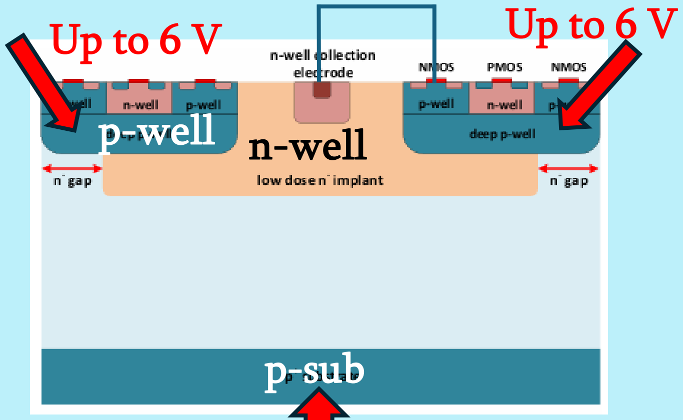
- Many detectors will reach their **maximum allowed occupancy** with scenarios 2 and 3 (SVD, CDC, TOP)

Comparison between front-ends

DC-coupled front-end

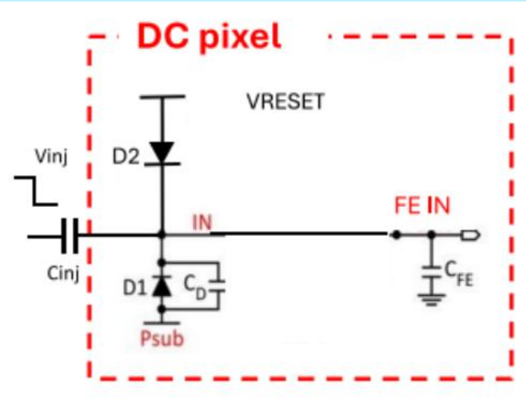
Electrode directly coupled

Biasing:



Non irr.: same as p-well
Irr.: up to 20 V

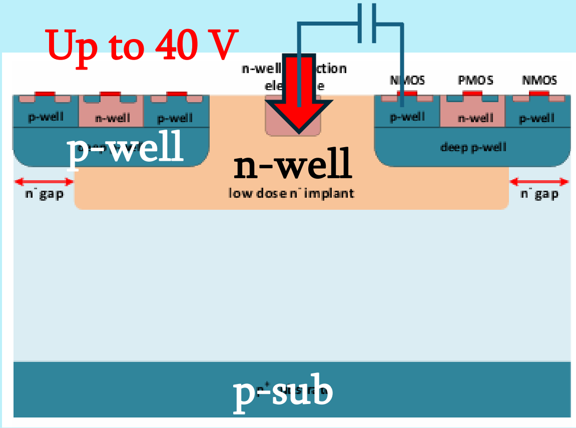
Input circuit:



AC-coupled front-end

Electrode coupled via a capacitor

Biasing:



Input circuit: