Status of FTK & requests 2013

- Old Milestones: we have even more relaxed our schedule
- Status of FTK work
- Money requests for 2013

NEWS & Future steps
- **TDR with tested prototypes June 2013**
- **University of Geneva joined FTK for the LAMB project**
- **LPNHE and University of Tessaloniki show interest**
- **Heidelberg got few funds (25 keuros x 4 years)**

Paola Giannetti, INFN Pisa, for the FTK Group

ATLAS Italia, May 17, 2012

Our intended schedule

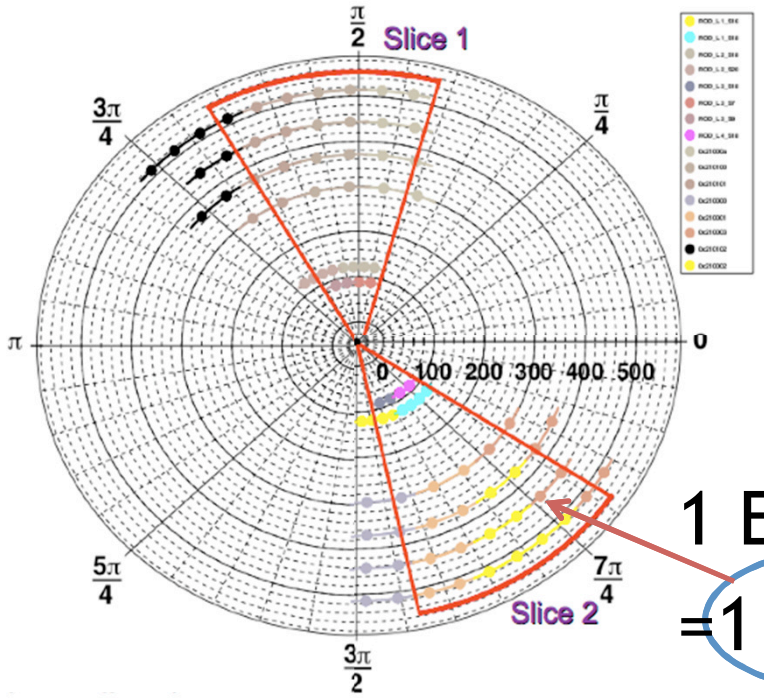
- **Install needed dual-output HOLAs during the upcoming winter shutdown.** DONE
- **Commission in 2012 the FTK vertical slice covering a small η-φ region of the detector.** 2013
- **Have tested prototypes of FTK boards by the end of ~~2012~~ (some delays are possible due to US funding delay and possible need for a second prototype).**
- **Install in 2014 FTK covering the ~~barrel~~** Two 45 degree wedges in the barrel

~~• If the run is extended to 2013, enlarge the vertical slice in 2012 for real triggering → "small demonstrator"~~

- ~~primary vertex identification, beam spot calculation …….~~
- ~~Track-isolated muons, highly ionizing particles …..~~

NO run EXTENSION

45degree phi towers (0.3<η<1.15)



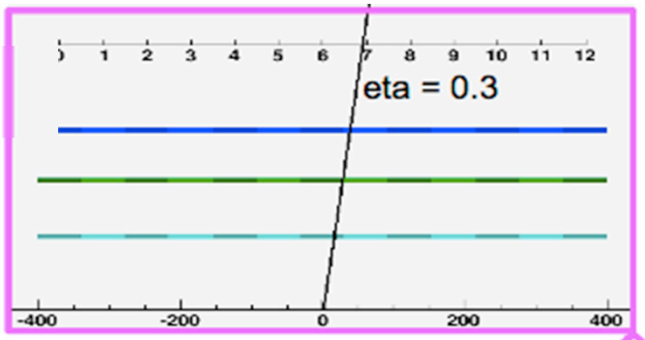
4 pix (L1, L2) + 4 SCT

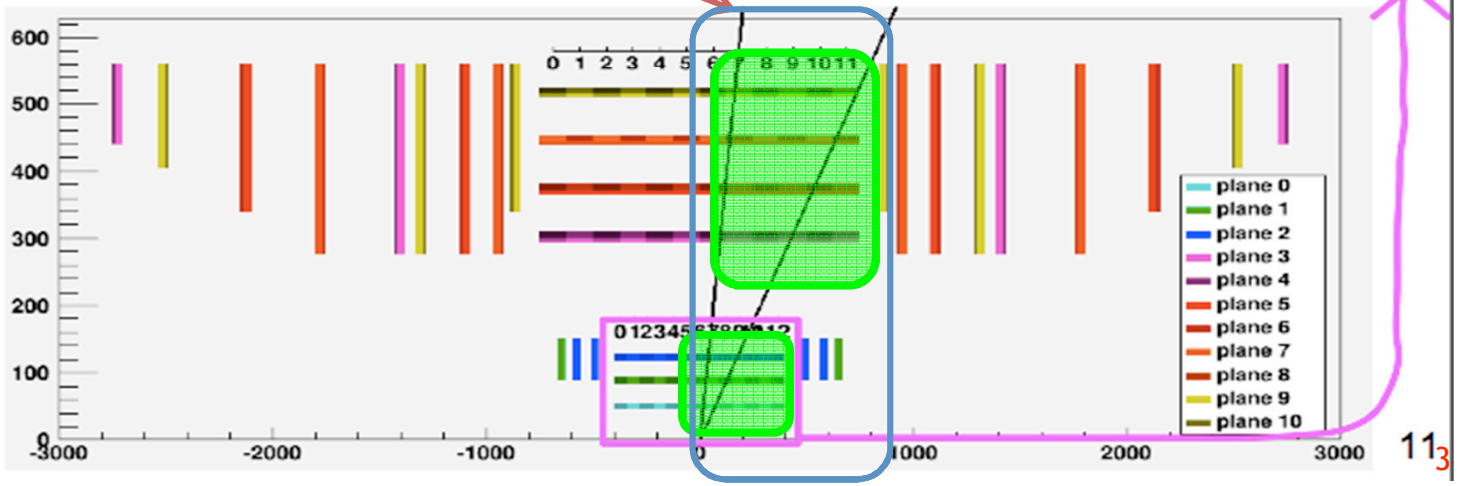
RODs per tower (0.3<η<1.15)

Total 16 ROLs for 2 towers

1 EDRO + 1AMB

=1 tower





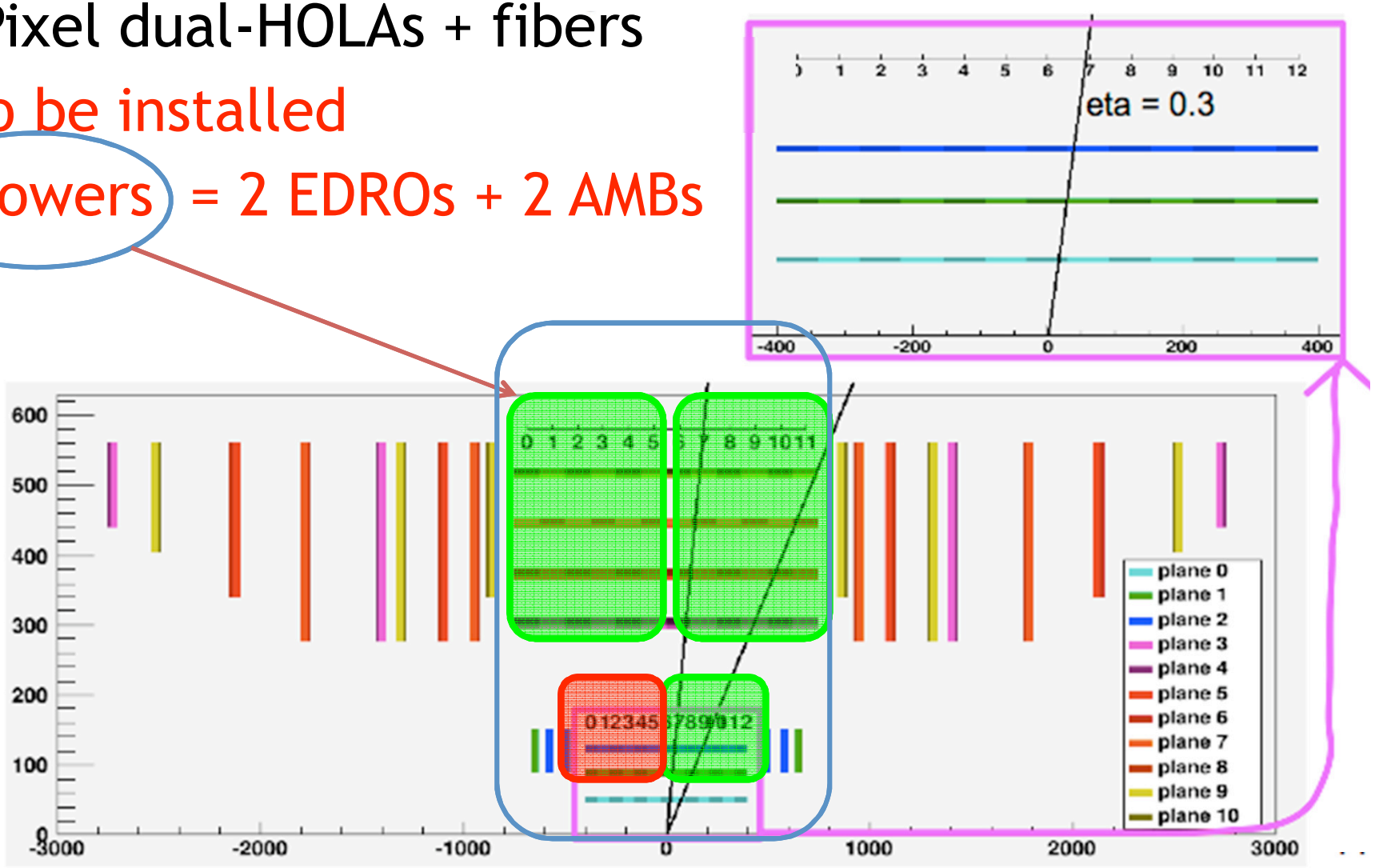
Double Installation of dual-output HOLAs

8 SCT dual-HOLAs + fibers installed

8 Pixel dual-HOLAs + fibers

to be installed

2 towers = 2 EDROs + 2 AMBs



VS idea born for ~5-10 (CDF chip, 6 layers only) – now ~30 !

- Guido study's (November TDAQ): 80% bank ε, ~20

  → no more than ~**10 kHz** event – **a lot of fakes** because 6 layers only

  NO VS study for ~30 but certainly worse!

- Take **only muon triggers** (use L1 ID in the header)
- We will also **prescale** events inside FTK_IM
- We will use banks with **low efficiency** to reduce # found roads
- We will cut the Amboard output at 1000 roads.

  Events will start to be complete only when **< ~20** (later in the store).

  NO TRACK FITTING - ONLY ROAD FINDING!

- Verify integration of FTK prototypes with ATLAS TDAQ
- Verify that real-time FTK output with collision data corresponds to FTK simulation

ANALYSIS of VS data

This task is independent of the hardware task:

If hardware produces the same roads as FTKsim →

can do everything else with FTKsim –

F. Crescioli since February: try to reconstruct top events in VS:

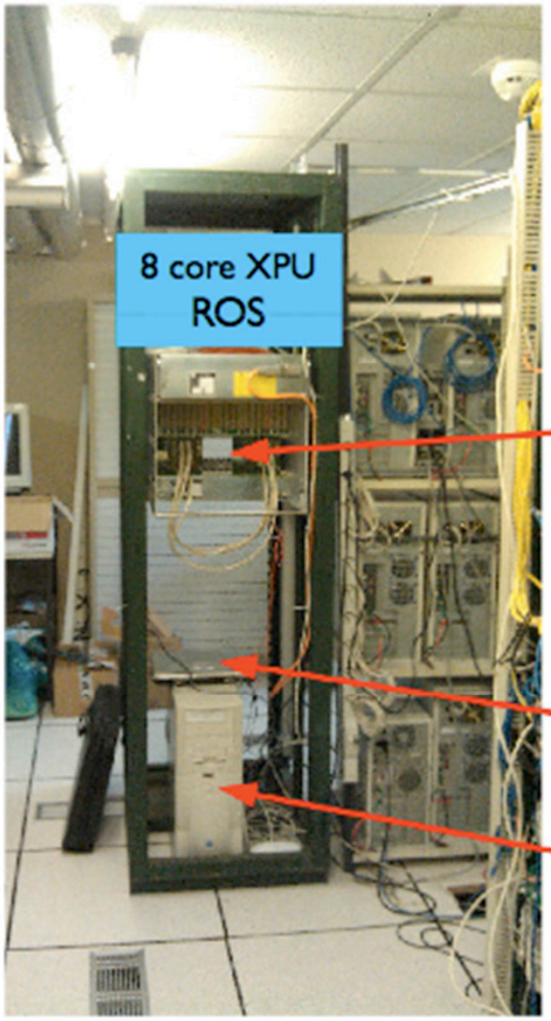
- apply track isolation to leptons
- measure rejection for muons from b-jets
- measure efficiency for muons from Ws

In 3 months: (a) choosing the right strategy to have FTK tracks available to trigger algorithms, (b) learning to run muComb – muIso on them.

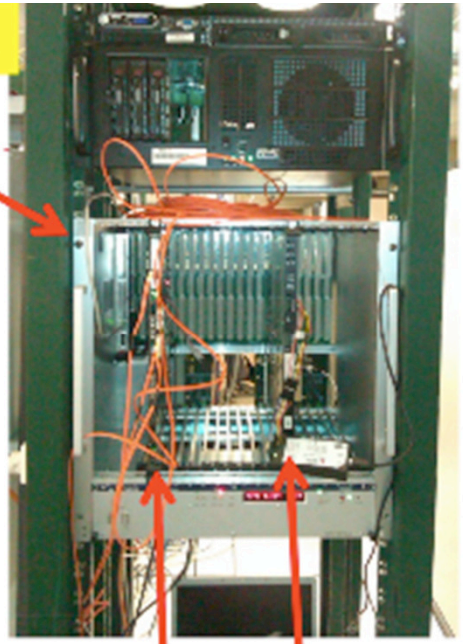
V. Cavaliere and A. McCarn are joining Francesco's effort now. Additional help would be welcomed **from HLT experts**.

Fakes will be a problem – but let's prepare the algos

Vertical Slice Relocation: bldg 32



FRONT OF THE CRATE



Crate with VS boards: it's accessible from the front and the back.

AMBOARD

EDRO
with input Fibers

Laptop with Xilinx programmer

PC with QUEST and FILAR cards

NEW crate @CERN this week for LAB 4

Extra PC + Quest needed

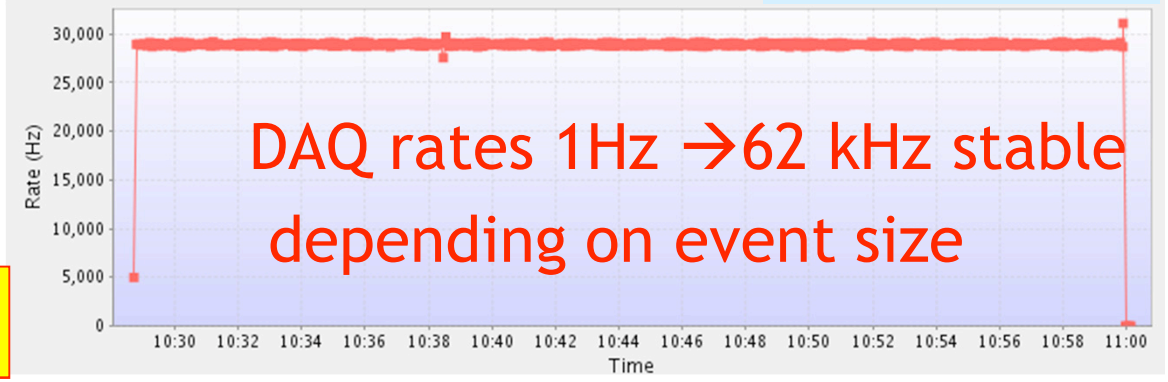
HW Hit generation in EDRO → AM → EDRO → ROS

Test system in Bologna: sample run

HW hit generation to exercise the system at low and high rates

No TDAQ errors

TDAQ Rate



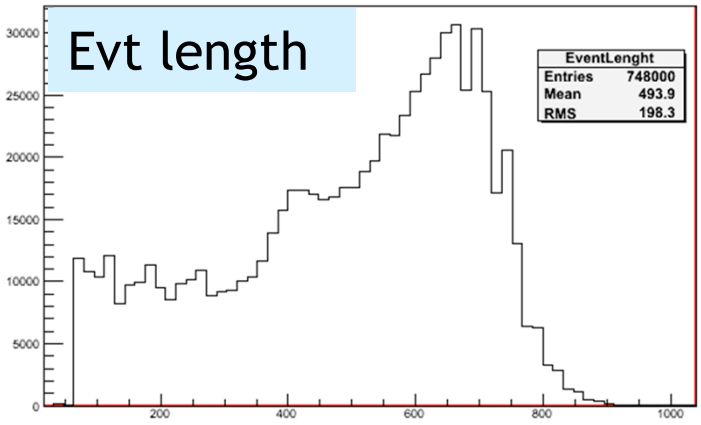
Mean size ≈ 500 words

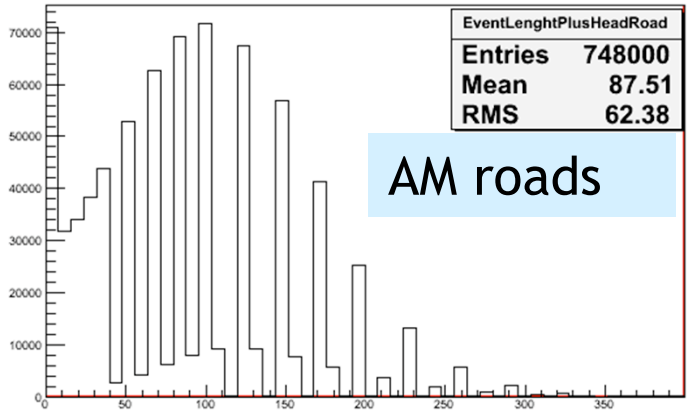
Mean roads ≈ 90

TDAQ rate: 28 kHz

HIGH frequency tests

Online histograms

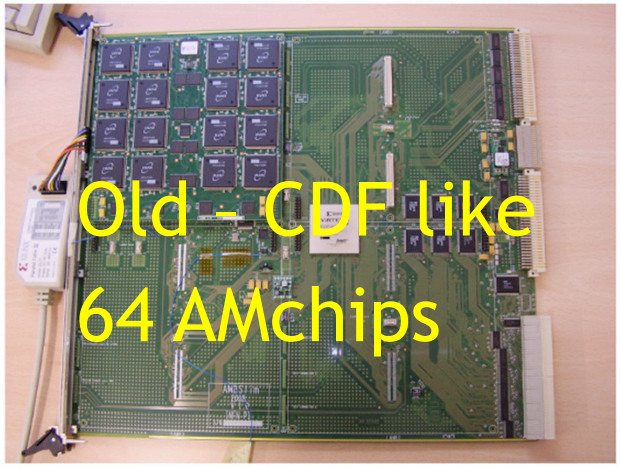




Comparison with offline analysis: on 100k events, 9M HW roads, 99% matched in simulation (missing roads due to event mixing, wrong data transfer or cuts), 0.1% missing End-Events.

AMBoard generations & tests

AMBslim5 for standard test stands



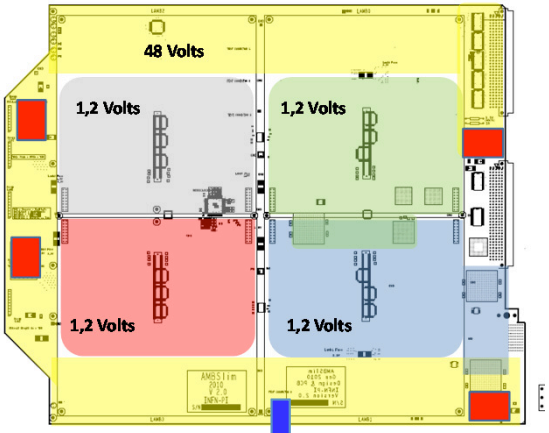
(a)

AMBslim5++ for cooling tests

(b)

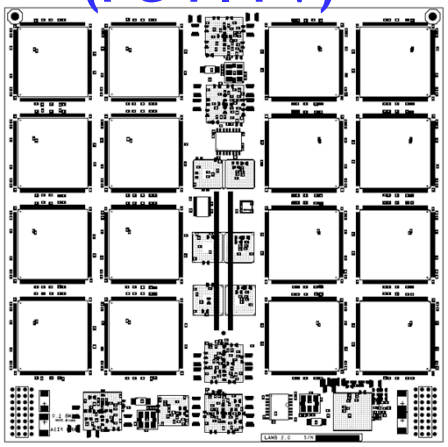
Figure 3: **AM Board** - (a) standard VME VIPA version (b) custom 48V version

NEW:AMBFTK for 2015 (PI-MI)



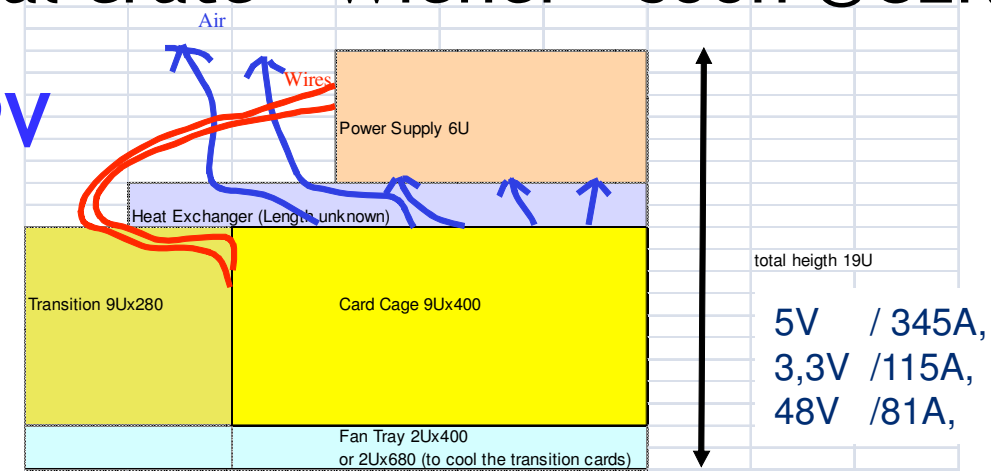
Just ordered the PCB

LAMBFTK just routed (PG-PI-PV)



Final crate - Wiener - soon @CERN

PI-PV



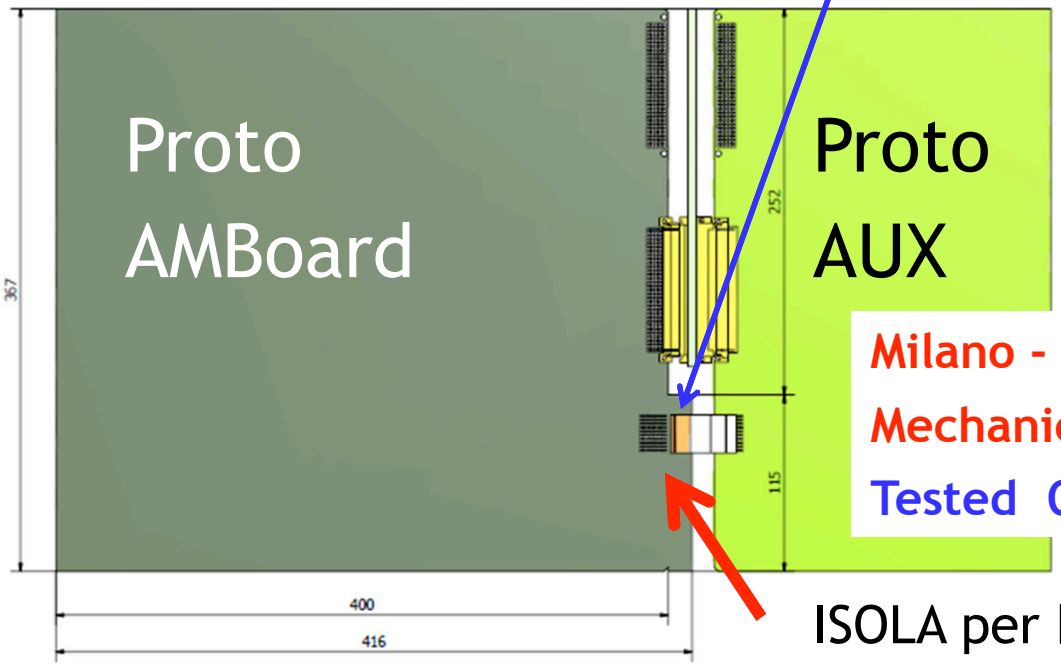
5V / 345A,
3,3V /115A,
48V /81A,

Next tests: AMBFTK and Proto-AUX

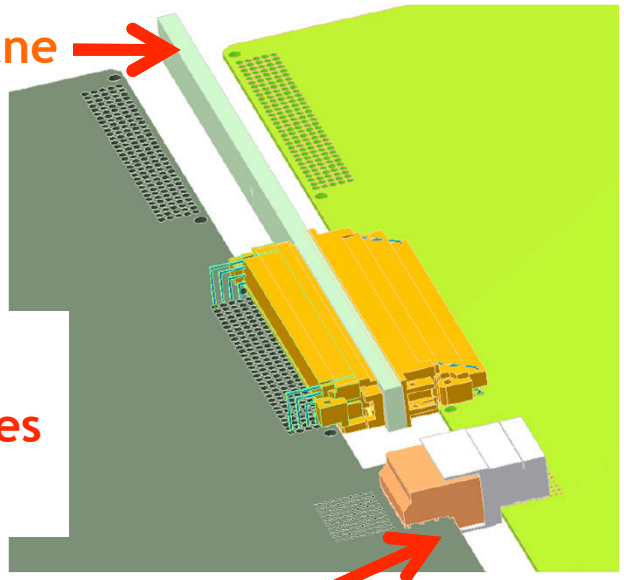
P3: 12 (1.5 GHz)+ 8 (3GHz)
= 20 serial links

A lot of high frequency
Serial links

TEST OF:
- Serial links
- VME on Proto AUX
- Compatibility with new AMchip



Backplane
VME



Milano - Pavia:
Mechanics studies
Tested OK

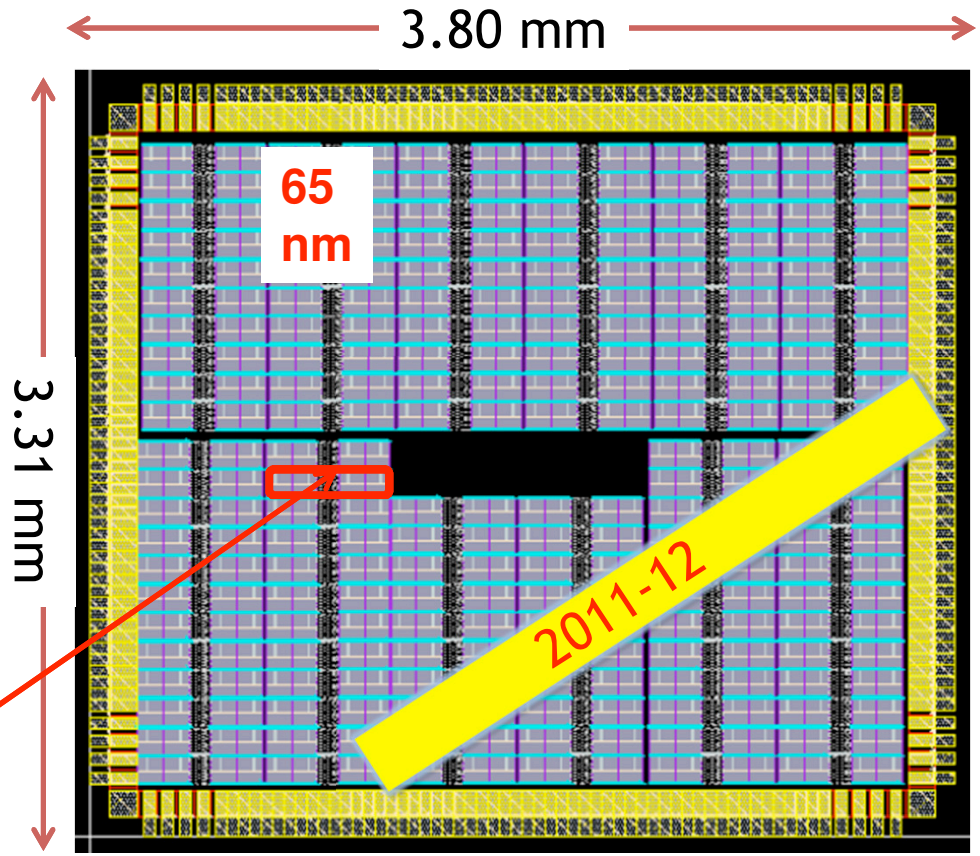
ISOLA per buon contatto P3

AMCHIP04 big Jump in technology! (LNF, Pisa, Milano + ideas from USA)

OLD	NEW	
40	100	MHz
6	8	#input parallel buses
4.3	12	Input BW Gbit/s
1	1	# output bus

Annovi, Beretta, Crescioli,
Liberali, Sacco, Stabile, Hoff

Consumption & perfomances
Measured soon! JUST ARRIVED



14 mm^2 = 8192 Patterns + 228 pads

Variable Resolution: high fake rejection with smaller banks

(Talk G. Volpi Animma 2011)

64 patterns= 2 full custum cells

What for 2015? Small production

If we have to use the small chip (14 mm^2):

2 barrel wedges like VS: 8 AMBFTKs **32** LAMBs **1 k chips**

How much costs 1kchips? 500 chips → **4 wafers, 7,765 k€/wafer**
12 wafer=1500 chips **93 keuro for a 66%** yield??

This is not too expensive for a demonstrator (small & modern)
After this (2015) we can do the pilot run

- 8 AMBoards → 20 keuro
- 32 LAMBs → 20 keuro
- 1,5 kchips → ~90 keuro

} ~ **130 keuro** in 2014

Richieste 2013 – linee guida

- Produzione **rimandata ancora**
- 2012 si costruiscono e testano **pre-prototipi**
- 2013 **prototipi finali e loro tests** (Test stand=CDF Crates to be adjusted)

  20 k€ a Pavia per LAMB finali – Test Stand (TS) VME

  10 k€ a Pisa per AMBFTK finali

  5 k€ a Milano per Test Stand (sviluppo di firmware)

  20 k€ a LNF per FTK_IM finale piccola produzione.
- **chip AM 2013**: IMPORTANTE prepararsi allo step finale costoso
  1. Crescita dell'area per ridurre il rischio step finale **(x10)**
  2. Input/output Serializzati per liberare pads per VCC/GND
  3. Multi-packaging of dies per aumentare la densita'

  → **100 k€** a Milano per crescita chip + **20 k€** a LNF per 2 + **20 k€** **per 3**
- Integration test still based on EDRO in 2013:

  5 k€ a Bologna per 'rewarking' of EDROs e miglioramento test stand

  SUPER TOT **200 k€**

Summary

Milano: 5 k€ TS + AMchip05, 100 k€

Pisa: 10 k€ new AMBFTK

Pavia: 20 k€: LAMBFTK (small prod) + Test stands

LNF: 20 k€ FTK_IM e 20 k€ Amchip

Bologna: 5 k€ (spese di laboratorio)

Tot: 200 keuro

Responsabilita' e ME

• Paola G.	L2	4 mesi
• Marco P.	L2	4 mesi
• Agostino L.	L2	1 mese
• Andrea N.	L2	1,5 mesi
• Annovi A.	L2	4 mesi
• Volpi G.	L3	2 mesi
• Mauro V.	L3	3 mesi
• A. Stabile	L3	1 mese
• Valentino L.	L3	1 mese

Responsabilita' descritte a questa pagina:
https://twiki.cern.ch/twiki/bin/viewauth/Atlas/FastTracKer

Integrazione di FTK con prototipi americani @CERN:

Pisa	1 mesi
Milano	1 mesi
Frascati	1 mesi
Pavia	1 mesi
Bologna	1 mesi

Missioni interne

4 K€	Frascati	integrazione prototipi e AMchip I e II
5 K€	Pisa	integrazione prototipi
4 K€	Milano	AMchip I e II
4 K€	Pavia	integrazione prototipi
	Bologna	integrazione prototipi

Conclusions

- We are working hard for both the Final FTK
  & the intermediate versions (vertical slice and demonstrator)
- First prototypes (chip and boards) will be under tests in June.
- the AMchip just arrived, as planned.
- the vertical slice plan has been reduced (LHC schedule).
- the TDR in 2013 should start final approvals
- A demonstrator expected in 2015, production will start after.

Backup

Other US board designs

- **The other US responsibilities (2nd-stage board at Illinois, Data Formatter at Fermilab, FTK output board at Argonne) have been impacted by the delay of FY11 engineering funds.**
- **The groups are working on board specifications and have assembled test stands, but real engineering design awaits the receipt of funds, hopefully soon.**
- **They are also using this time to see if it makes sense to switch from VME to ATCA for the FTK input (DF) crates and output crate.**

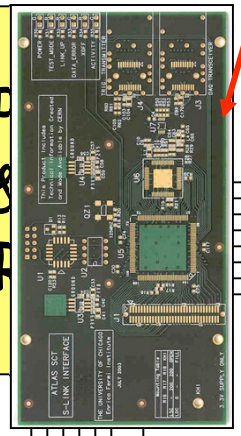
FTK: Projects to Institutions

Frascati-Waseda: Clustering in Pixels-SCT mezznines

Pisa & Frascati & Fermilab the AMChip could be 3D

USA-Italy "2-outHola"

Pisa: AMBoard



4 DF crates: cluster finding split by layer

8 "core" crates: AMboard Data Organizer GigaFitter

Illinois: Final board in core crate

Fermilab: DF motherboards

S-links

1 Readout Crate

Argonne

Raw data ROBs

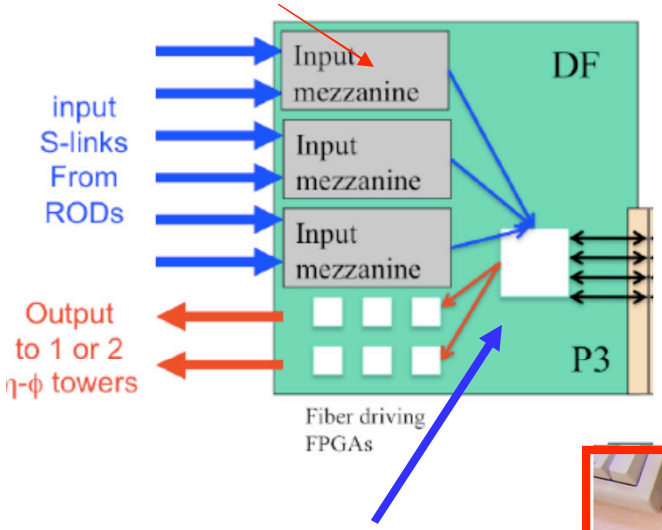
Chicago GigaFitter + Data Organizer + HW

Track data ROB

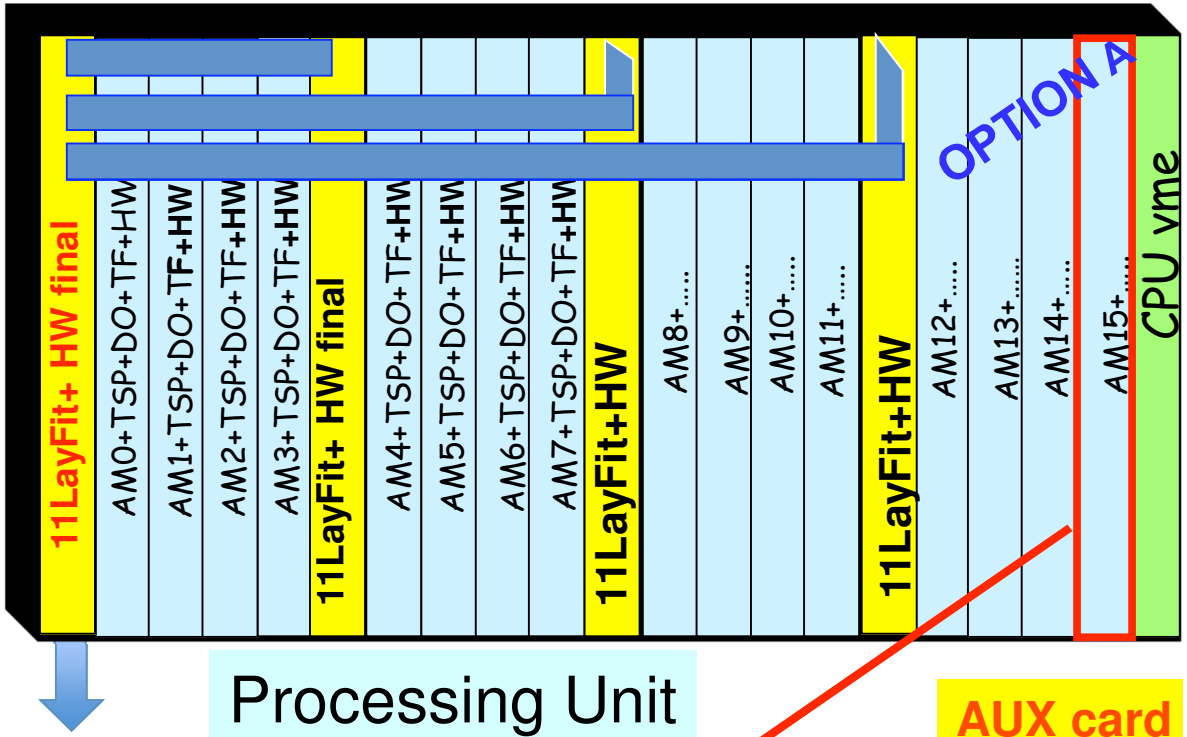
USA+Italy: crates + links + backplanes…

ITALIAN DUTIES for 3x10**34

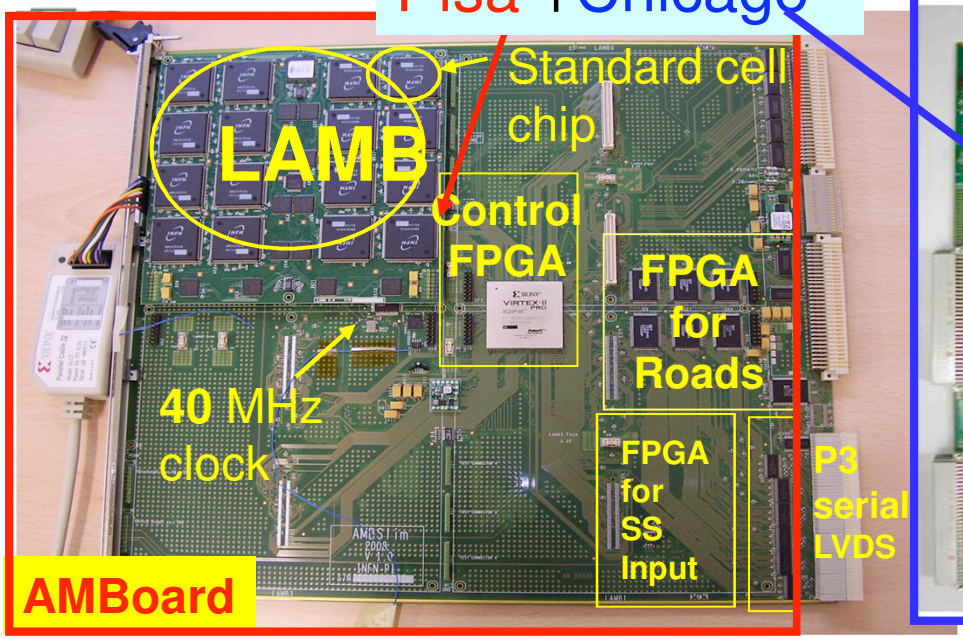
DATA FORMATTER FRASCATI



FERMILAB



Processing Unit Pisa +Chicago



AUX card