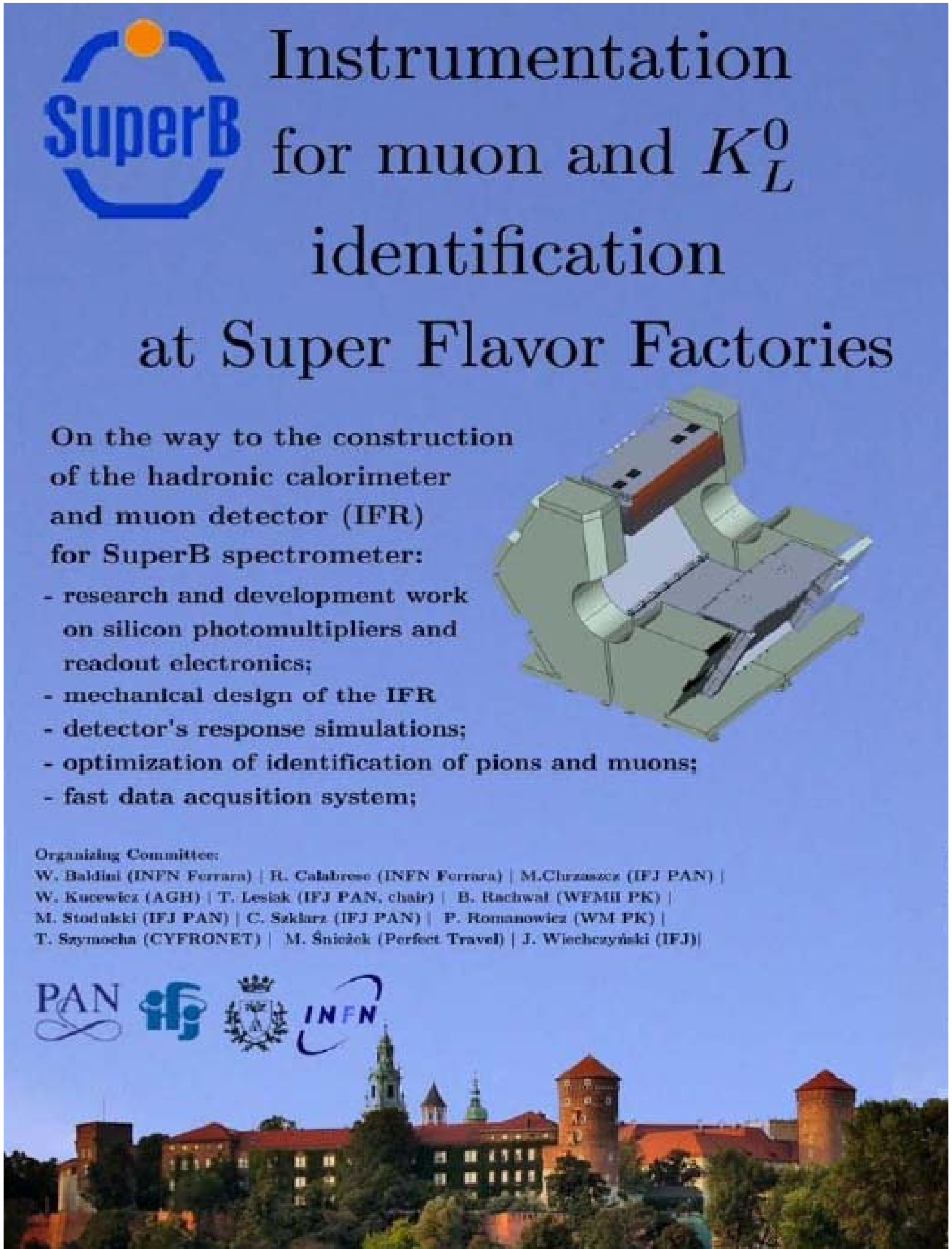


SuperB IFR electronics: an overview

Angelo Cotta Ramusino

on behalf of the IFR collaboration

Invitation to the „IFR workshop in Krakow”

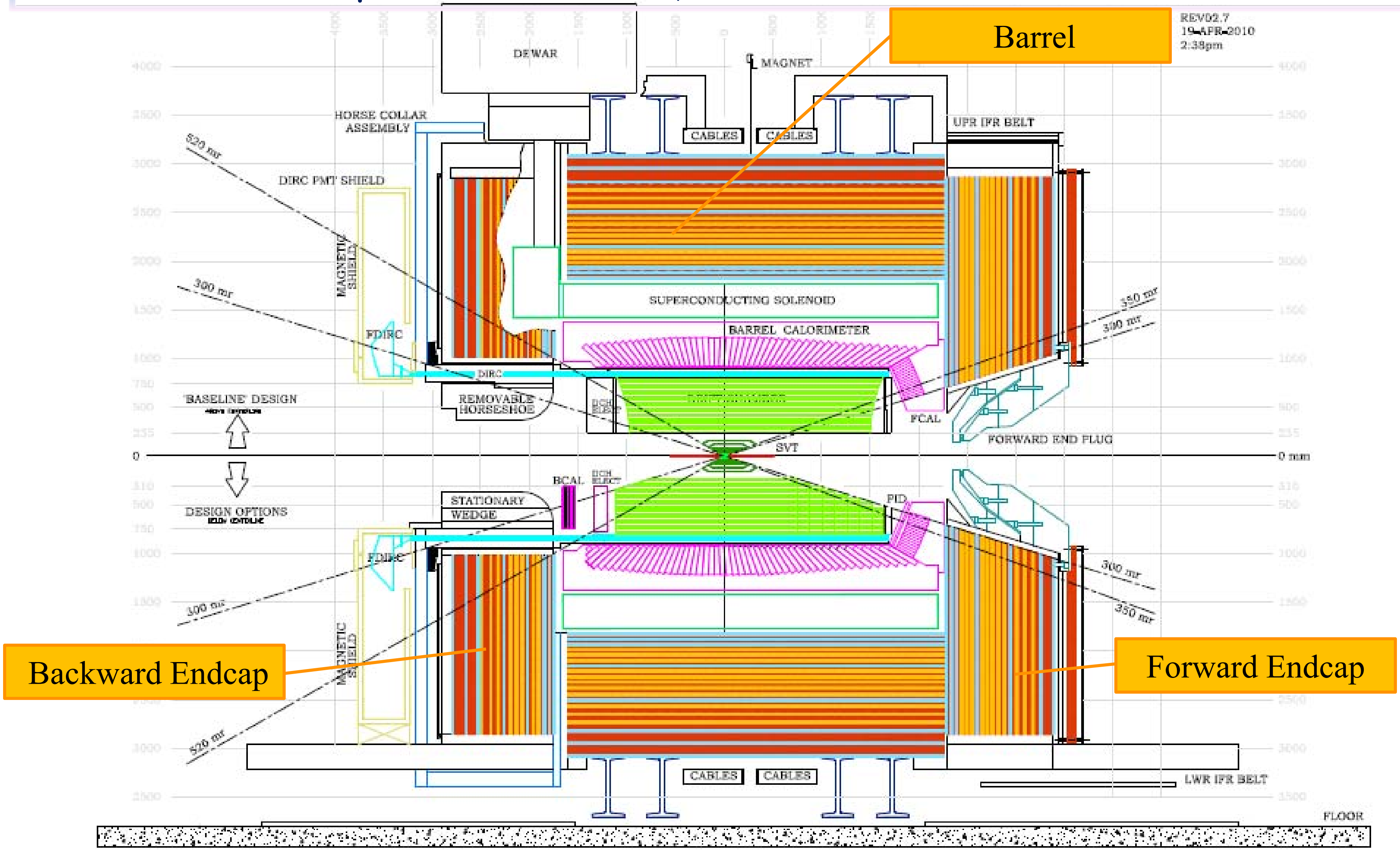
First of all I wish to thank the Krakow group for giving us the privilege to work with them and, on top, in this wonderful town too.

SUMMARY:

- IFR basics
- IFR electronics overview (TDR baseline)
- Topics to be covered in the "electronics" parallel sessions of this workshop

IFR basics

The SuperB detector (from: "SuperB Detector Status-Elba-2012", Blair Ratcliff, SLAC)



from: "The IFR detector at SuperB", JAROSŁAW WIECHCZYŃSKI, Institute of Nuclear Physics PAS, 11.01.2012

What is the IFR for...

Physical purposes:

- Muon identification
- Identification (along with the electromagnetic calorimeter) of the neutral hadrons – mostly K^0_L's

- Good separation between penetrating particles (muons) and charged hadrons is crucial for extracting signal of several important *B* decays like:

$$b \to s\, l^+ l^- \qquad B \to \mu\nu_\mu$$
$$b \to d\, l^+ l^- \qquad B \to \tau\nu_\tau$$
$$B \to \mu^+\mu^-$$

- identification of the neutral particles allows for background suppression (veto) in reconstruction of final states with missing energy (especially those with neutrinos) from: "The IFR detector at SuperB", JAROSŁAW WIECHCZYŃSKI, Institute of Nuclear Physics PAS, 11.01.2012

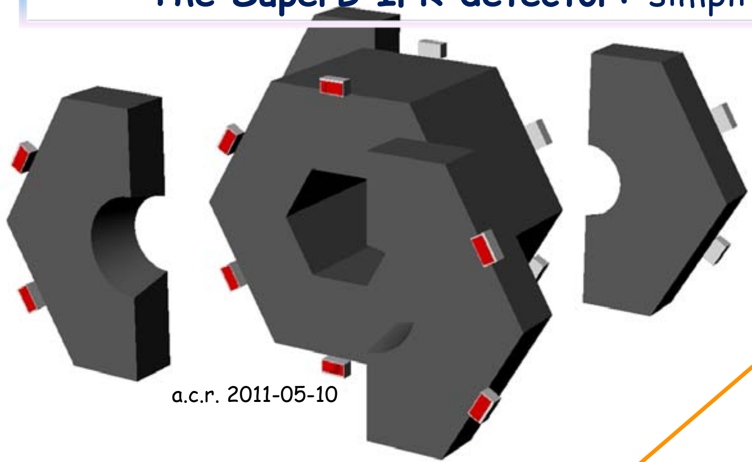
IFR Institutions

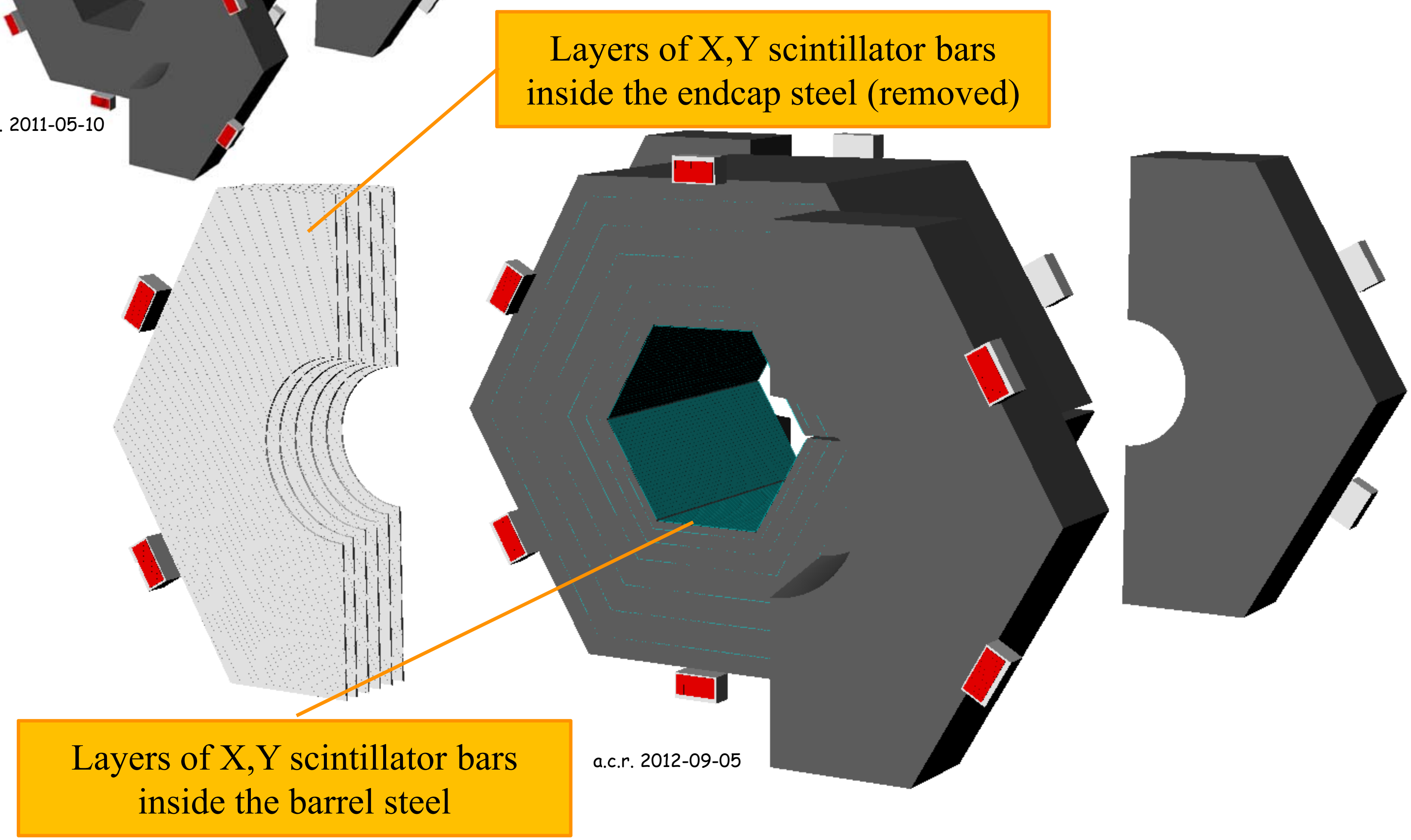
- INFN, Sezione di Bologna
- INFN, Sezione di Ferrara
- INFN, Sezione di Padova
- INFN, Sezione di Torino

Krakow:

- Institute of Nuclear Physics PAS (software; prototype data analysis)
- AGH University of Science and Technology, Faculty of Electrical Engineering, Automatics, Computer Science and Electronics (studies of SiPM front-end electronics, readout and data acquisition system)
- the Cracow University of Technology, Faculty of Mechanical Engineering (numerical calculations, using Finite Element Method, supporting the design and construction process)

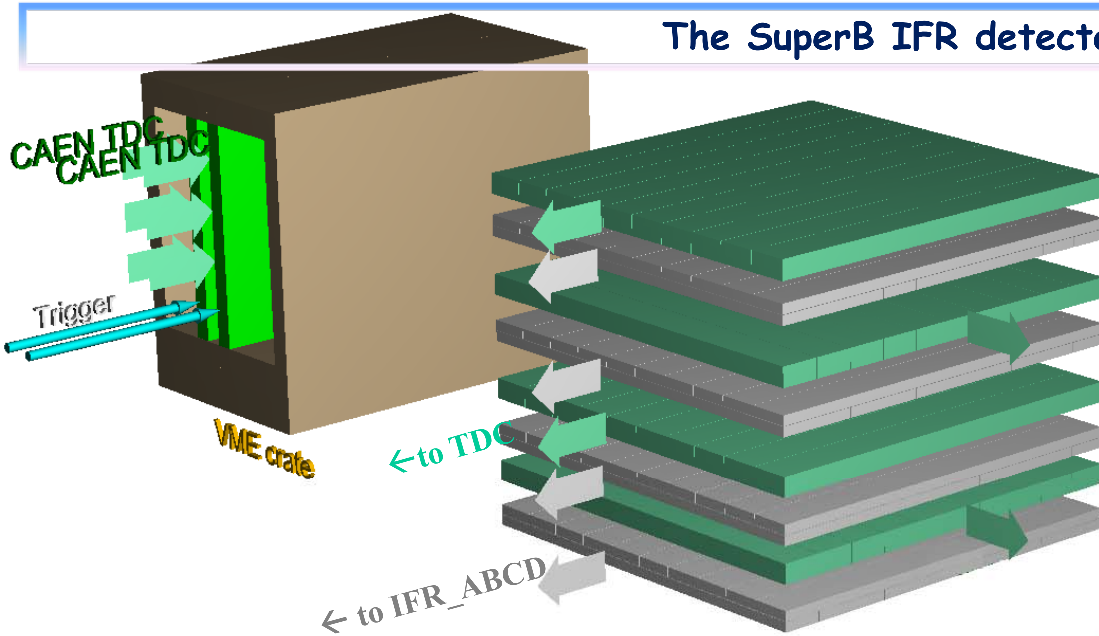
The SuperB IFR detector: simplified view of the IFR and partial view of the detector elements

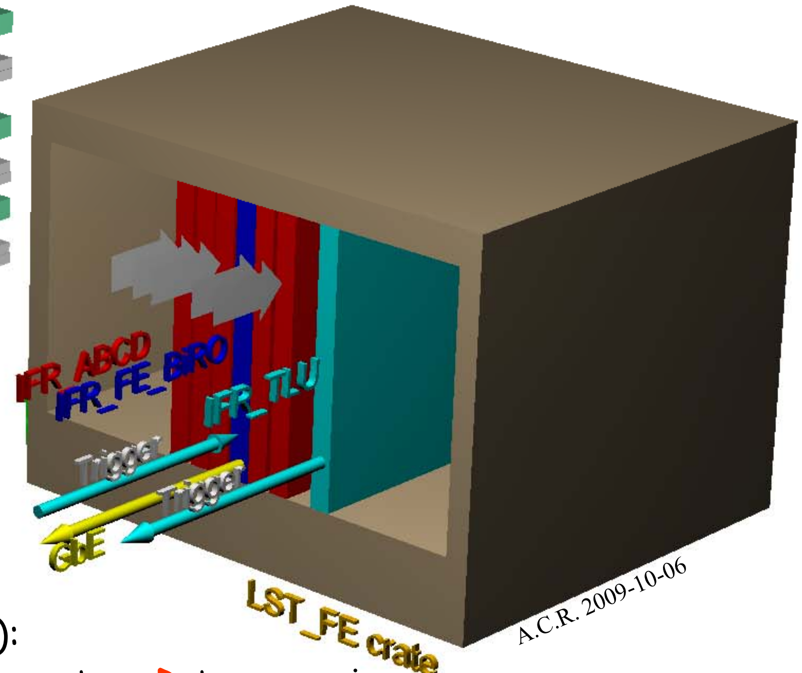




The SuperB IFR detector prototype

the concept....



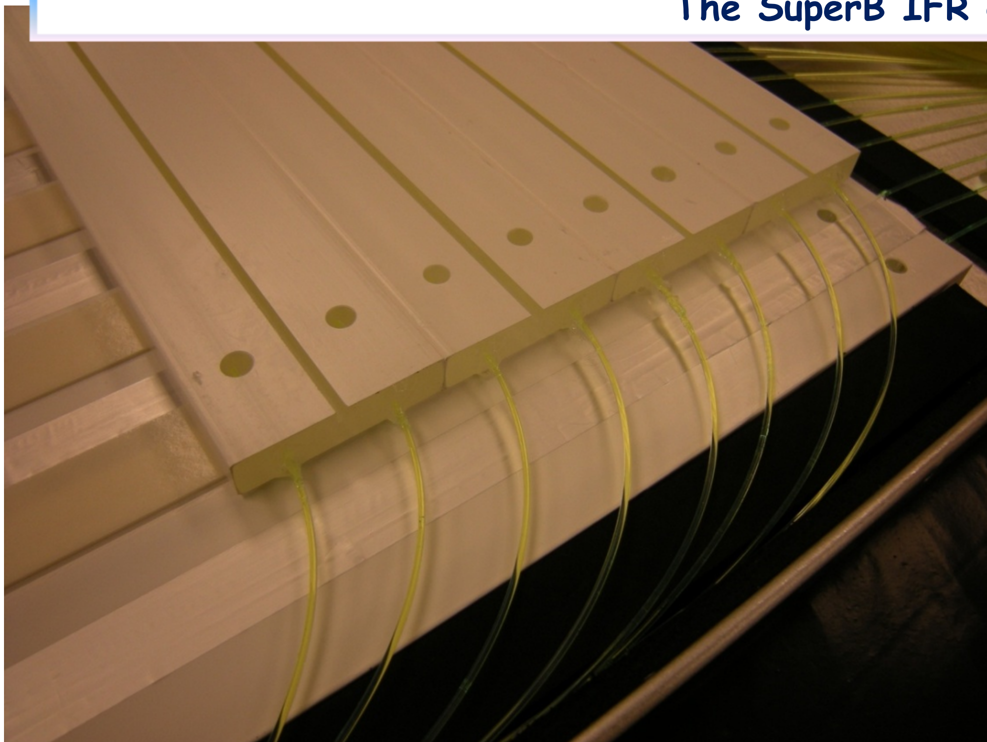


SuperB IFR prototype:
- 4 layers of x-y scintillators, 1 cm thick, read in binary mode
- 4 layers of scintillators 2 cm thick, read in timing mode

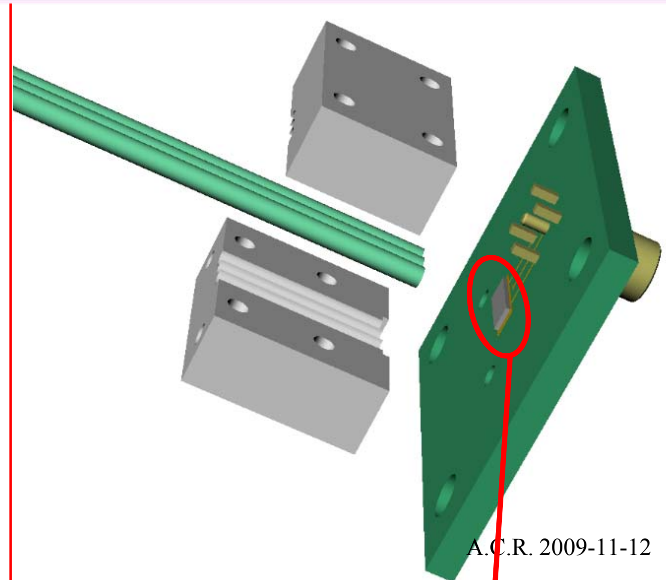
SuperB-IFR prototype readout electronics (baseline):
- "IFR_ABCD": sensor Amplification, Bias-conditioning, Comparators, Data processing: it samples the level of the comparators outputs @ >= 80MHz and stores it, pending the trigger request
- "CAEN_TDC": a multi-hit TDC design based on CERN HP-TDC; hosted in a VME crate and read out via a VME CPU or via a VME-PCI bridge to the DAQ PC
- "IFR_FE_BiRO": collects data from IFR_ABCD cards upon trigger request and sends it to DAQ PC (via GbE)
- "IFR_TLU": a module (Trigger Logic Unit) to generate a fixed latency trigger based on primitives from the IFR prototype itself or from external sources

IFR_FE_BiRO + IFR_TLU are now a single module

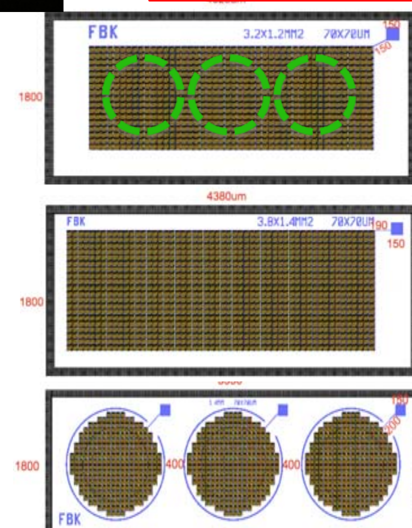
The SuperB IFR detector prototype



SuperB IFR : the scintillating bars are equipped with wavelength shifting fibers (3 for each bar in the prototype), which are then coupled to a SiPM device by means of precisely machined plastic supports.



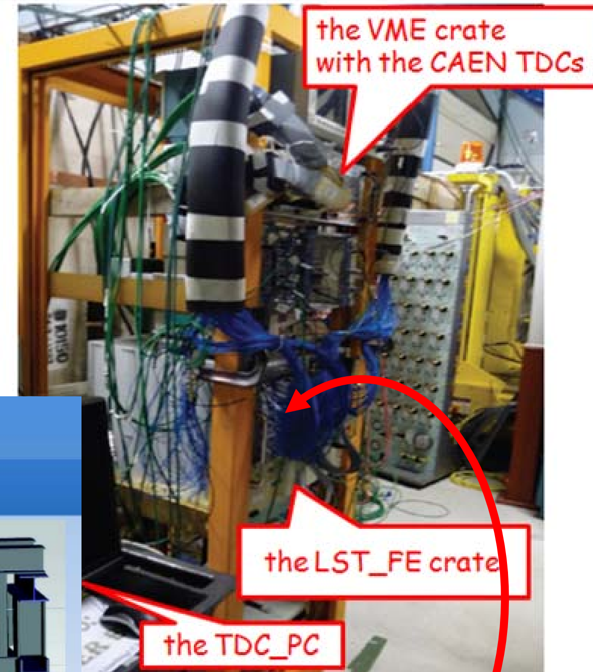
pictures/drawing from the prototype construction



SiPM by FBK, Trento. 70x70um^2 cell size, n-on-p.

Bonding of the SiPM to the carrier PCB was performed at INFN Perugia thanks to G. Ambrosi, M. Ionica

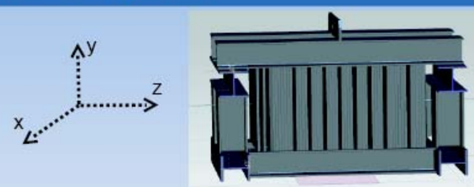
The SuperB IFR detector prototype

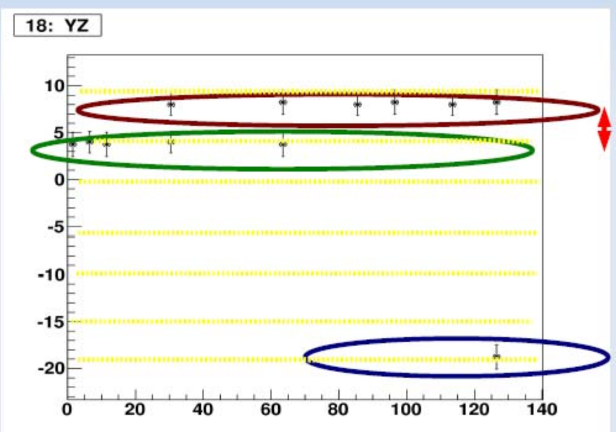


Prototype data analysis

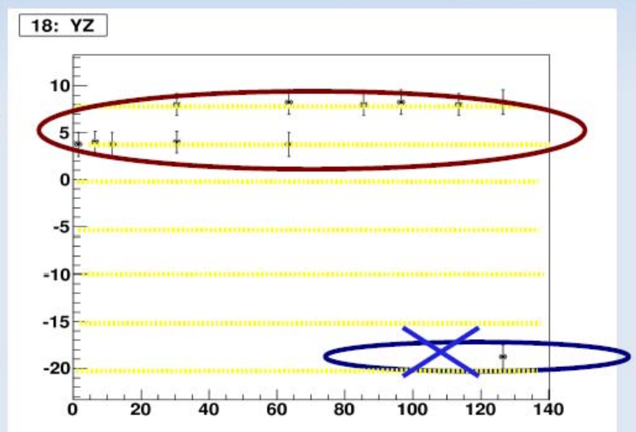
(J.Wiechczyński)

- Clusterizing algorithm
  → rejection of the background hits

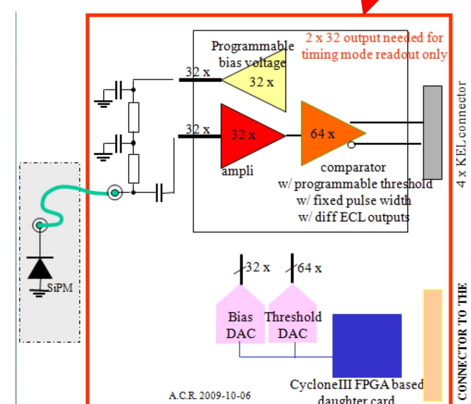




biggest cluster – good muon track



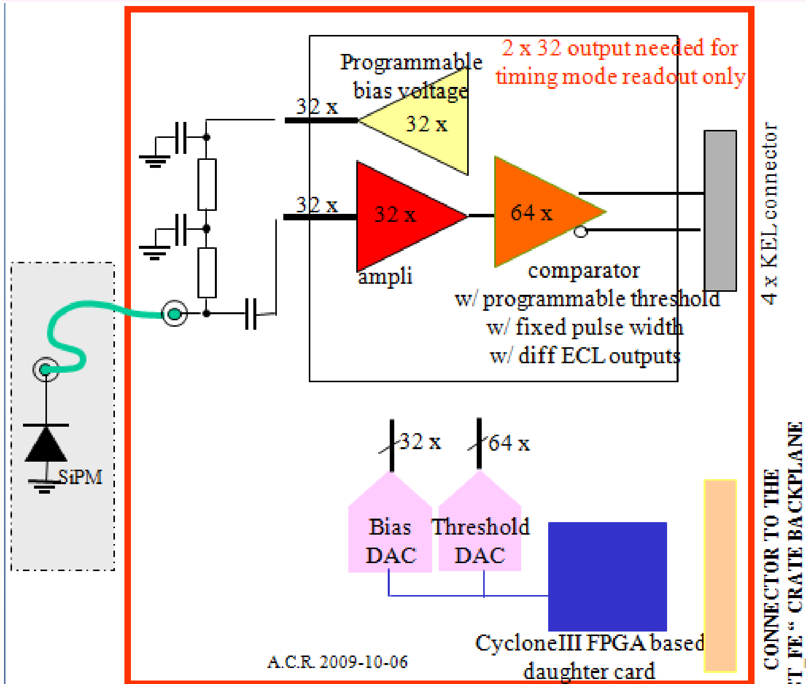
adjacent clusters merged if close enough



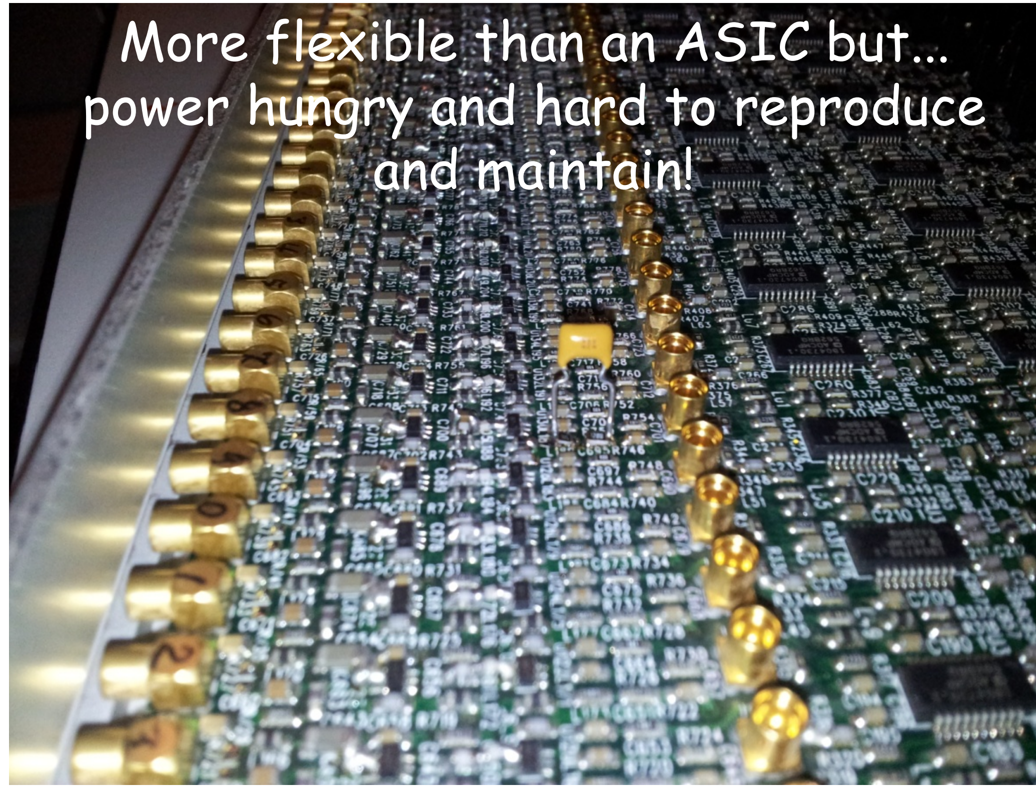
"IFR_ABCD" card (Amplifier, Bias, Comparator, DataProcessing)

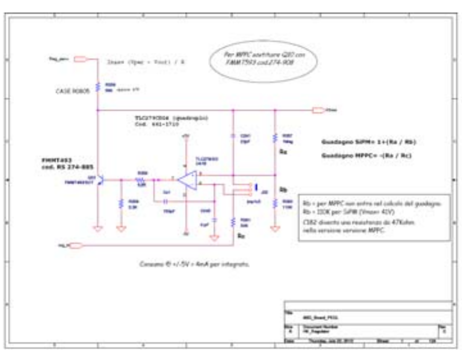
GOTO: "ABCD" description

The SuperB IFR detector prototype

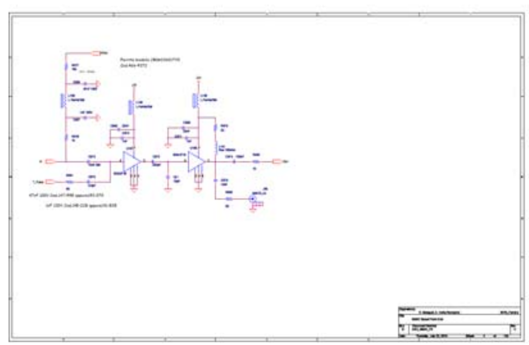


"IFR_ABCD" card (Amplifier, Bias, Comparator DataProcessing)

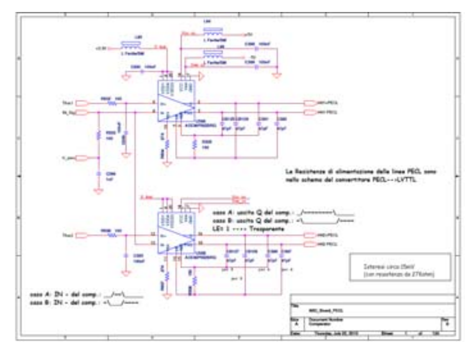




GOTO: bias generator schematic



GOTO: amplifier schematic



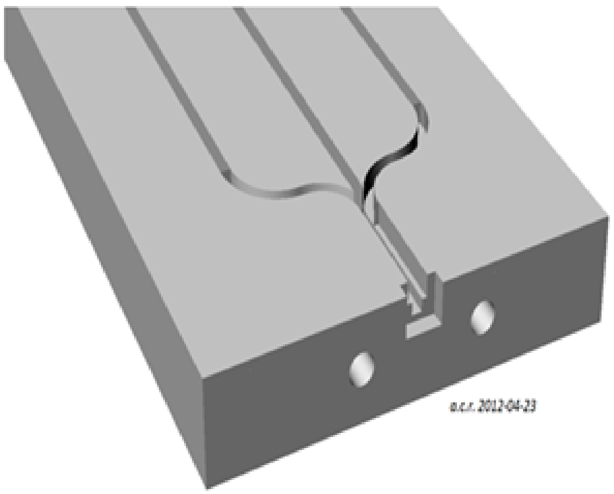
GOTO: comparator schematic

IFR electronics overview (TDR baseline)

• details of the detector elements

The IFR will exploit extruded plastic scintillators to detect ionizing radiation crossing the apparatus. The light from the scintillator is collected and converted by wavelength shifting (WLS) fibers and guided to the SiPM.

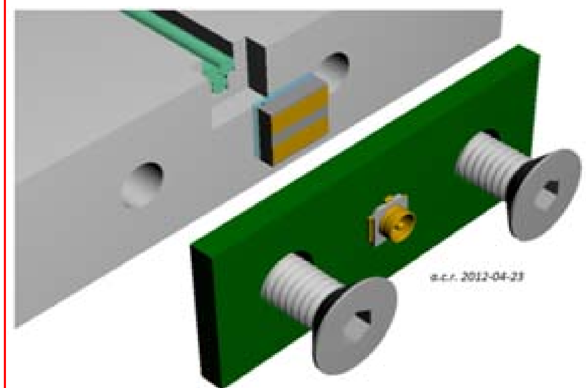
Three WLS fibers should be installed in each scintillator bar.



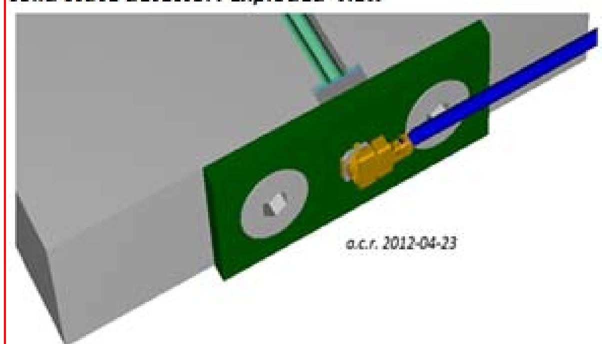
a scintillator bar machined to host three WLS fibers, the silicon photomultiplier and the carrier printed circuit board (PCB)

Only one end of a scintillator bar is equipped with a SiPM.

A printed circuit board (PCB) will be designed to support the photodetector and the miniature connector to a small diameter coaxial cable.

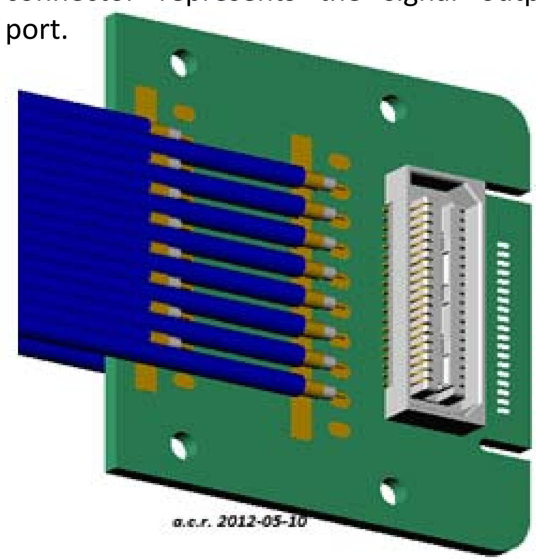


details of the three WLS fibers and the PCB for the solid state detector: exploded view



details of the three WLS fibers and the PCB for the solid state detector

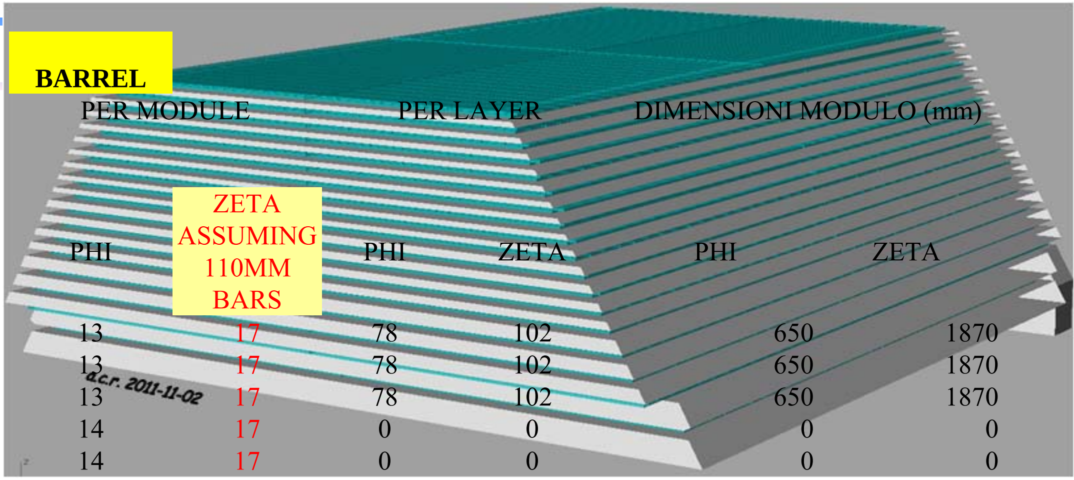
The other ends of the minicoax cables are soldered onto a **“mass termination” PCB.** The light tigh enclosure containing the scintillator bars must be machined to provide an output port for the bundle of minicoax cable. A more elegant but more expensive solution would be to install the “mass termination PCB” inside the enclosure so that the high performance connector represents the signal output port.



detail of the multi coaxial connector assembly

IFR electronics overview (TDR baseline)

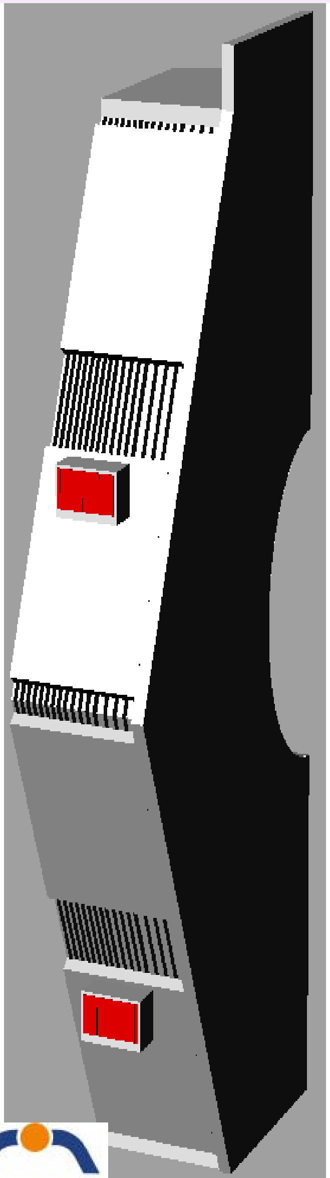
- numerology

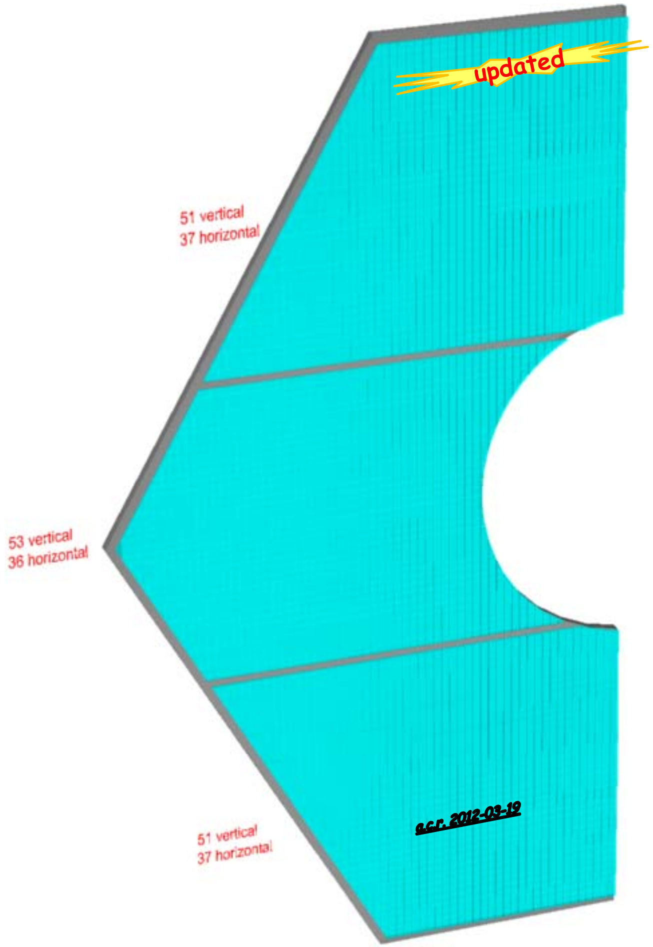


BARREL

LAYER WIDTH	LAYER	No.Modules per layer	LAYER ENABLE	PER MODULE PHI	PER MODULE ZETA ASSUMING 110MM BARS	PER LAYER PHI	PER LAYER ZETA	DIMENSIONI MODULO (mm) PHI	DIMENSIONI MODULO (mm) ZETA
1963	1	6	1	13	17	78	102	650	1870
1987	2	6	1	13	17	78	102	650	1870
2050	3	6	1	13	17	78	102	650	1870
2113	4	6		14	17	0	0	0	0
2176	5	6		14	17	0	0	0	0
2240	6	6	1	14	17	84	102	700	1870
2304	7	6		15	17	0	0	0	0
2367	8	6		15	17	0	0	0	0
2431	9	6		16	17	0	0	0	0
2494	10	8	1	12	17	96	136	600	1870
2569	11	8		12	17	0	0	0	0
2641	12	8		13	17	0	0	0	0
2712	13	8	1	13	17	104	136	650	1870
2784	14	8		13	17	0	0	0	0
2879	15	8	1	14	17	112	136	700	1870
2973	16	8		14	17	0	0	0	0
3068	17	8		15	17	0	0	0	0
3144	18	8	1	15	16	120	128	750	1870
3296	19	8	1	16	16	128	128	800	1870
NUMBER OF MODULES per sextant:	64			TOTAL PER SEXTANT	1950	878	1072		
TOTAL NUMBER OF MODULES	**384**			**TOTAL CHANNELS PER BARREL**	**11700**	5268	6432		

- numerology



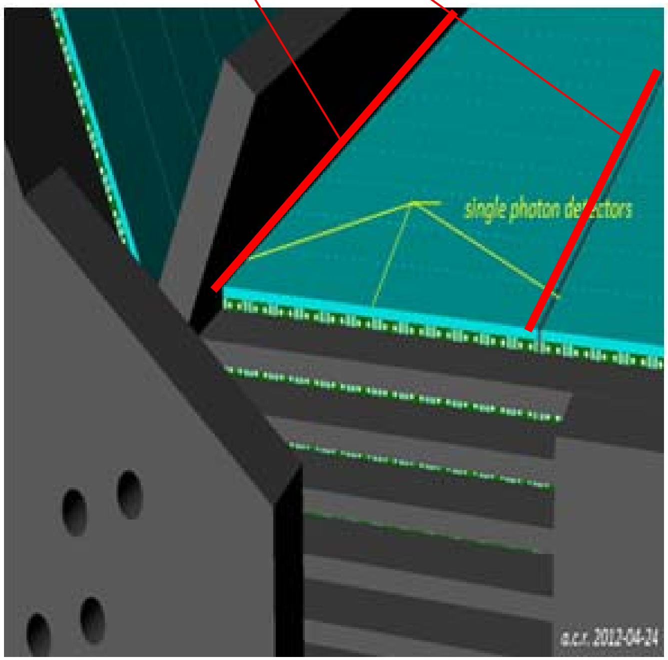


ENDCAP		
top section	horizontal bars per module:	37
	vertical bars per module:	51
center section	horizontal bars per module:	36
	vertical bars per module:	53
bottom section	horizontal bars per module:	37
	vertical bars per module:	51
AVERAGE channel count per module:		88,4
NO_OF_MOD_PER_LAYER_EC:		**3**
horizontal bars per layer		110
vertical bars per layer		155
NUMBER OF LAYER PER DOOR		9
NUMBER OF DOORS IN ENDCAPS		4
TOTAL NUMBER OF MODULES IN ENDCAPS: (+50%)		**108**
horizontal bars per door:		990
vertical bars per door:		1395
TOTAL HORIZONTAL BARS:		3960
TOTAL VERTICAL BARS:		5580
TOTAL CHANNELS IN ENDCAPS: (+12.3%)		**9540**

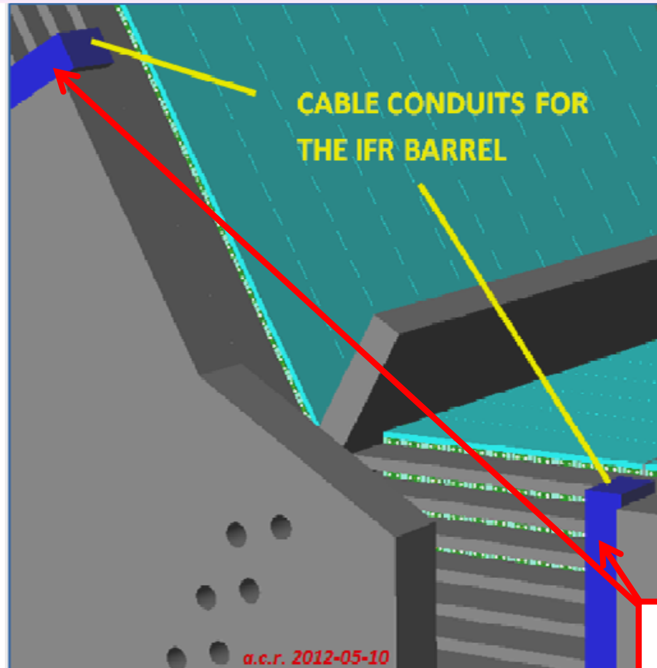
IFR electronics overview (TDR baseline)

- details of detector installation: the barrel case

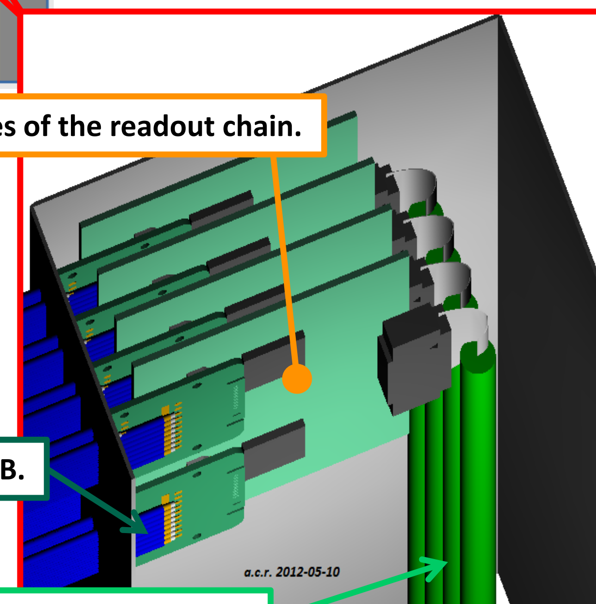
SiPMs applied to the elements of the Z array are distributed all along these edges. An alternative would have been to concentrate the SiPMs at the short edge of the module and carry the scintillation light there by means of clear fibers. Ruled out for eccessive light loss.



detector elements (metal enclosure not shown) shown in their position in the gaps (or on the inward side of the metal sheet for layer 0)



Proposed location for the front end stages of the readout electronics



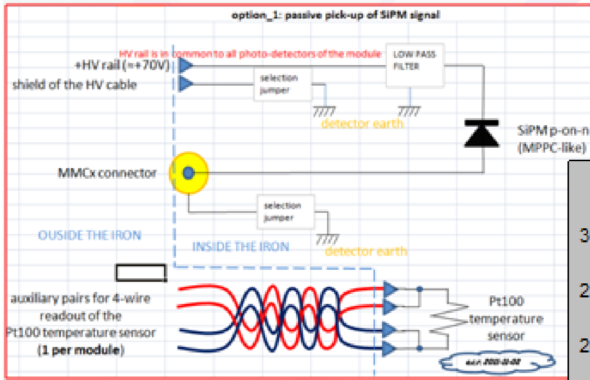
PCBs for "ON_DETECTOR" stages of the readout chain.

"mass termination" PCB.

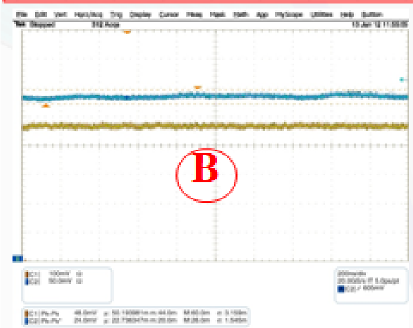
Double shielded differential twisted pair output cable (17 pairs).

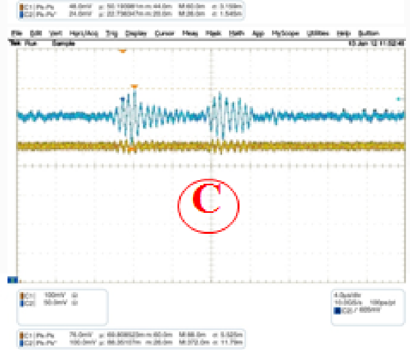
IFR electronics overview (TDR baseline)

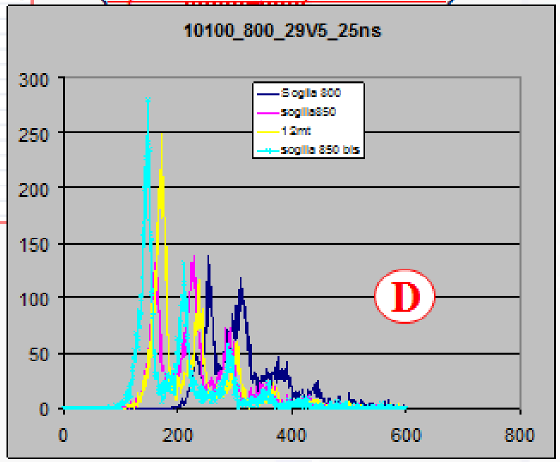
"straight-through" approach for the **"ON_DETECTOR"** stage: not baseline but tested nonetheless



Test of Single Ended option for "picking-up" the signals from SiPM (by R. Malaguti, INFN-FE)







The test was carried out by connecting a SensL 10100_800 SiPM (biased at 29,5V) to the EASIROC (A) development board and looking at the amplitude histogram of the dark current pulses. The yellow histogram refers to the case in which the SiPM was connected via a 12m long coaxial cable. THERE IS LITTLE DIFFERENCE WITH THE HISTOGRAM OBTAINED WITH A 0.25m LONG CABLE

The waveforms (B) shows the outputs of the LOW_GAIN stage (BLUE trace) and of the fast shaper (LIGHT BROWN trace) with the SensL connected with a 0,25m long cable and UNBIASED.

The waveforms (C) shows the outputs of the LOW_GAIN stage (BLUE trace) and of the fast shaper (LIGHT BROWN trace) with the SensL connected with the 12m long cable and UNBIASED. While there is certainly EMI noise pick up this didn't seem to affect the overall outcome of the test.

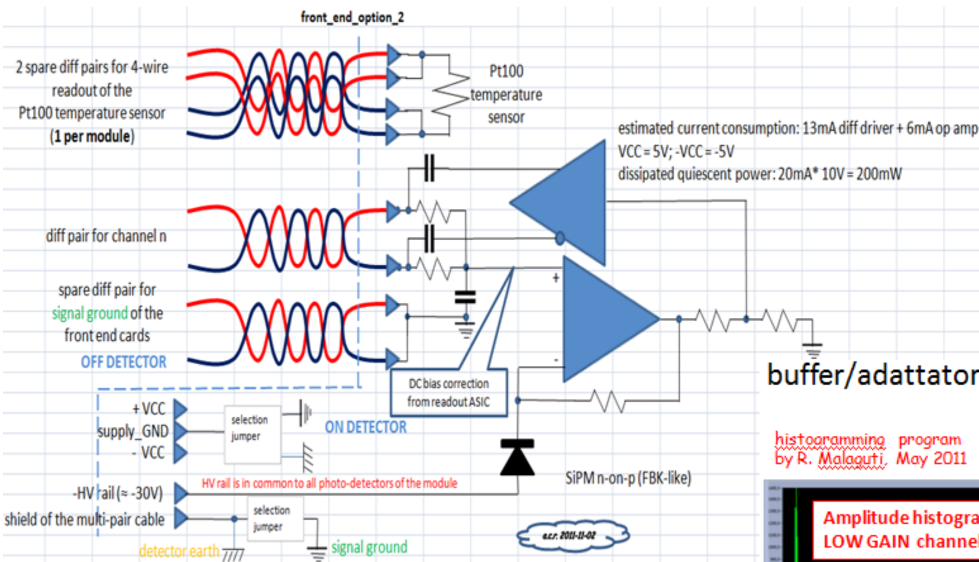
CAVEAT: only one channel was connected -> pick-up noise might increase with the number of channels connected

In this approach ONE SiPM was connected to the signal processing unit (**the EASIROC ASIC**) via a **12m long coaxial cable**: some EMI noise was picked up enroute (as shown in C) but the amplitude spectrum of the received pulse was still well defined!

IFR electronics overview (TDR baseline)

"analog buffer-only" approach for the **"ON_DETECTOR"** stage: not baseline but tested nonetheless

buffer/adattatore di polarita' per SiPM



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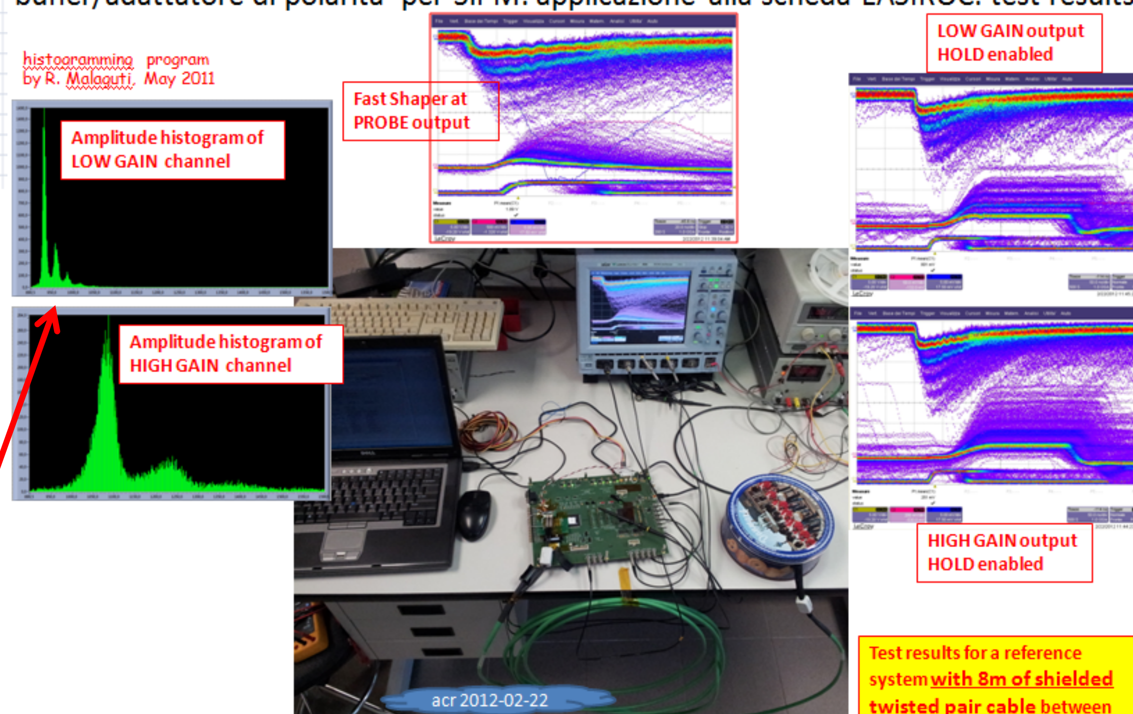
In this approach the front end stage only performs the functions of:

- setting the offset voltage to adjust the operating point of the SiPM
- amplifying the SiPM signal
- driving the amplified signal on the output differential twisted pair cable

buffer/adattatore di polarita' per SiPM: applicazione alla scheda EASIROC: test results



Test results for a reference system **with 8m of shielded twisted pair cable between driver and receiver**

PRO: the more critical processing stages might be located further away from high radiation area (BUT UNFORTUNATELY NOT AS FAR AS tHE RADIATION SHIELDING WALL)

CON: power consumption, cable cost, could sensitive to EMI interference (it worked well with **8m** of the high quality twisted shielded pair cable and the LAL Orsay "**EASIROC**" ASIC as the front end signal processor).

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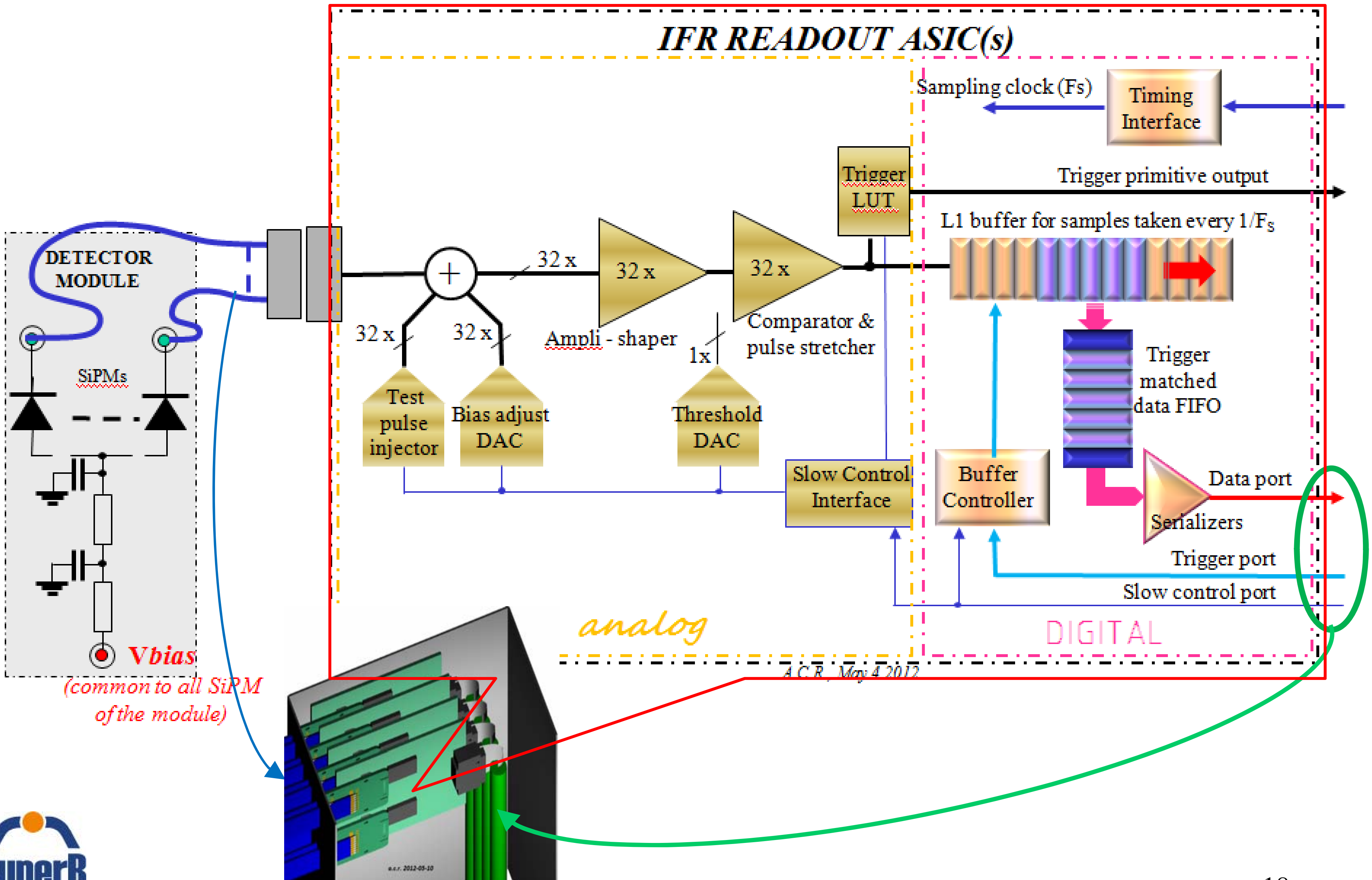
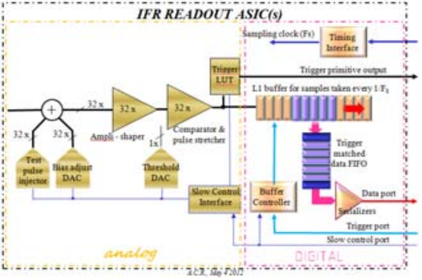
IFR electronics overview (TDR baseline)

Baseline approach: an "ON_DETECTOR" stage based on a dedicated ASIC





IFR electronics overview (TDR baseline)

Baseline approach: an "ON_DETECTOR" stage based on a dedicated ASIC

The ASIC must be designed to reliably operate in the SuperB background radiation environment

Specifications for a dedicated ASIC for SuperB IFR front end

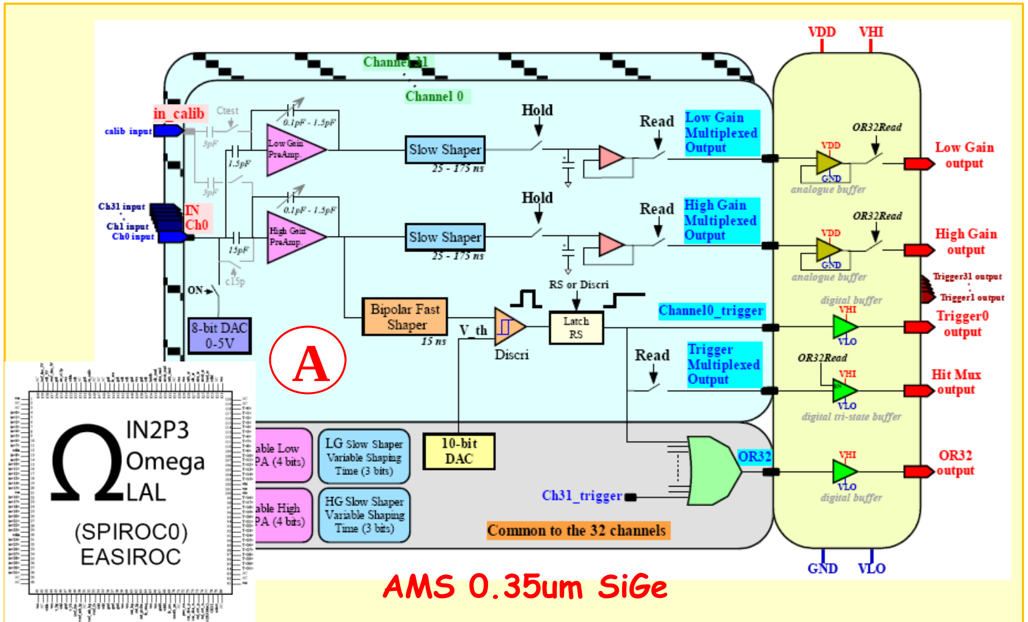
- (**AB**) input amplifier design suited for positive and negative signals ; linear dynamic range ≈100 p.e. equivalent signal
- (**AB**) a fast shaper design with peaking time in the range of a few ns, to minimize the pulse pile-up effects at high input rates
- (**AB**) individual bias setting DACs: range of a few Volts; resolution up to 8 bit; external or an internal voltage reference
- (**AB**) high speed comparator with differential topology to reduce the switching noise
- (**AB**) one common threshold setting DAC: range of a few Volts; resolution up to 10 bit; external or an internal voltage reference
- (**AB**) configurable test pulse injection circuitry
- (**DB**) SEU protected registers for all configurable features of the ASIC
- (**DB**) SEU protected slow control interface logic
- (**AB**) auxiliary differential output buffers for diagnostic purposes
- (**AB**) clock interface unit to generate all internal timing signals from the SuperB clock
- (**DB**) configurable latency buffer, based on a dual ported memory, holding the data during the trigger decision time
- (**DB**) trigger interface: to perform the extraction of the data from the proper window of the latency buffer upon the trigger request
- (**AB**) suitable low power serializers to transmit the trigger match data to the downstream readout stages
- (**DB**) Trigger primitives generator: a SEU protected configurable look-up table to generate trigger signals from the inputs

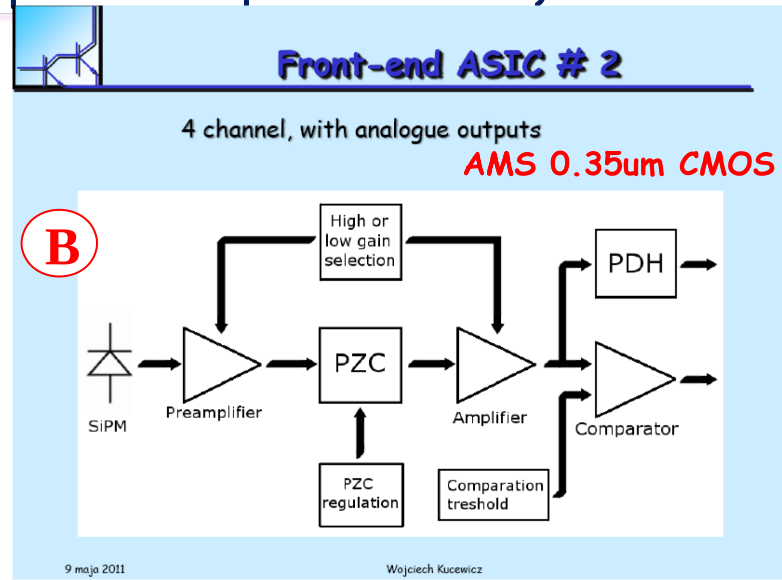
AB: analog block
DB: digital block

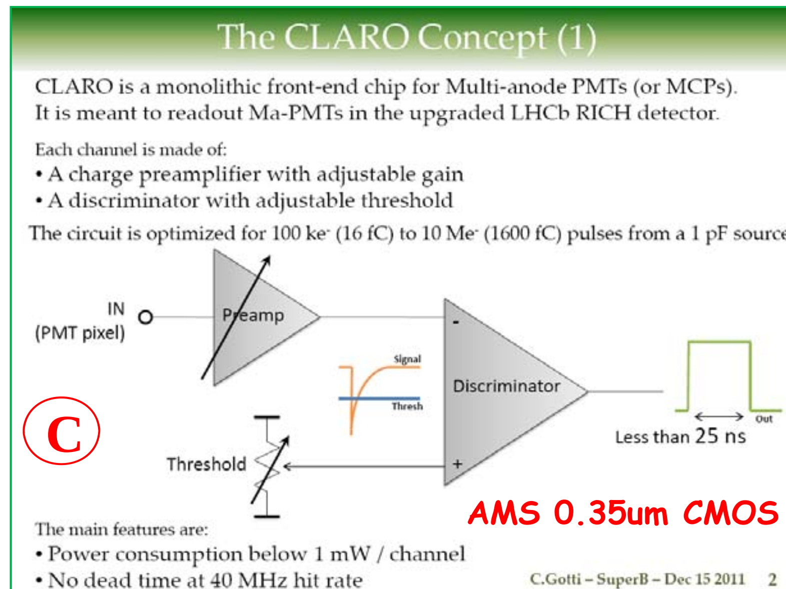
Experts involved in the ASIC development:

- *Wojciech Kucewicz, AGH Krakow*
- *Gianluigi Pessina, Claudio Gotti, INFN Milano Bicocca*
- *Gianni Mazza, Giulio della Casa, INFN Torino*

STEPPING STONES: existing ASICs implementing featuring part of the above specifications which have undergone neutron irradiation studies (see reports in the parallel sessions)





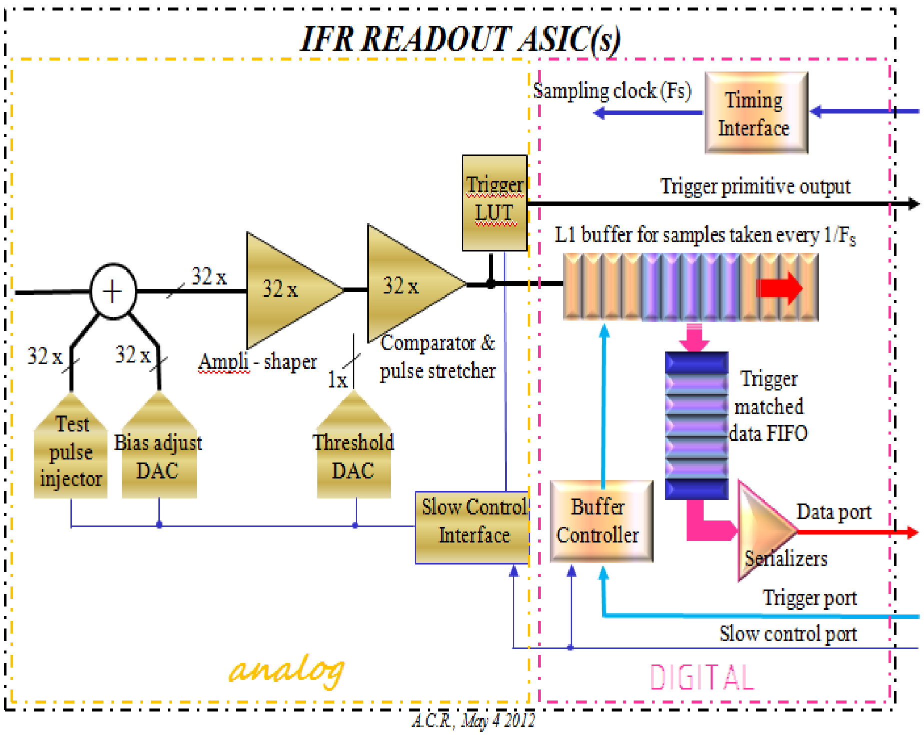


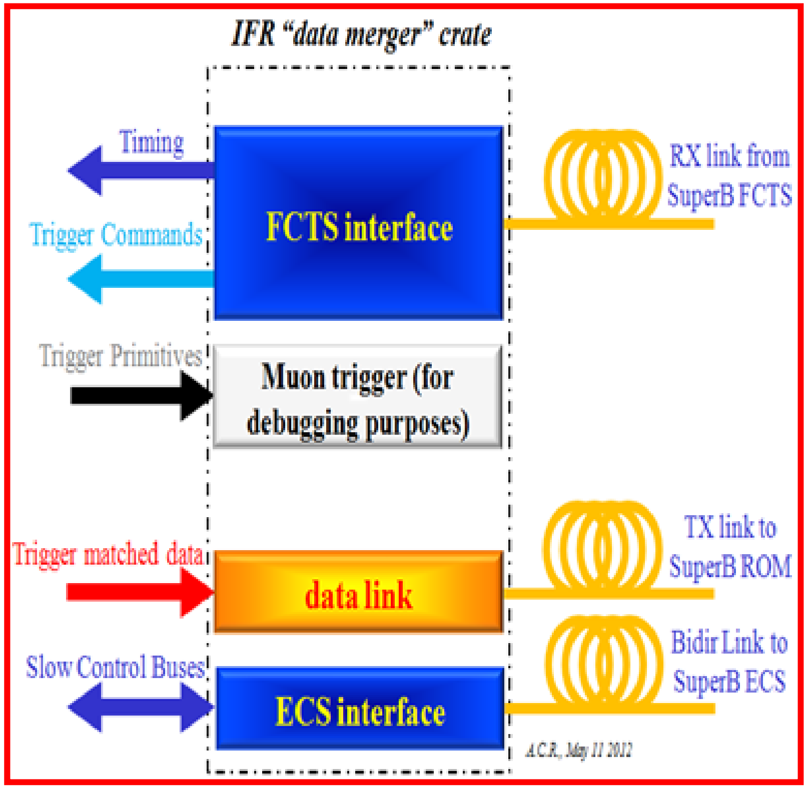
(A) The EASIROC has been designed by the Omega group of LAL and it has been extensively used and tested in Ferrara thanks to evaluation board provided by LAL. It has already described in previous presentations

(B) The RAPSODI ASIC#2 has been designed by **Woitek Kucewicz** of AGH University in Krakow, Poland. It has already been introduced in previous presentations

(C) The CLARO ASIC has been designed by **Gianluigi Pessina and Claudio Gotti** and presented at the 2nd SuperB meeting last December.

Baseline approach: downstream elements of the readout chain: the IFR "data merger" modules



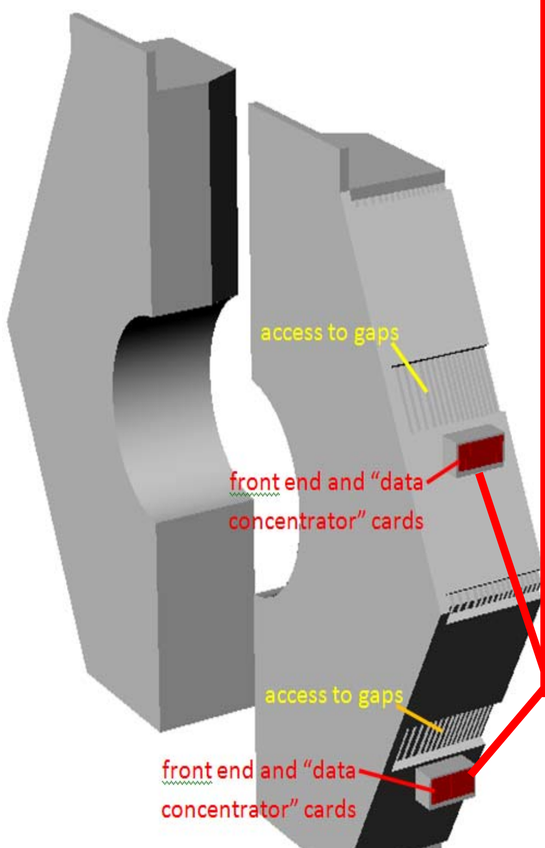


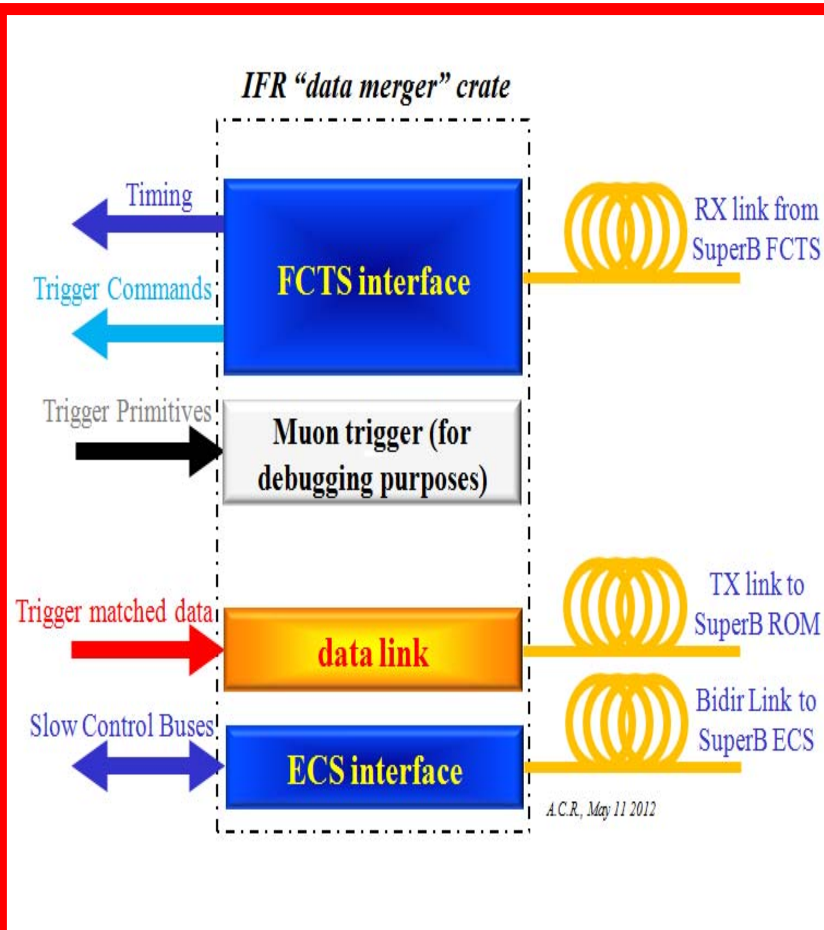
Functions performed by the units installed in a data-merger crate:

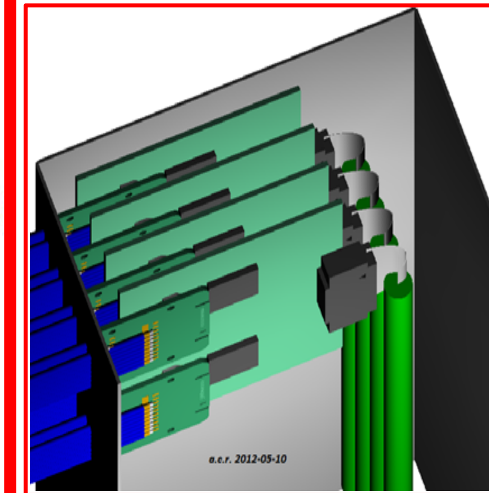
- **FCTS interface**: linked to the SuperB Fast Control and Timing System (FCTS), it fans out to the IFR front end cards the timing (clock and reset) and the received trigger commands
- **Muon trigger module** (optional): it processes trigger primitives generated by the IFR front end cards to generate a muon trigger for local debugging purposes
- **Data link**: data sent by the front end units in response to a trigger command is received by this unit and merged onto a suitable number (4 for the barrel section, 2 for the endcap ones) of high speed serial links connected to the ReadOut Modules (ROM) input port.
- **ECS interface**: this unit is linked via optical fiber to the SuperB Experiment Control System (ECS); it fans out configuration commands and calibration data to the front end cards and collects from them the operating status information.

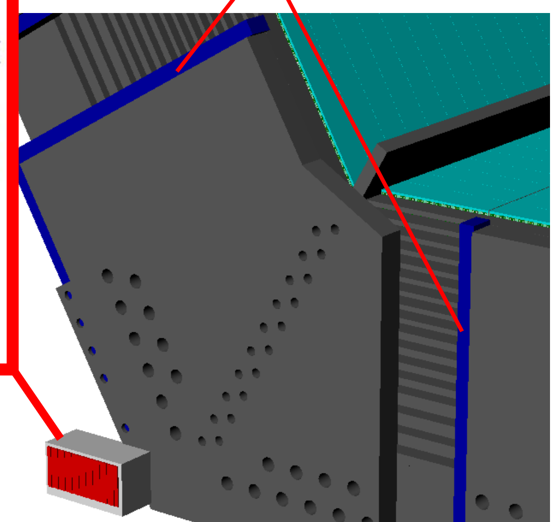
IFR electronics overview (TDR baseline)

Baseline approach: the IFR "data merger" locations







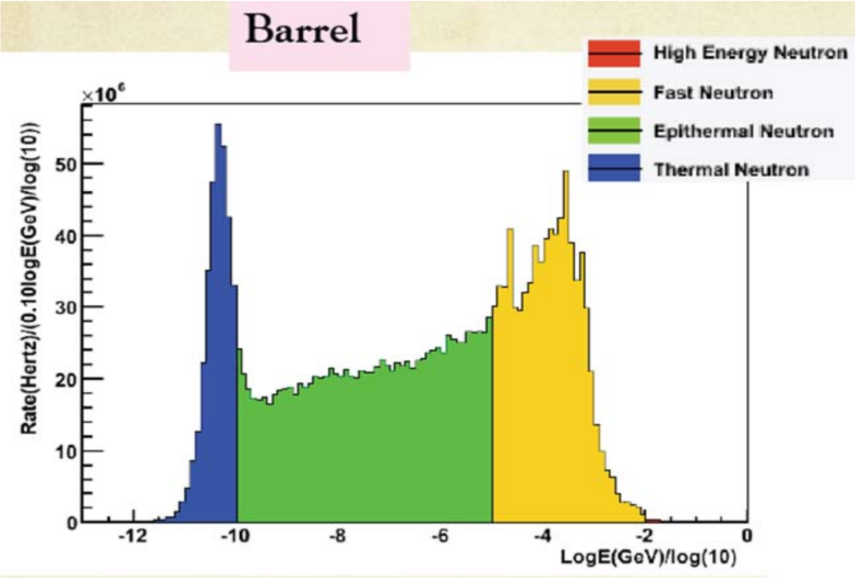


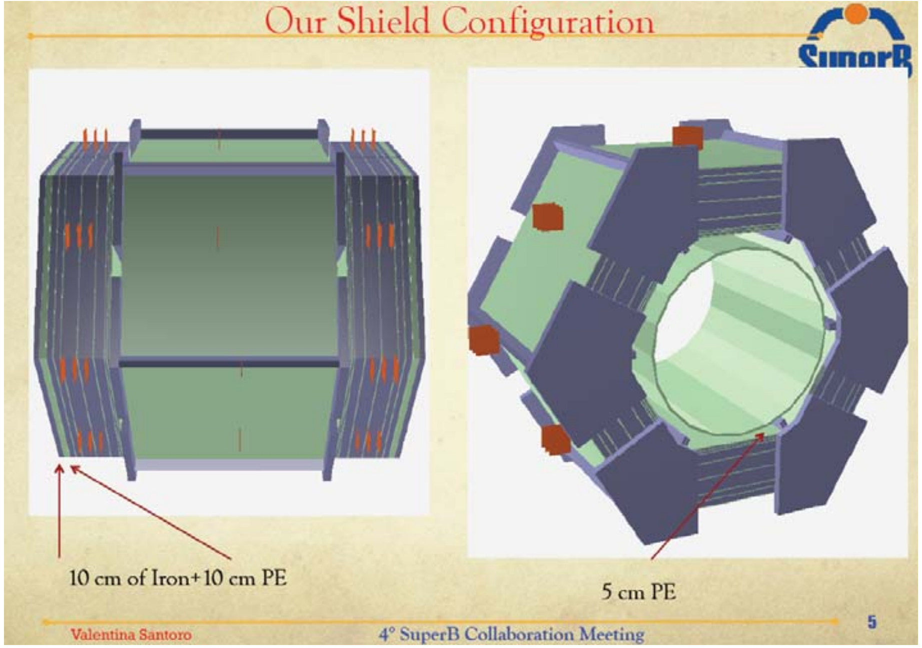
ALL the elements of the IFR readout electronics described above must be designed to reliably operate in the SuperB background radiation environment

Background radiation issues: damage from neutrons is the main concern

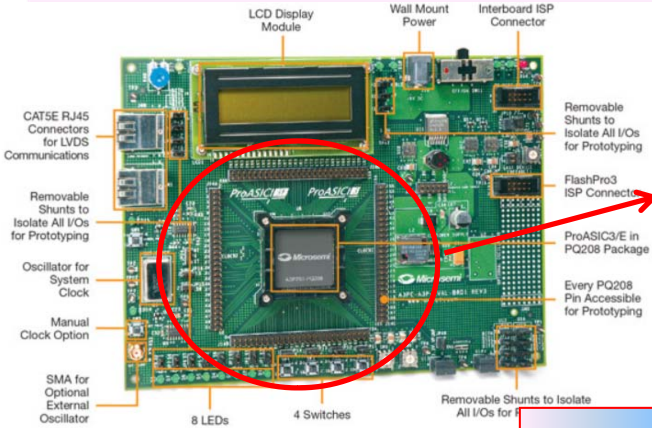
- Expected neutron flux @ superB:
  - ~ 50 n/cm^2/s (1 MeV equivalent)
  - → ~ 1.3 x 10^8 n/cm^2 /month (6.5 x 10^8 with safety factor)
  - → 1.6 x 10^9 n/cm^2/year (8 x 10^9 with safety factor)
  - → **~ 8x 10^{10} n/cm^2** (10 years x safety factor 5)
- Note that these numbers are 1MeV equivalent rates

BUT: number may change due to the insertion of radiation shields for the different components of the spectrometer

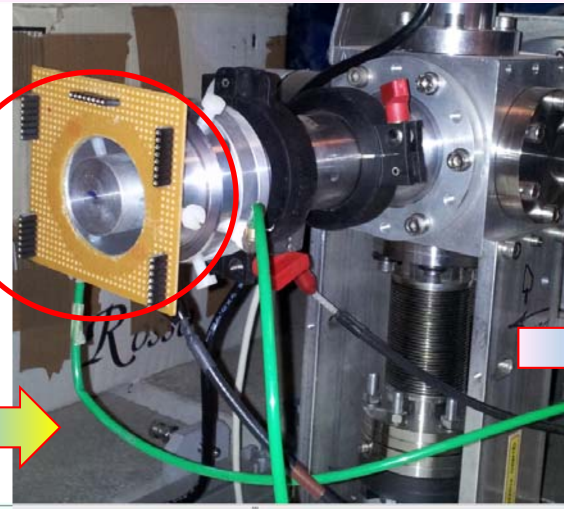


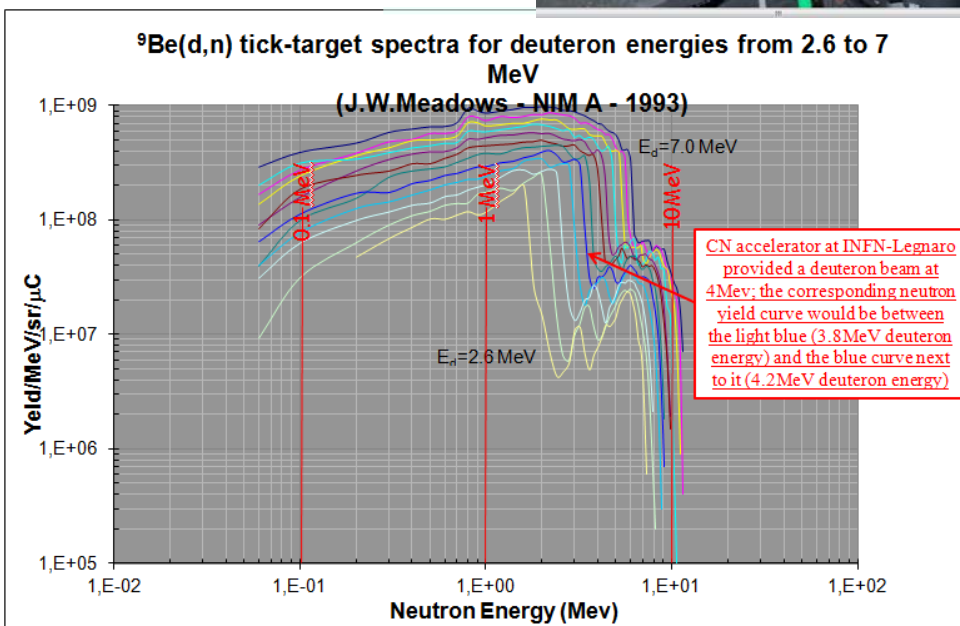


Results from tests at the CN facility of the INFN Laboratori Nazionali di Legnaro



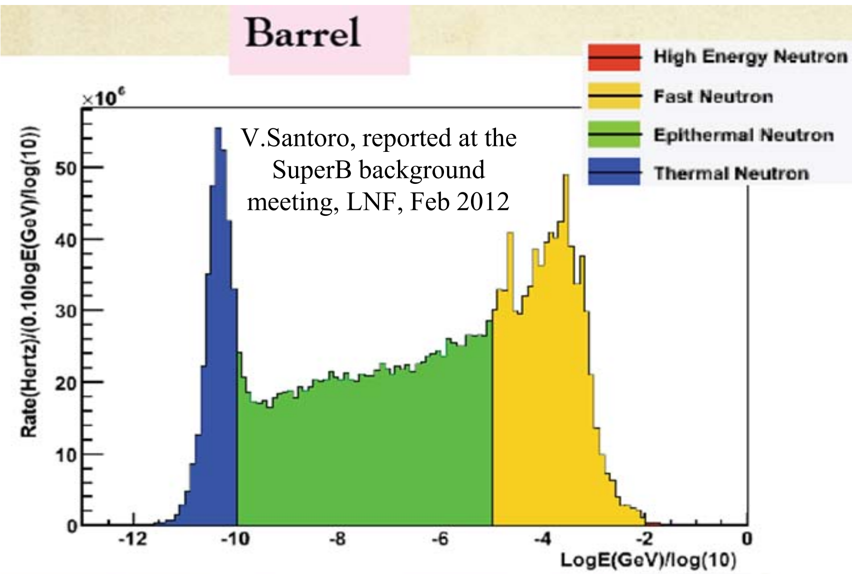
Evaluation board with an A3PE1500-PQ208 FPGA



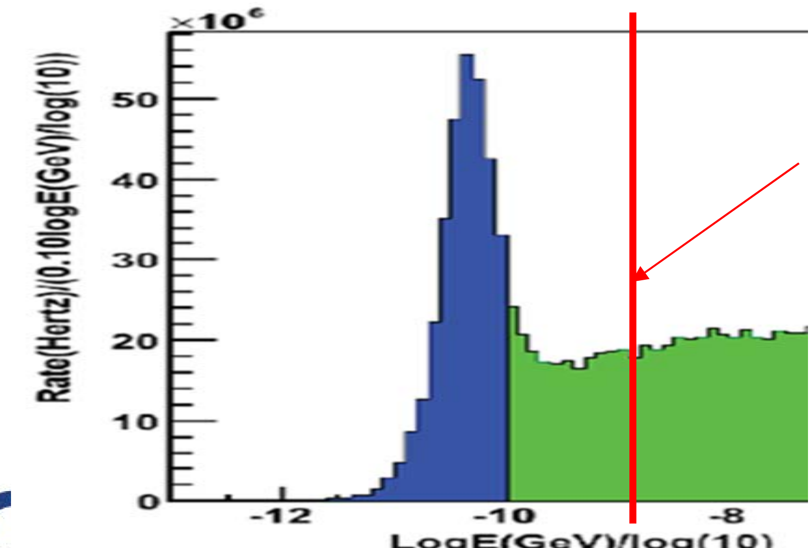


Acknowledgements:
We exploited beam time which had been allocated by our colleagues Roberto Stroili and Flavio Dal Corso who also provided the information needed to estimate the neutron flux.

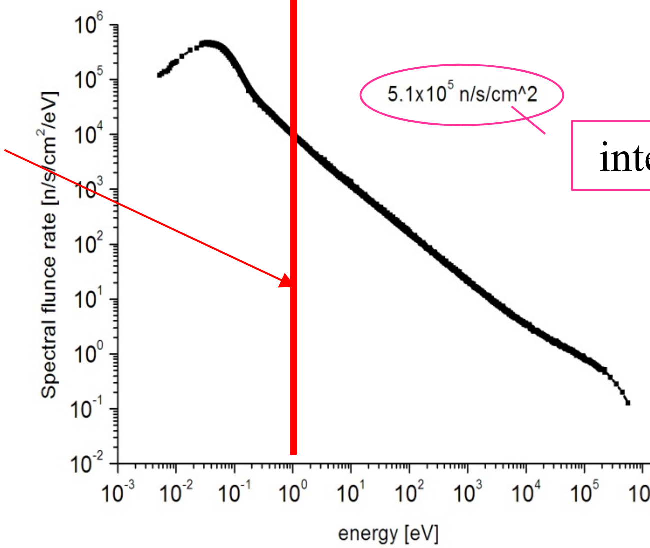
Results from tests at "GELINA", neutron time -of-flight facility at the Institute for Reference Materials and Measurements (IRMM)



V.Santoro, reported at the SuperB background meeting, LNF, Feb 2012



1 eV



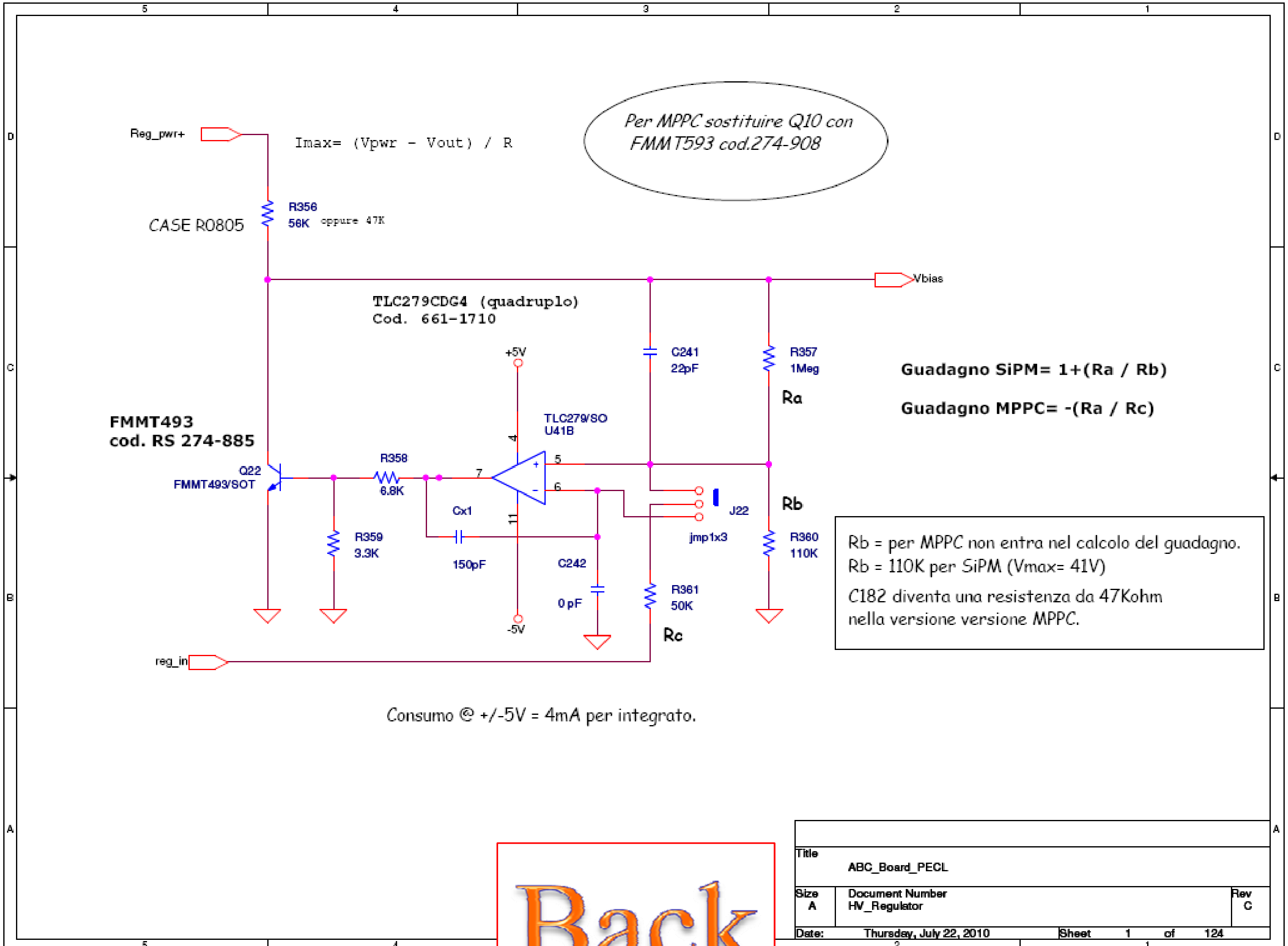
integral fluence

Topics to be covered in the "electronics" parallel sessions of this workshop

- "Thermal Stabilization of Silicon Photomultiplier measurement system for IFR" (Piotr Dorosz)
- "SiPM test with thermal neutrons at the IRMM" (A. Cotta Ramusino); more on this subject is covered in the R&D parallel sessions
- "CLARO and RAPSODI ASICs irradiation at the CN facility of the INFN-LNL" (A. Cotta Ramusino, Bartłomiej Rachwał)
- "Characterization of RAPSODI ASICs after Irradiation" (Mateusz Baszczyk)
- "Acquisition system for cosmic ray measurements" (Mateusz Baszczyk)
- submission of a short development time test ASIC in AMS 0.35um CMOS :
  - "An idea of IFR ASIC front-end with gain stabilization" (Juliusz Godek & Jacek Kołodziej)
  - "Test of CLARO chip readout" (from a presentation of Claudio Gotti et al. at the 3rd SuperB Meeting in LNF)
  - "CLARO-CMOS, a very low power ASIC for fast photon counting with pixellated photodetectors", G. Pessina et al

Extra slides

SuperB IFR electronics : APPENDIX A: schematic diagrams of some key parts of the "IFR_ABCD" board: individual SiPM bias



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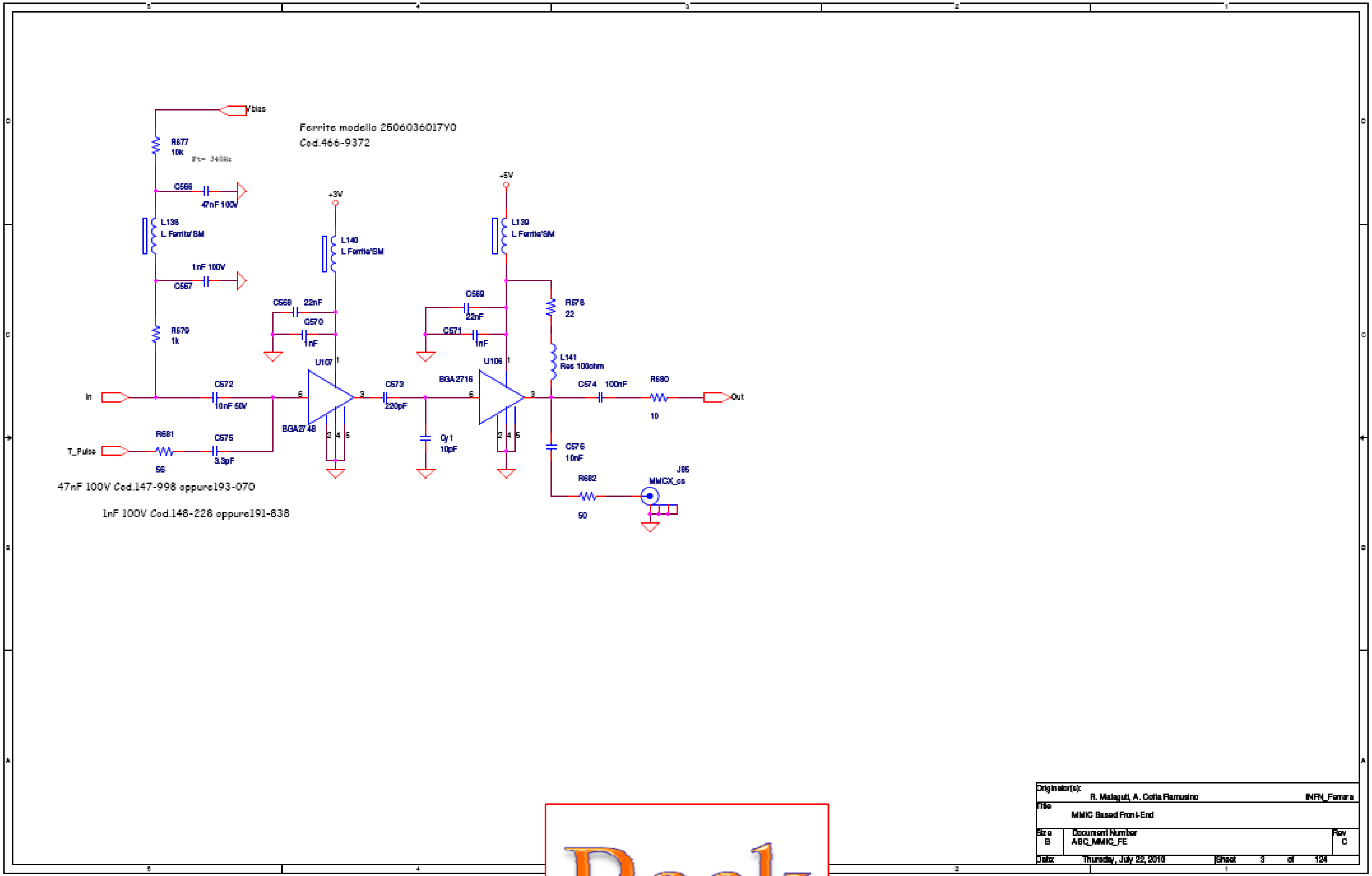

Vbias
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Ferrite modello 2506036017Y0
Cod.466-9372
C566
47nF 100V
L138
L Ferrite/SM
1nF 100V
C567
R679
1k
+3V
L140
L Ferrite/SM
C568
22nF
C570
1nF
U107
BGA2748
+5V
L139
L Ferrite/SM
C569
22nF
C571
1nF
U106
BGA2716
R678
22
L141
Res 100ohm
In
C572
10nF 50V
C573
220pF
Cy1
10pF
C574
100nF
R680
10
Out
T_Pulse
R681
56
C575
3.3pF
C576
10nF
R682
50
J85
MMCX_cs
47nF 100V Cod.147-998 oppure193-070
1nF 100V Cod.148-228 oppure191-838
Originator(s):
R. Malaguti, A. Cotta Ramusino
INFN_Ferrara
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MMIC Based Front-End
Size
B
Document Number
ABC_MMIC_FE
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Date:
Thursday, July 22, 2010
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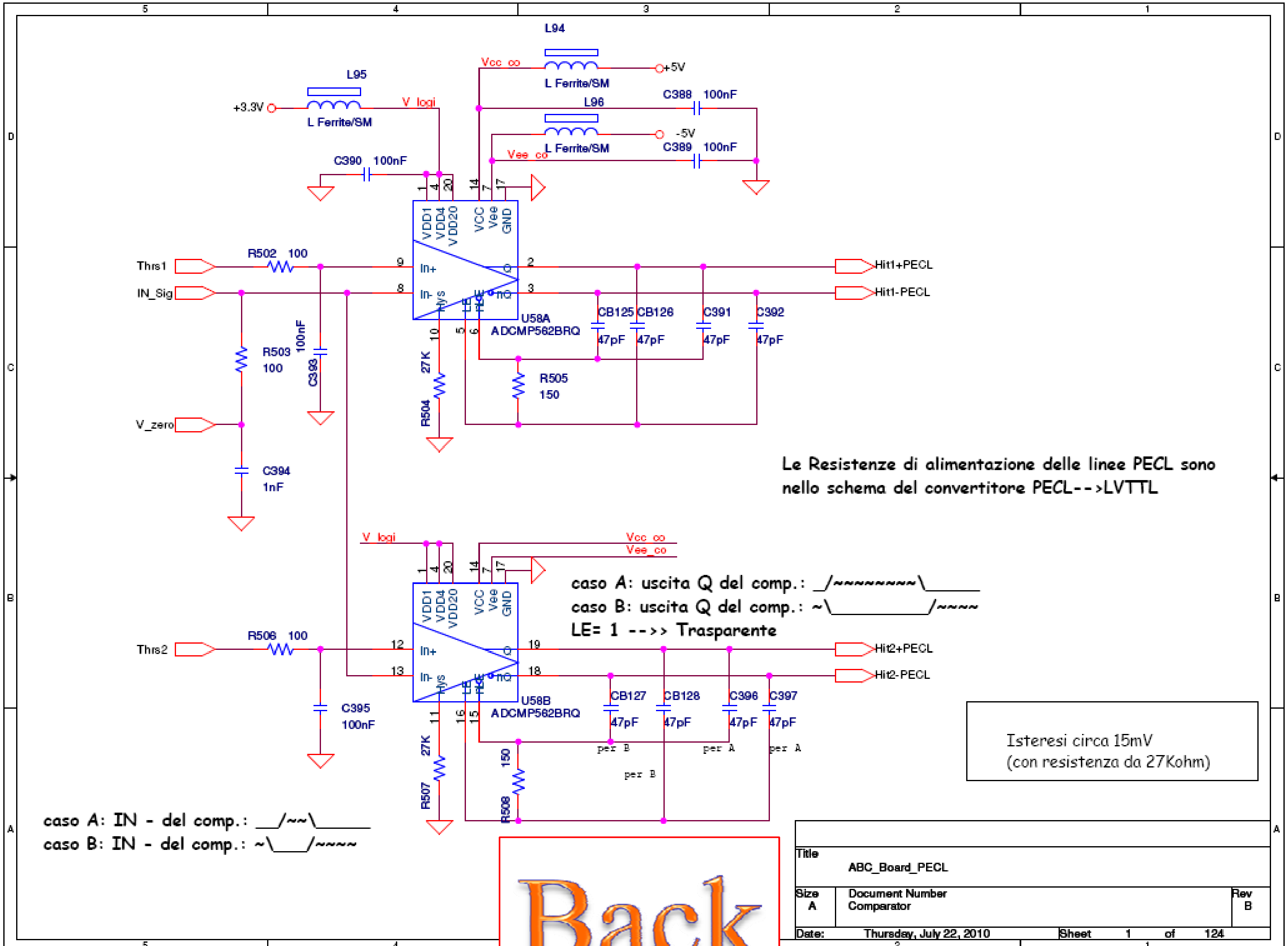
L94
L Ferrite/SM
+5V
Vcc_co
L95
+3.3V
L Ferrite/SM
V_logi
L96
C388 100nF
-5V
L Ferrite/SM
C389 100nF
Vee_co
C390 100nF
VDD1 VDD4 VDD20 VCC Vee GND
R502 100
Thrs1
IN_Sig
In+
In-
Q
nQ
Hit1+PECL
Hit1-PECL
U58A
ADCMP562BRQ
CB125 CB126 C391 C392
47pF 47pF 47pF 47pF
R503 100
100nF C393
27K R504
R505 150
V_zero
C394 1nF
Le Resistenze di alimentazione delle linee PECL sono nello schema del convertitore PECL-->LVTTL
V_logi
Vcc_co
Vee_co
caso A: uscita Q del comp.: _/~~~~~~~~_____
caso B: uscita Q del comp.: ~__________/~~~~
LE= 1 -->> Trasparente
Thrs2
R506 100
Hit2+PECL
Hit2-PECL
U58B
ADCMP562BRQ
CB127 CB128 C396 C397
47pF 47pF 47pF 47pF
C395 100nF
27K R507
150 R508
per B per A per A per B
Isteresi circa 15mV
(con resistenza da 27Kohm)
caso A: IN - del comp.: __/~~_____
caso B: IN - del comp.: ~___/~~~~
Title ABC_Board_PECL
Size A
Document Number Comparator
Rev B
Date: Thursday, July 22, 2010
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