* 1. **Silicon Vertex Tracker**

**1.1.1 Electronic Readout for Strip and Striplet Detectors**

The front-end processing of the signals from the silicon strip detectors will be performed by custom-designed ICs mounted on hybrid circuits that distribute power and signals, and thermally interface the ICs to the cooling system. As discussed below, the very different features of inner (Layer 0 - 3) and outer layers (4 and 5) of the SVT set divergent requirements to the readout chips, which most probably makes it necessary to develop two distinct integrated circuits. This obviously holds also in the case a different technology (pixels) is adopted for Layer 0 instead of short strips (striplets). Generally speaking, both types of ICs will consist of 128 channels, each connected to a detector strip. The signals from the strips, after amplification and shaping will be compared to a preset threshold. If a signal exceeding the threshold is detected, a 4 bit analog information about the signal amplitude will be provided by an ADC: this will mostly serve for calibration and monitoring purposes in the innermost layers, whereas in outer layers it will be essential for dE/dx measurements**.** The dimensions of the readout IC are expected to be about 6 x 4 mm2 *.* As discussed in the SVT HDI subsection of this TDR, the dimensions of the HDI set a 6 mm upper limit on the side of the chip with the bonding pads for the interconnection with the strip sensors. The power dissipation will be below 4 mW/channel including both analog and digital sections. For each channel with a signal above threshold, the strip number, the amplitude information, the chip identification number and the related time stamp will be stored inside the chip waiting for a trigger signal for a time corresponding to the trigger latency (about 7 us, corresponding to a 150 kHz trigger rate). When a trigger is received, data will be read out and transmitted off chip, otherwise they will be discarded. The data output from the microstrip detector will be sparsified, i.e. will consist only of those channels generating a hit. The readout integrated circuits must remain functional up to 5 times nominal background.

The option of operating in a data push fashion could be preserved for the external layers, where this will be allowed by the low strip hit rate. This will give the possibility to feed data from these layers to the trigger system.

**1.1.2 Readout chips**

**Requirements**

The microstrip electronics must ensure that the detector system operates with adequate efficiency, but also must be robust and easy to test, and must facilitate testing and monitoring of the microstrip sensors. AC coupling is assumed between the strips and the readout electronics.

* **Mechanical Requirements:**

Number of channels per chip: 128

Chip size: width ≤ 6 mm, length ≤ 4 mm

Pitch of input bonding pads: ≤ 45 um

* **Operational Requirements:**

Operating temperature: < 40 °C

Radiation tolerance: > 4 Mrad/year, > 6 . 1012 neq/cm2/year

 (these are the expected values in Layer 0; in outer layers, radiation levels are at least on order of magnitude lower

Power dissipation: < 4 mW/channel

Detector and fanout capacitance: 10 pF ≤ CD ≤ 70 pF

(the chip must be stable when sensor strips are disconnected from the input pads of the analog channels)

* **Dynamic range:** The front-end chips must accept signals from either P and N-side of the strip detectors. A linear response of the analog processing section is required from a minimum input charge corresponding to 0.2 MIP up to a full dynamic range of 10-15 MIP charge for dE/dx measurements.
* **Analog Resolution:** The front-end chips have to provide an analog information about the charge collected in the detector, which will be also used for calibrating and monitoring the system. A resolution of 0.2 MIP charge is required for dE/dx measurements. In case of a compression-type ADC, based on the time-over-threshold technique (ToT), this may translate in 4 bits of information.
* **Efficiency:** At design luminosity, the microstrip readout must have a hit efficiency of at least 95% during its entire operational lifetime. This includes any loss of data by readout electronics or readout dead time.

# Readout bandwidth: Data coming out of the chip will be substantially reduced by operating in a triggered mode. The chips can use up to 4 output LVDS lines, as it is needed to handle the higher data throughput in inner SVT layers.

* **Radiation Tolerance:** All the components of the microstrip readout system must remain operational up to 10 years of SuperB running at the nominal luminosity.

# Peaking Time: The constraints for the peaking time of the signal at the shaper output are dictated by different needs in inner and outer layers. In Layer 0, the high occupancy due to background and the need to avoid pulse overlap and consequent hit inefficiencies set the maximum peaking time at tP = 25 ns, which also allow for a high timing resolution (see below). In the external layers 4 and 5, where background hit frequency is much smaller and where strips are longer and have a larger capacitance, the peaking time will be mostly determined by the need of reducing series noise contributions and has to be in the range of 0.5 - 1 s.

# Signal-to-Noise Ratio: Concerning the signal, this requirement has to take into account the different thickness of silicon detectors in inner (200 m) and outer (300 m) layers, as well the signal spread among various strips that depends on the track angle inside detectors and that, again, may vary in different SVT layers. Noise–related parameters (strip capacitance and distributed resistance) also sizably vary across the SVT. A signal-to noise ratio of 20 has to be ensured across the whole SVT and should not decrease significantly after irradiation. Here are the two extreme cases (where the equivalent noise charge ENC includes the thermal noise contribution from the distributed resistance of the strips):

# Layer 0 striplets: ENC ~ 700 e-  at CD = 10 pF and at tP = 25 ns

# Layer 5 strips: ENC ~ 1000 e-  at CD = 70 pF and at tP = 1 s

# Threshold and Dispersion: Each microstrip channel will be read out by comparing its signal to a settable threshold around 0.2 MIP. Threshold dispersion must be low enough that the noise hit rate and the efficiency are degraded to a negligible extent. Typically, this should be 300 rms electrons at most and should be stable during its entire operational lifetime.

* **Comparator Time Resolution:** The comparator must be fast enough to guarantee that the output can be latched in the right time stamp period.
* **Time Stamp:** 30 ns time stamp resolution is required for inner layers to get a good hit time resolution in order to reduce the occupancy in the offline time window (50-100ns). In the outer layers the time stamp resolution is less critical since the hit time resolution will be dominated by the long pulse shaping time. A single 30 ns time stamp clock in all layers will be used.
* **Chip clock frequency:** Two main clocks will be used inside the readout chip, the time stamp clock (33 MHz) and the readout clock (132 MHz or 198 MHz). These clocks will be synchronized with the 66 MHz SuperB system clock. In case the analog-to-digital conversion is based on the Time-Over-Threshold method, a ToT clock has to be generated inside the chip. The ToT clock period should at least match the pulse shaping time to get a good analog resolution. A faster ToT clock could slightly improve the analog resolution but an upper limit (~3.5) on the ratio between ToT clock frequency and the shaping time frequency is imposed by the required dynamic range needed for low momentum particle dE/dx measurements (~10-15 MIP) and the number of bits available for ToT. With the experience of the BaBar Atom chip a TOT clock frequency 3 times higher than the pulse shaping frequency could be used: 132 MHz for L0, 66 MHz for L1-2, 16.5 MHz for Layer3 and 6.6-3.3 MHz for L4-5.
* **Masking, Kill and Inject:** Each micro-strip channel must be testable by charge injection to the front-end amplifier. By digital control, it shall be possible to turn off any micro-strip element from the readout chain.
* **Maximum data rate:** Simulations show that machine-related backgrounds dominate the overall rates. At nominal background levels (including a safety factor of 5), the maximum hit rate per strip goes from about 1 MHz/strip in Layer0 to about 50 kHz/strip in Layer 5, z-side.
* **Deadtime limits:** The maximum total deadtime of the system must not exceed 10 % at a 150 kHz trigger rate and background 5 times the nominal expected rate.
* **Trigger specifications:** The trigger has a nominal latency of about 7 us, a maximum jitter of 0.1 us, and the minimum time between triggers is 70 ns. The maximum Level 1 Trigger rate is 150 kHz.

## Cross-talk: Must be less than 2 %

# Control of Analog Circuitry on Power-Up: Upon power-up, the readout chip shall be operational at default settings.

# Memory of Downloaded Control of Analog Circuitry: Changes to default settings shall be downloadable via the readout chip control circuitry, and stored by the readout chip until a new power-up cycle or additional change to default settings.

* **Read-back of Downloadable Information:** All the data that can be downloaded also shall be readable. This includes data that has been modified from the default values and the default values as applied on each chip when not modified.
* **Data Sparsification:** The data output from the microstrip detector shall be only of those channels that are above the settable threshold.
* **Microstrip** **output data content:** The microstrip hit data must include the time stamp and the microstrip hits (strip number and relevant signal amplitude) for that time stamp. The output data word for each strip hit should contain 16 bits (7 strip address, 4 ToT, 1 type (Hit or Time Stamp) 4 bits to be defined). A 10-bit time stamp information (with 6 additional bits: 1 type, 5 bits to be defined) will be attached to each group of hits associated to a given time stamp (hit readout will be time-ordered).

**1.1.3 Readout Chip Implementation**

The SuperB SVT readout chips are mixed-signal integrated circuits in a 130 nm CMOS technology and are being designed to comply with the requirements discussed above. Each chip comprises 128 analog channels, each consisting of a charge-sensitive preamplifier, a unipolar semi-Gaussian shaper and a hit discriminator. A polarity selection stage will allow the chip to operate with signals delivered both from n- and p-sides of the SVT double-sided strip detectors. A symmetric baseline restorer may be included to achieve baseline shift suppression.When a hit is detected, a 4 bit analog-to-digital conversion will be performed by means of a Time-Over-Threshold (ToT) detection. The hit information will be buffered until a trigger is received; together with the hit time stamp, it will be then transferred to an output interface, where data will be serialized and transmitted off chip on 2 output LVDS lines. An n-bit data output word will be generated for each hit on a strip. A programming interface accepts commands and data from a serial input bus and programmable registers are used to hold input values for DACs that provide currents and voltages required by the analog section. These registers have other functions, such as controlling data output speed and selecting the pattern for charge injection tests.

Given the very different requirements of inner and outer layers, in terms both of detector parameters and hit frequency, two different chips will be designed; they will be based on a same data protocol, but will be optimized for operation at different clock frequencies.

The block diagram of the analog channel is shown in Fig. 1.1.1.

Peaking time selection

Fig. 1.1.1 Analog channel block diagram.

The digital readout of the matrix will exploit the architecture that was originally devised for a high-rate, high-efficiency readout of a large CMOS pixel sensor matrix. Each strip has a dedicated array of pre-trigger buffers, which can be filled by hits with different time stamps. The size of this array (32 buffers) is determined by the maximum strip hit rate (inner layers) and by the trigger latency. After arrival of a trigger, only hits with the same time stamp as the one provided by the triggering system send their information to the back-end. The array of 128 strips is divided in four sections, each with a dedicated sparsifier encoding the hits in a single clock cycle. The storage element next to each sparsifier (barrel level-2) acts like a FIFO memory conveying data to a barrel-L1 by a concentrator which merges the flux of data and preserves the time order of the hits. This barrel-L1 will drive the output data bus which will use one or two output lines depending on the data throughput and will be synchronous to a 198 MHz clock.

FE

Ctrl

 logic

Buf

 #k

...

Buf

 #1

ADC

Or ToT

BUF #1

readout/slow control

strip #127

strip #0

FE

Ctrl

 logic

Buf

 #k

...

Buf

 #1

ADC

Or ToT

**Sparsifier**

**~hit\_rate \* trig\_latency**

Triggered hits only

Fig. 1.1.2. Readout architecture of the SVT strip readout chips.

**1.1.4 R&D for strip readout chips**

The R&D to support the development of the SuperB strip readout chips has begun in 2011. The chosen technology for integration is a 130 nm CMOS process: this has an intrinsically high degree of radiation resistance, which can be enhanced with some proper layout prescriptions such as enclosed NMOS transistors and guard rings. There is a large degree of experience with mixed-signal design in this CMOS node that was gained in the last few years inside the HEP community.

The readout architecture is being tested with realistic data created by Monte Carlo analysis of the interaction region. Verilog simulations demonstrate that the chip will be able to operate with a 99% readout efficiency in the worst case condition, which includes the safety factor of 5 in the background levels.

The analog section of the chip is being optimized from the standpoint of noise, comparator threshold dispersion and sensitivity to variations of process parameters. It will be possible to select the peaking time of the signal at the shaper output (25 - 100 ns for inner layers, 400 ns – 1 us for outer layers) by changing the value of capacitors in the shaper. In this way the noise performances of the chip can be optimized according to the signal occupancy, preserving the required efficiency. Fig. 1.1.3 shows the main parameters of the analog section, according to simulation estimates for realistic values of detector parameters and strip hit rates. The loss in efficiency is determined by the limits in the double pulse resolution of the analog section, which depends on the signal peaking time. An acceptable compromise will be found here with the noise performance.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Layer | CD (pF) including fanout (with ganging) | Available tP (ns) | Selected tP (ns) | Total ENC (e rms) | Total ENC after 7.5 years (e rms) | Total ENC after 7.5 years with x5 safety factor (e rms) | Hit rate /strip (kHz)nominal | Efficiency 1-N nominal | Efficiency 1-N with x5 safety factor |
| 0 – side 1 | 11.2 | 25 – 200, with 25 ns steps | 25 |  |  |  | 187 | 0.99 | 0.95 |
| 0 – side 2 | 4 | 25 |  |  |  | 187 | 0.99 | 0.97 |
| 1 phi | 33.4 | 75 | 850 | 930 | 1180 | 170 | 0.98 | 0.92 |
| 1 z | 27.6 | 75 | 925 | 1025 | 1345 | 134 | 0.98 | 0.91 |
| 2 phi | 37.2 | 100 | 815 | 895 | 1165 | 134 | 0.98 | 0.90 |
| 2 z | 30.3 | 100 | 910 | 1010 | 1335 | 134 | 0.98 | 0.88 |
| 3 phi | 35.7 | 150 | 890 | 1040 | 1505 | 116 | 0.96 | 0.82 |
| 3 z | 40.8 | 150 | 1030 | 1140 | 1505 | 79 | 0.98 | 0.90 |
| 4 phi | 52.5 | 375, 500, 750, 1000 | 500 | 1075 | 1265 | 1805 | 25 | 0.98 | 0.92 |
| 4 z | 47.2 | 500 | 895 | 1115 | 1715 | 13.4 | 0.99 | 0.95 |
| 5 phi | 65.5 | 750 | 1085 | 1205 | 1530 | 16.2 | 0.98 | 0.93 |
| 5 z | 52.2 | 750 | 855 | 965 | 1280 | 8.8 | 0.99 | 0.95 |

Fig. 1.1.3 Main parameters of the analog section of the SVT strip readout chips.

In 2012, the submission of a chip prototype including 64 analog channels and a reduced-scale version of the readout architecture is foreseen.

The submission of the full-scale, 128-channels chip prototypes is then scheduled in late 2013. This version will have the full functionality of the final production chip.

**References**

[1] Gabrielli A, et al, High efficiency readout circuits for large matrices of pixels, *Nucl. Instr. Meth. A* 2011; **658**: 141-144.