P-SUPERB

Sezione di Pavia

Status report

Consiglio di Sezione INFN Pavia, 30 maggio 2012

Gruppo P-SUPERB Pavia

Responsabile: Valerio Re

- Università di Pavia
- Università di Bergamo

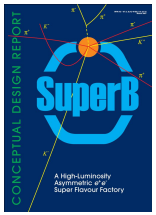
Attività principali

- Sviluppo di MAPS (Monolithic Active Pixel Sensors) in CMOS 130 nm per il Layer 0 di SVT
- Chip di lettura rivelatori a strip di SVT, opzione a pixel ibridi per Layer 0

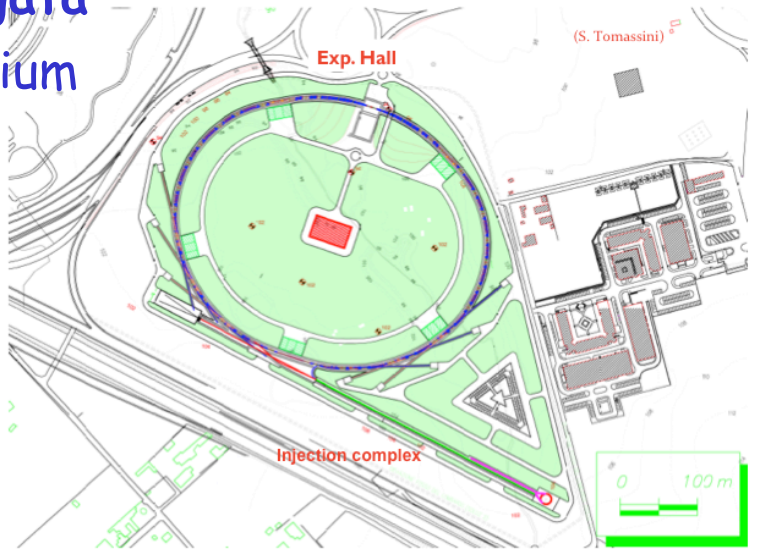
The SuperB Project

- Flavour physics promises sensitivity to New Physics … but **large statistics is needed** (50-100 ab-1) → upgrade of **~2 orders of magnitude** in **Luminosity** needed w.r.t the first generation B-Factories.
- The **SuperB** factory is the Italian e+ e- accelerator concept that allows to reach L =10^{36} **cm**$^{-2}$**s**$^{-1}$ with moderate beam current (2A) using very small beam size (~1/100 of first generation B-Factories beams)

- **2007** : **Conceptual Design Report published**
- **2010** : **Approved** by the Italian Government (250 ME allocated for the Infrastructures)
- **2011** : **Established site: Roma Tor Vergata**
- **Management** under **Cabibbo Lab** consortium (INFN, Uni Tor Vergata).
- **2012: Accelerator costing review**
  Technical Design Report



SuperB @ Tor Vergata



FEL @ SuperB

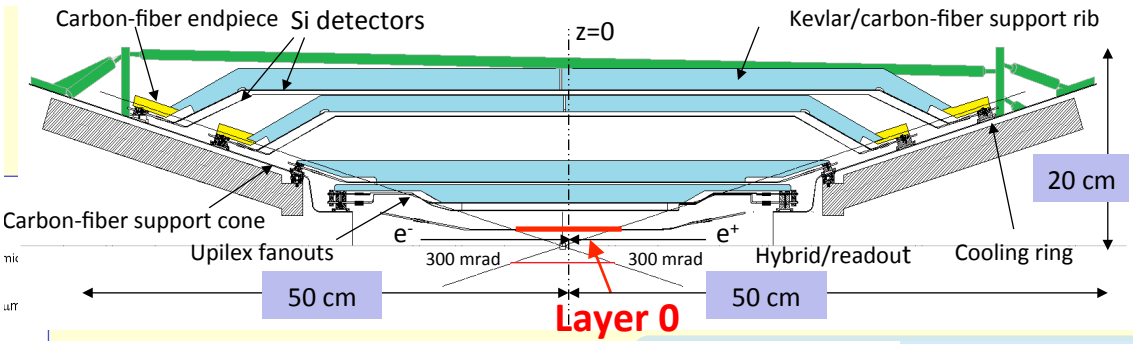
- The SuperB Linac (LINear ACcelerator) is designed to inject electrons in the accelerator ring at an energy of 6.7 GeV and it is perfectly compatible with a high-performance FEL, able to produce monochromatic radiation in the region of "hard" X-rays

- Production of ultra-short radiation pulses, on a scale of femto-seconds, useful to "filming" the dynamics of extremely fast processes. The extraordinary potentiality of this technology can be applied in the science of new materials, the development of nanotechnology, cellular biophysics and protein crystallography

- The FEL will not in any way compromise the performance of the Linac, designed to accelerate and inject the electrons in the SuperB ring. Although occurring continuously, the electrons packets are injected in the FEL at a frequency rate that is very different from that of electrons injected in the SuperB ring, thus avoiding limitations on the performances of the accelerator.

The SuperB Silicon Vertex Tracker

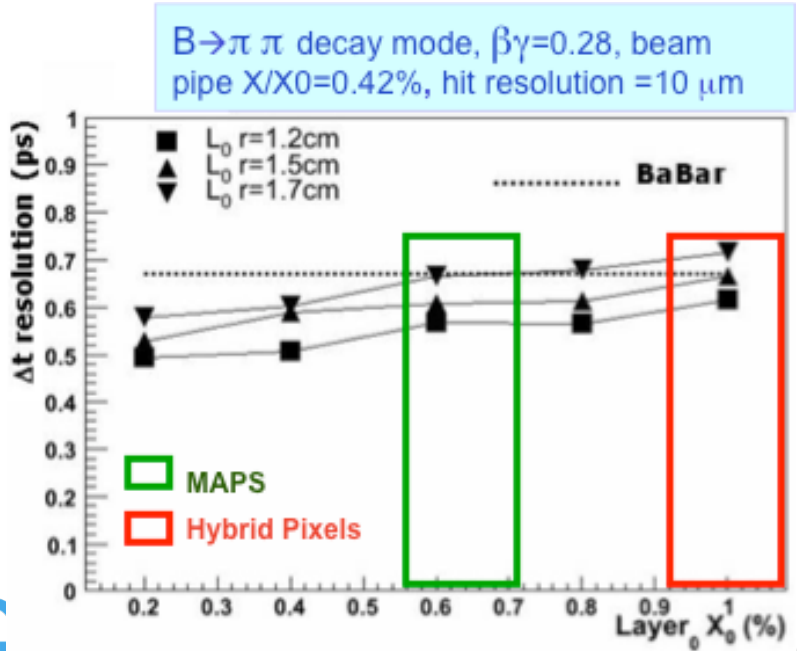
The SVT provides precise tracking and vertex reconstruction, crucial for time dependent measurements.



BaBar SVT

- 5 Layers of double-sided Si strip sensor
- Low-mass design. (P_t < 2.7 GeV)
- Stand-alone tracking for slow particles.
- 97% reconstruction efficiency
- Resolution ~15μm at normal incidence

SuperB SVT based on Babar SVT design for R>3cm. BUT:



1) reduced beam energy asymmetry (7x4 GeV vs. 9x3.1 GeV) requires an improved vertex resolution (~factor 2)

- Layer0 very close to IP (@1.5 cm) with low material budget (<1% X_0) and fine granularity (50 μm pitch)
- Layer0 area 100 cm^2

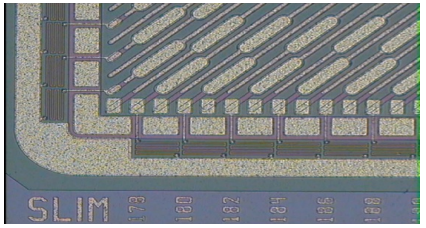
2) bkg levels depend steeply on radius

- Layer0 needs to be fast and rad hard
  hit rate 20 MHz/cm^2, TID 3 MRad/yr, eq. neutron fluence 5 x 10^{12} n/cm^2/yr
  x5 safety factor to be inlcuded!

SuperB SVT Layer 0 technology options

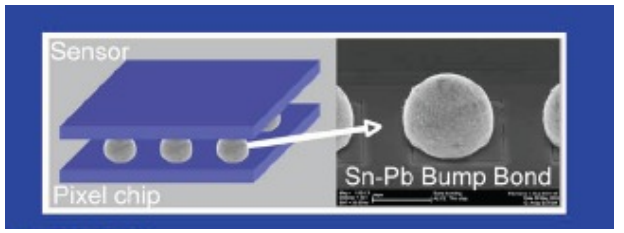
Complexity

- **Striplets option:** mature technology, not so robust against background occupancy.
  - Marginal with background rate higher than ~ 5 MHz/cm^2
  - Moderate R&D needed on module interconnection/mechanics/FE chip (FSSR2 or new chip)

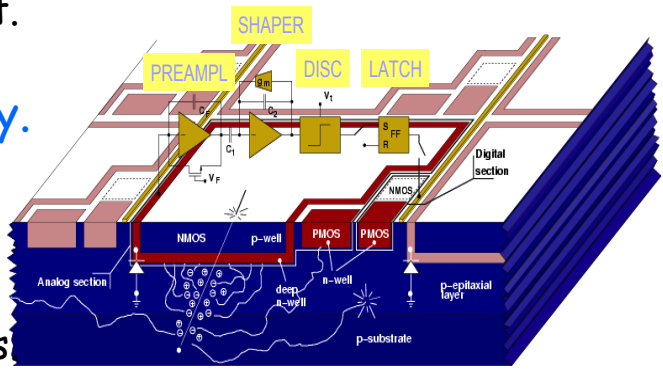


- **Hybrid Pixel option:** viable, although marginal.
  - Reduction of total material needed!
  - Reduction in the front-end pitch to 50x50 μm^2 with data push readout (developed for DNW MAPS)

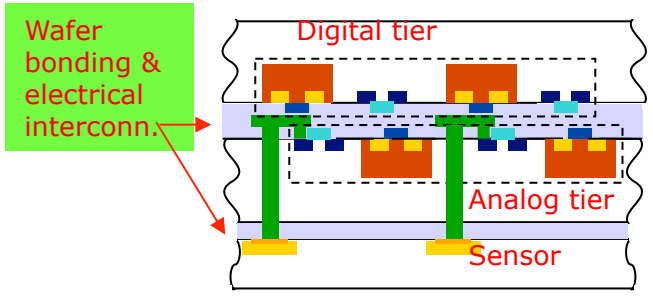
  → FE prototype chip (4k pixel, ST 130 nm) now under test.



- **CMOS MAPS option:** new & challenging technology.
  - Sensor & readout in 50 μm thick chip!
  - Extensive R&D (SLIM5-Collaboration) on
    - Deep N-well devices 50x50μm^2 with in-pixel sparsification.
    - Fast readout architecture implemented
  - CMOS MAPS (4k pixels) successfully tested with beams



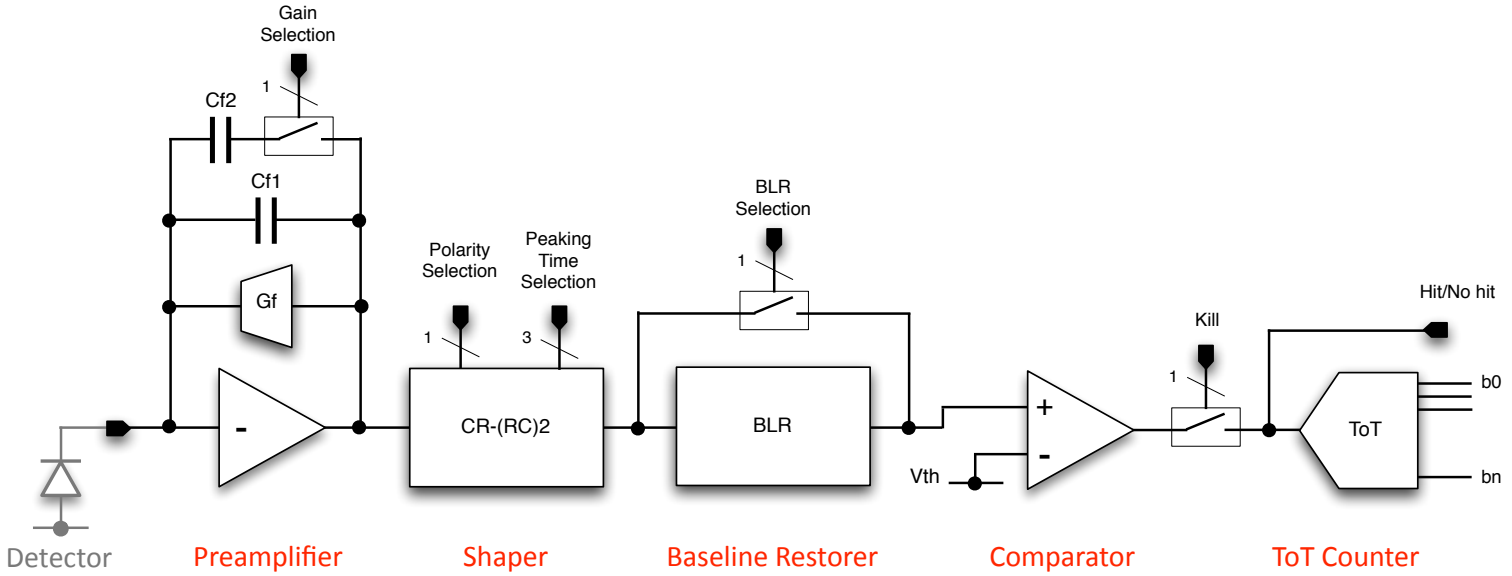
- **Thin pixels with Vertical Integration: reduction of material and improved performance.**
  - Two options are being pursued (VIPIX-Collaboration)
    - DNW MAPS with 2 tiers
    - Hybrid Pixel: FE chip with 2 tiers + high resistivity sensor



SVT Detectors

- **Baseline**
  - 5 layers of **silicon strip** modules (extended coverage w.r.t BaBar)
  - **Striplets** for layer0 @ R~1.5 cm.
  - Need to develop **2 new FE chips** for strips: existent chips do not match all the requirements: analog info needed, high rates in inner Layers (up to 1.4 MHz/strip in L0) & short shaping time (25-100ns), very long modules and long shaping time (0.5-1 us) in Layers 4-5.
- **Layer0 upgrade** for full luminosity run
  - SVT Mechanics will allow a **quick access/removal** of Layer0
  - Upgrading to thin **pixel sensors**
    - **More robust** against background **occupancy**
    - Several options investigated:
      - **CMOS MAPS**
      - **Hybrid Pixels**
      - **Vertical Integration…** reliable and stable ?
  - R&D continue in 2012 after TDR → pixel technology decision by 2013

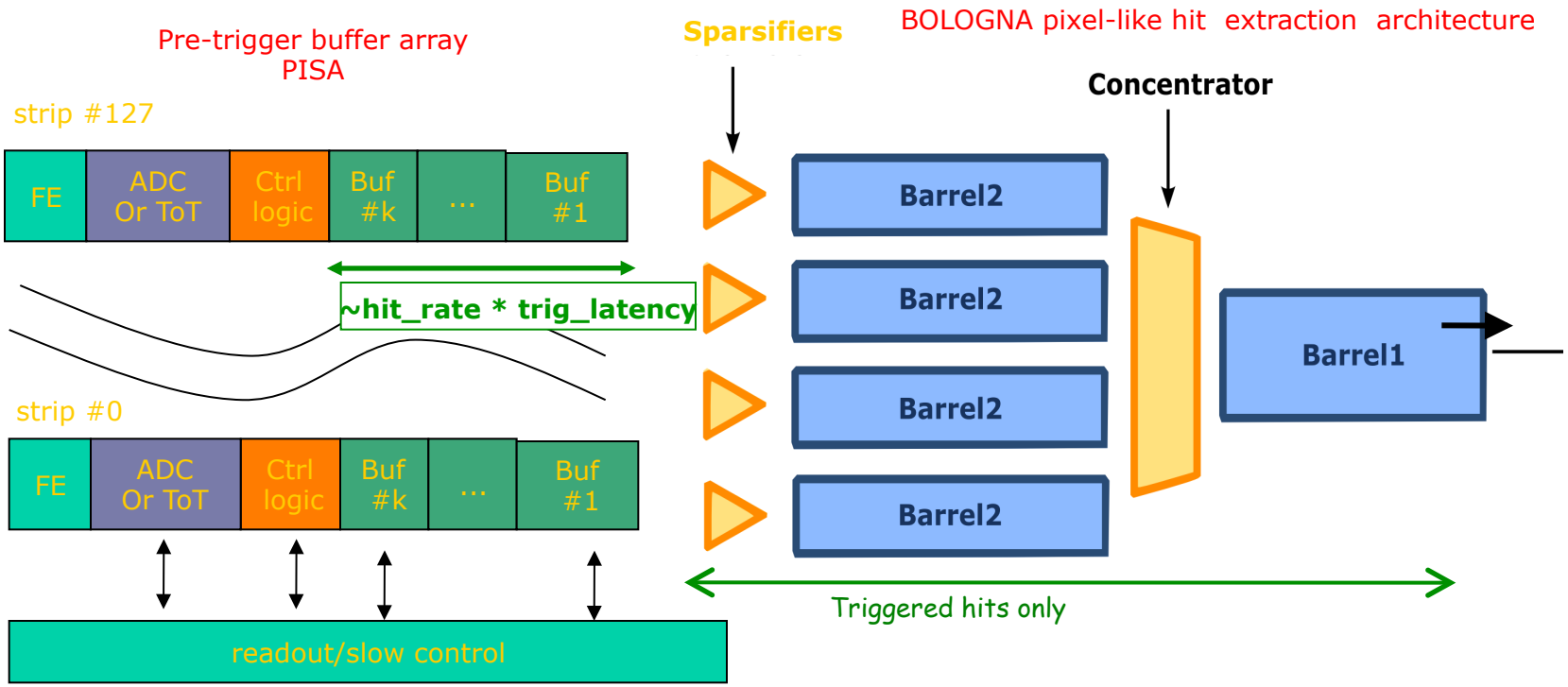
SuperB SVT analog front-end for strips in CMOS 130 nm



The analog channel consists of

- Charge-sensitive preamplifier with gain selection (1 bit)
- Unipolar semi-Gaussian shaper with polarity (1 bit) and peaking time (3 bit) selection options
- Symmetric baseline restorer to achieve baseline shift suppression, may be included or not (1 bit)
- Hit discriminator threshold circuit and comparator
- 3-4 bit analog-to-digital conversion will be performed by a Time-Over-Threshold (TOT) detection

Strip readout architecture



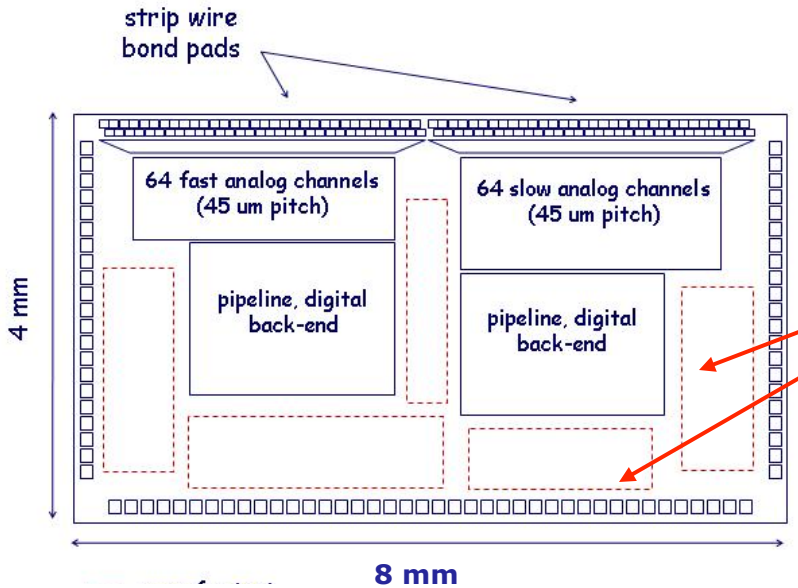
Adaptation of the readout architecture of APSEL-like pixel chips

SuperB strip FE chip development:

- **2 front-end chips** under development with different analog characteristics same digital architecture
- **Digital readout architecture** mostly inherited from pixel R&D
- Addition of **dedicated FIFOs** as hit buffers during trigger latency
- Whole digital readout architecture simulated (VHDL) with Monte Carlo hit generator: **100% digital efficiency** achievable even for high Layer0 rates even **including SF x5**.
- **Analog channel simulated**: shaping time reduction for some layers under evaluation to mitigate background impact:
- FE chip **work completed for TDR**

Next steps

- First FE chip submission with IBM 130 nm - Nov. 2012



Milestones for strip front-end development

- 2012: first test structures - 2 x 64 channels (fast and slow front-end), auxiliary blocks
- 2013: first fully operational prototype chip – 2 x 128 channels (fast and slow readout)
- 2014: production run
- Account for some contingency after the first or the second step

R&D on SVT Layer0 pixels

R&D on advanced pixel sensors for Layer0 is in progress:

- **INMAPS (CMOS 0.18 μm)**

  APSEL-like architecture, deep P-well and high resistivity epilayer to enhance charge collection; submission in preparation

- **CMOS 65 nm for hybrid pixels**

  Tests have begun on small prototypes (MAPS, fast front-end circuits)

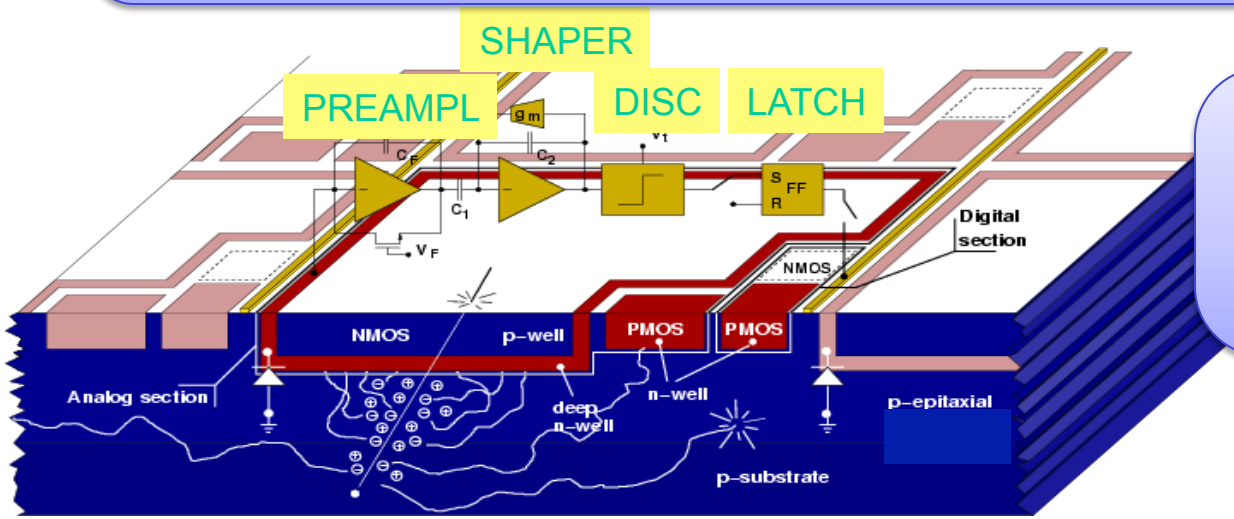
- **Pixels based on 3D integration**

  First Tezzaron/Chartered prototypes are presently in the 3D interconnection stage; a second submission is in preparation with a 3D MAPS and a 3D integrated circuit for high resistivity pixels

  An alternative 3D technology will be explored by AIDA

Deep Nwell (DNW) sensor concept

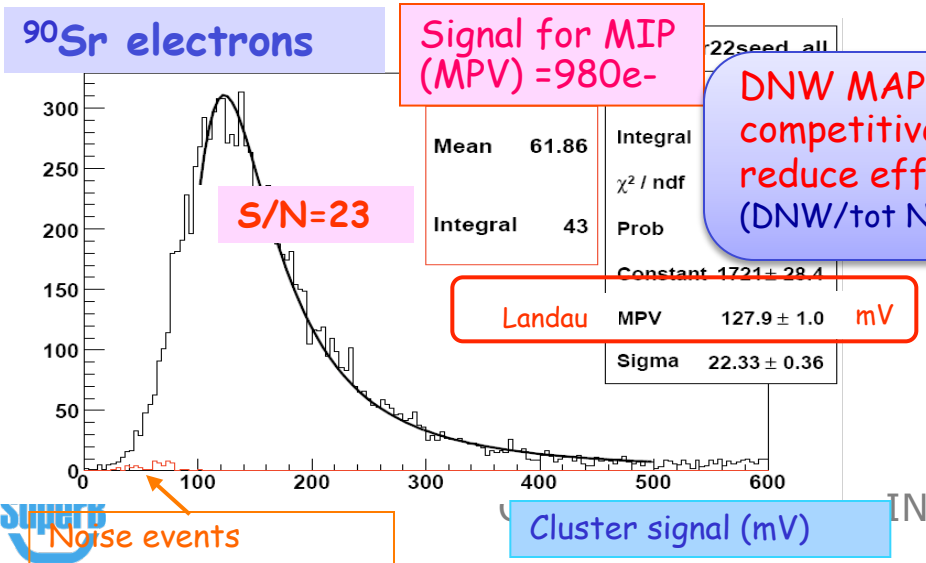
New approach in CMOS MAPS design compatible with data sparsification architecture to improve readout speed potential



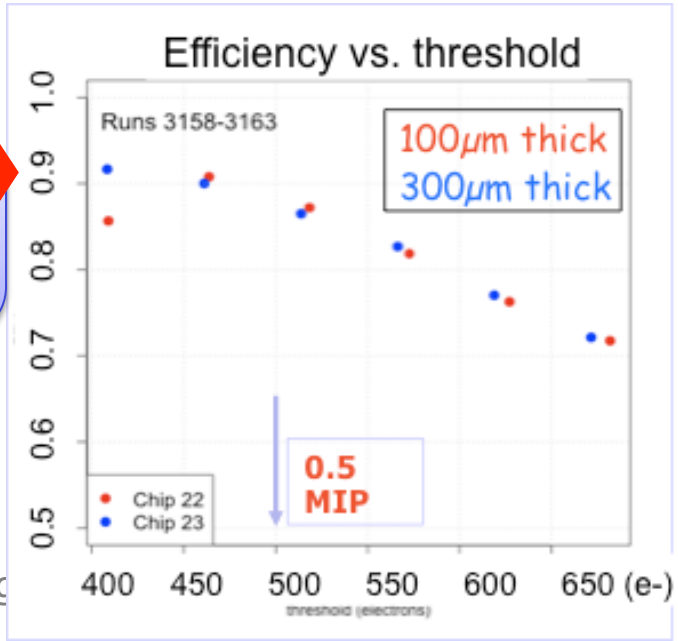
Developed in a 130 nm CMOS process, various different chips successfully tested with radioactive sources and beam

^{90}Sr electrons

Signal for MIP (MPV) =980e-



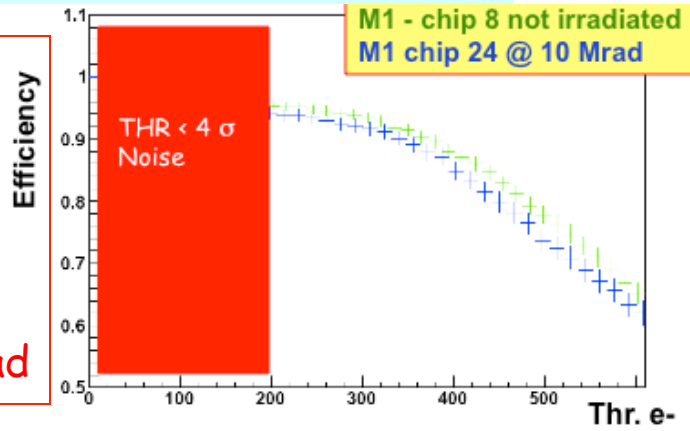
DNW MAPS effi 92%: competitive N-wells (PMOS) reduce efficiency: fill factor (DNW/tot N-well) ~ 90 %



DNW MAPS Radiation hardness

Irradiations with γ from ^{60}Co up to 10 Mrad

- beam test results for MAPS (3x3 matrix) with analog output (pre/post irrad)
  - Qcluster ~1040 e- for M1 (930 e- for M2)
  - S/N~15-20 depending on the electrode geometry
- modest reduction in collected charge and efficiency
  ENC increased by ~35% in chip irradiated up to 10 Mrad

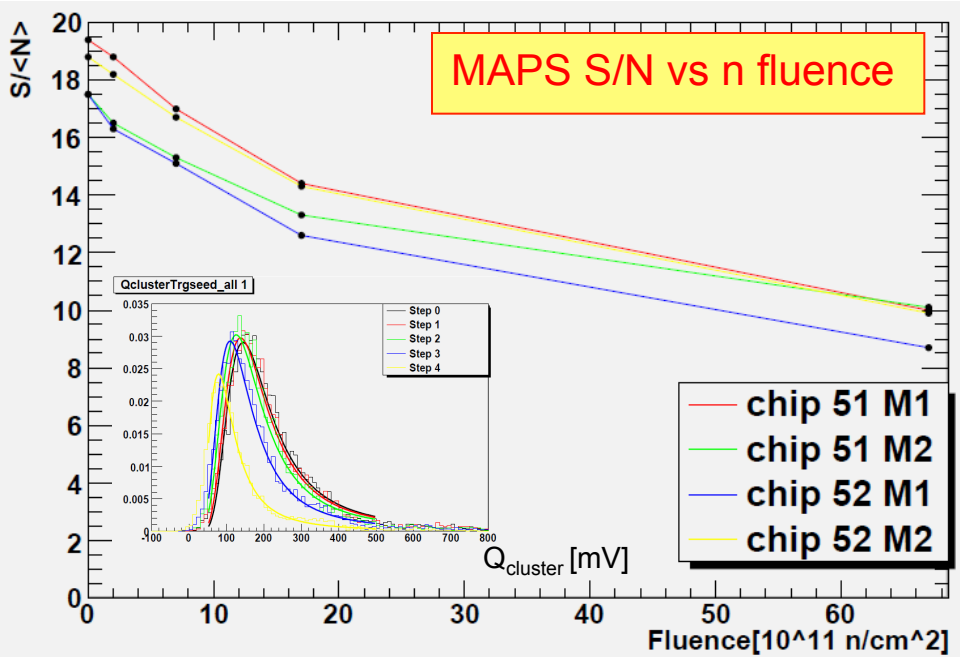


Irradiation with neutron up to ~ 7x10^{12}n/cm^2

- Expected fluence in Layer0 ~ 5x10^{12}n/cm^2/yr (no safety included)

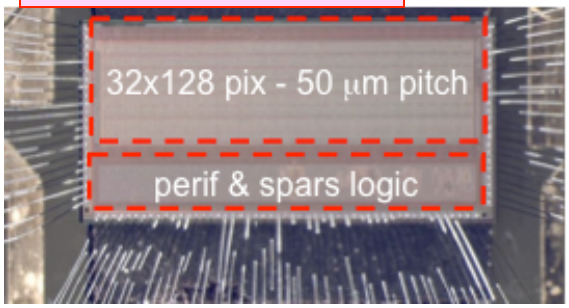
Results:

- Noise and gain not affected by neutron
- Signal degradation studied with β Sr^{90} source at each step:
- S/N → 10 in last step → limitation for application in Layer0
- Expect higher resistance with MAPS on high resistivity epitaxial layer



Evolution of DNW MAPS

APSEL4D – DNW MAPS



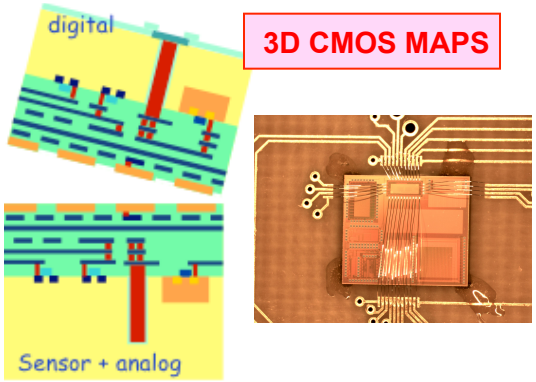
Charge collection efficiency main limitation of DNW MAPS for application in Layer0:

- Area of competive Nwell increses with more complex in-pixel logic (fast readout needed)
- Charge collection further reduced by radiation damage

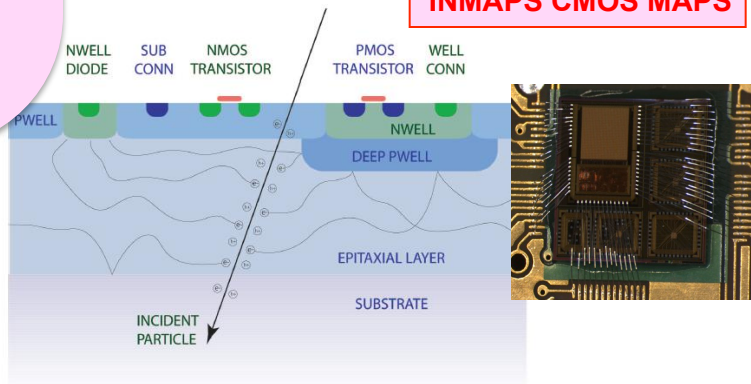
Two approaches to improve MAPS performance

- **3D MAPS with wertical integration:**
  - 2 tiers for sensor&analog + digital)
  - fill factor and efficiency can improves significantly even introducing more in-pixel logic
- **2D MAPS with INMAPS 180 nm process**
  - 4th well (deep Pwell), below competitive Nwells, used to avoid parassitic charge collection
  - high resistivity epitaxial layer also available for improved charge collection and radiation hardness!

3D CMOS MAPS



INMAPS CMOS MAPS

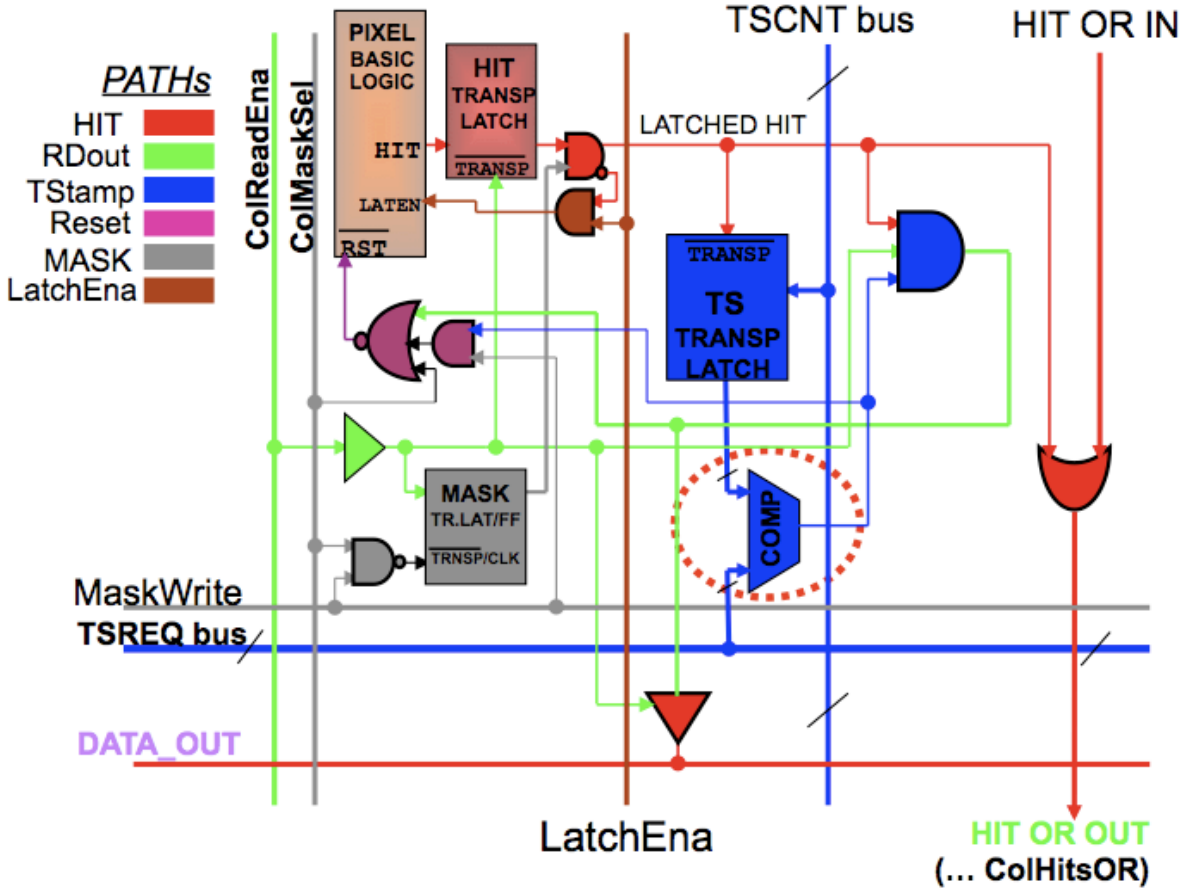


Readout architecture in the pixel cell: time-stamp latch and comparator for a time-ordered triggered readout

- **Complex in-pixel logic can be implemented without reducing the pixel collection efficiency; readout can be data push or triggered (only selected time stamps are read out).**

- Timestamp (TS) is broadcast to pixels and each pixel latches the current TS when fires.

- Matrix readout is TS ordered
  - A readout TS enters the pixel and an HIT-OR-OUT is generated for columns with hits associated to that TS
  - A column is read only if HIT-OR-OUT=1
  - DATA_OUT is generated for pixels in the active columns with hits associated to that TS.

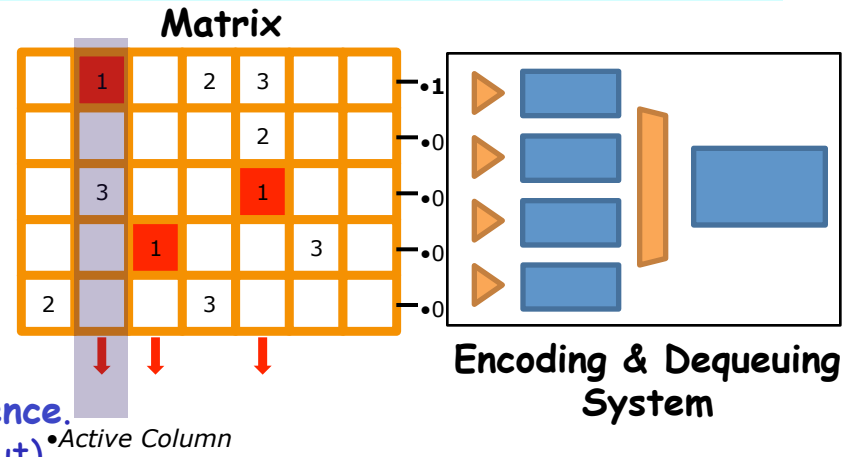


New Pixel Readout Architecture Features

- **In-pixel** Hit & Time Stamp Latch
- **TS request** to the matrix
- Pixel FastOR activates **IF** *latched TS == requested TS*
- Cascaded column FastORs
- **1 column sparsified in 1 clk cycle** (whatever the occupancy)
- **Only active-FastOR columns are enabled in sequence.** (i.e. 10 active column FastORs → 10 clk cycles readout)
- **Triggered** and **Data-Push** mode.
- **Implemented** in our INMAPS chips & ready for next 3D submissions

100 ns timestamp

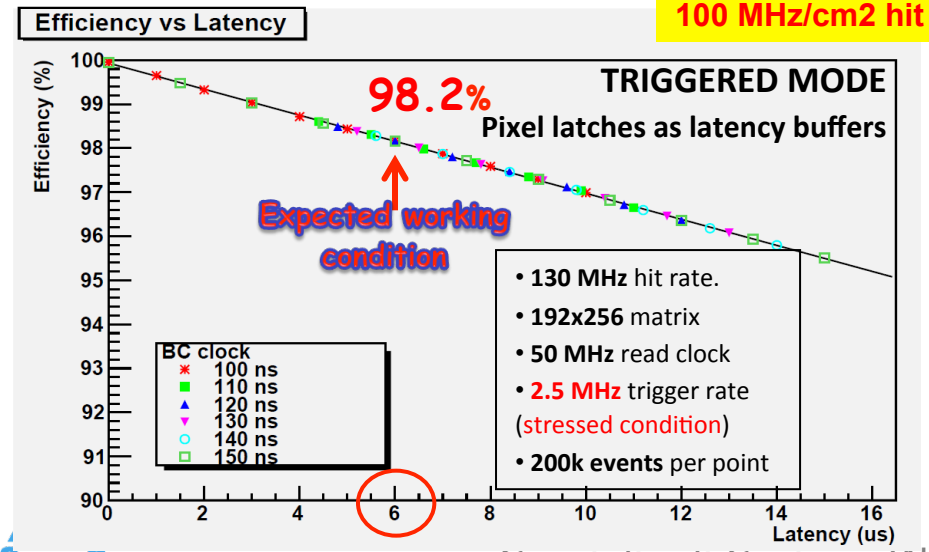
Requesting TS: 1

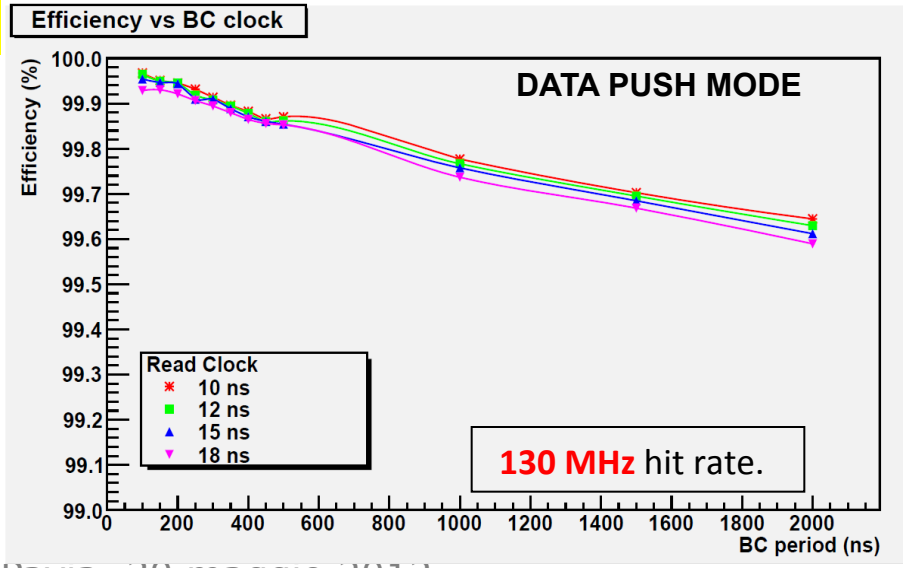


Simulations DO NOT take into account:

- **Sensor Efficiency**
- **Analog FE**

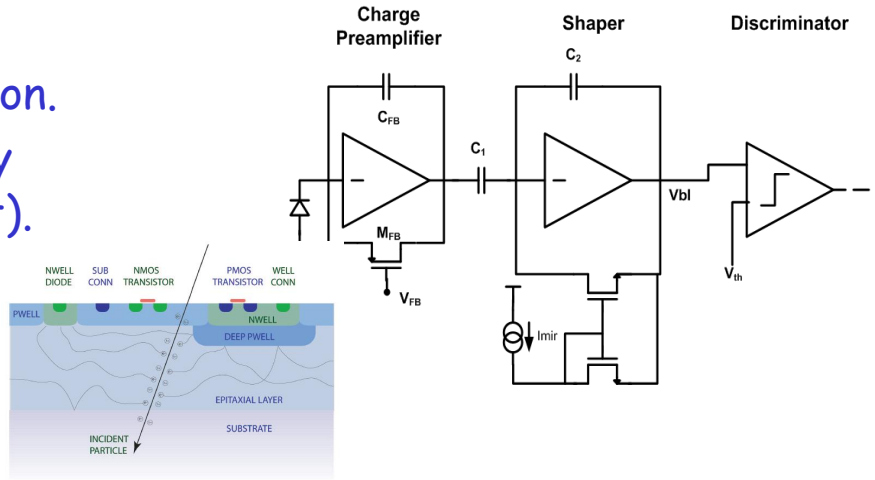
100 MHz/cm2 hit rate





INMAPS developments for SuperB Layer0

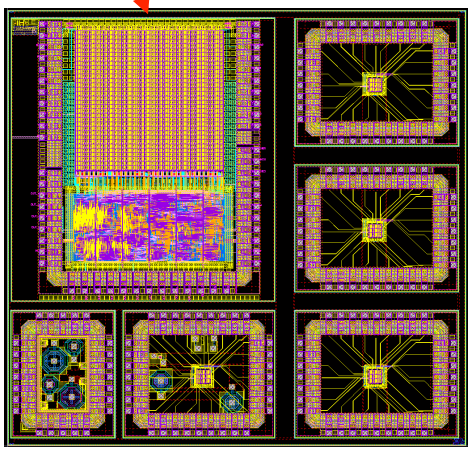
- Small N-well collecting diodes with small input capacitance and low power consumption.
- The forth-well prevents charge stealing by the parasitic N-wells (→efficiency benefit).
- Same analog and digital architecture as APSEL chips, to fit at best the high background rate of Layer0.

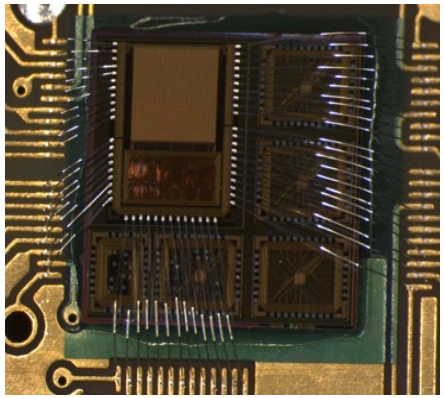


Apsel4well - Post Layout Simulation	
Charge sensitivity	930 mV/fC
t_p @ 800 injected electrons	240 ns
ENC (C_D = 30 fF)	26 e-
Threshold dispersion	23 e-
NLI (@ 2000e-)	1%
Analog Power consumption	18 μW/pixel
Pixel pitch	50 μm

32x32 matrix with sparsified digital readout architecture

3x3 analog matrices with different diodes configurations





INMAPS Chip (5x5 mm^2)

First chips under test now

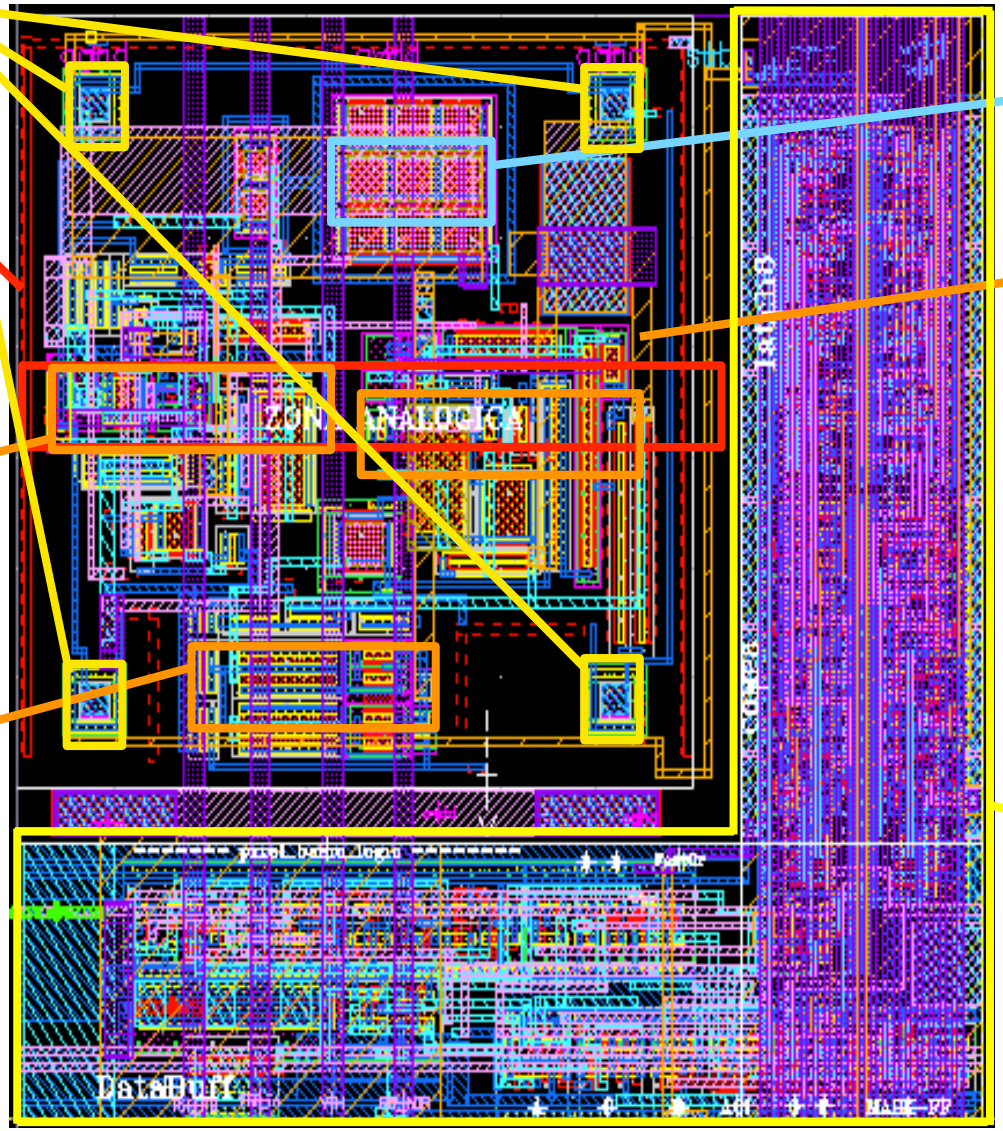
INMAPS CELL

Collecting diodes
1.5 x 1.5 μm^2

Analog section

Charge preamplifier

Discriminator



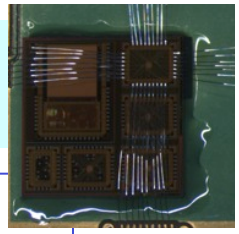
Differentiating capacitor (at the shaper input)

Shaper

Digital section

See S. Zucca's poster for more details on analog design

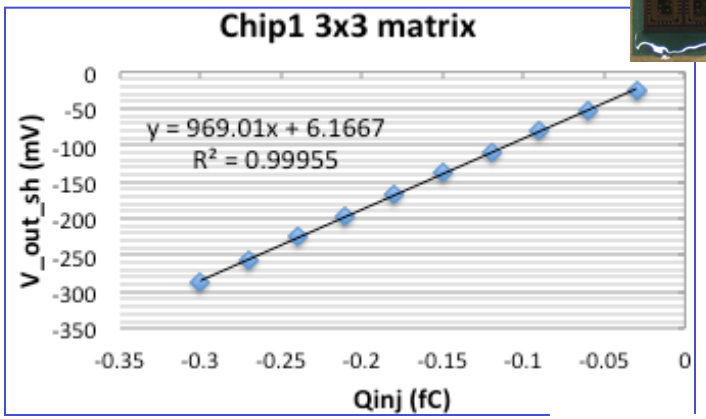
INMAPS RESULTS: 3x3 analog matrix



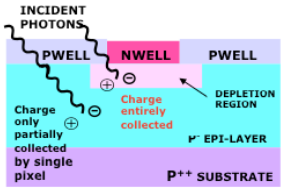
Preliminary

Noise and gain measured in 3x3 analog matrix in good agreement with PLS:

- ENC = 30 e- (~20% dispersion)
- Gain=920 mV/fC (~10% dispersion)

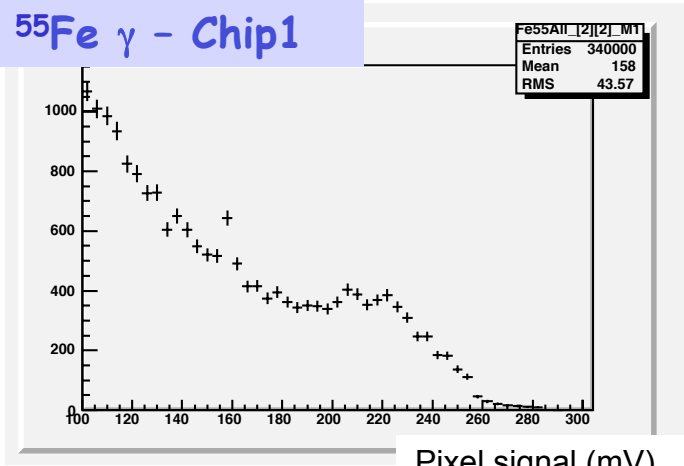


- Response to radioactive source
  - ^{55}Fe γ: 5.9keV foto peak hardly visible due to very small diode area.
    - Charge totally collected for γ interaction in the depleted volume below the diode. Partial collection elsewhere. End point (5.9 keV + 3 σ noise) used for gain evaluation (agreement within 10% with Cinj)



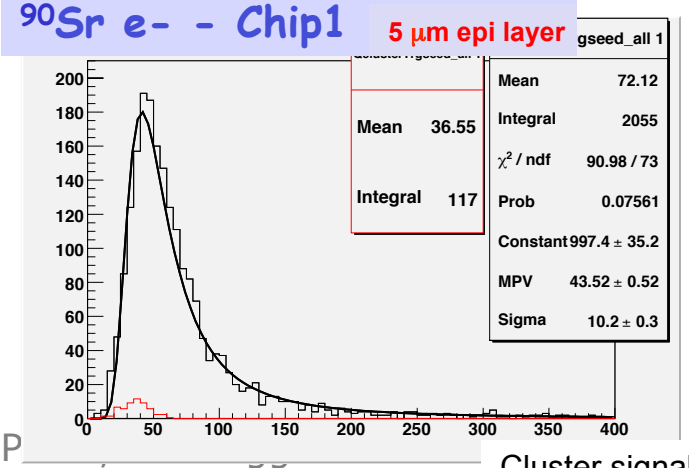
  - ^{90}Sr e- signal cluster: MPV ~ 350 e-, compatible with 5 um epi layer of first chips → chips with 12 um epi layer (standard & high resistivity) available in June.

^{55}Fe γ - Chip1



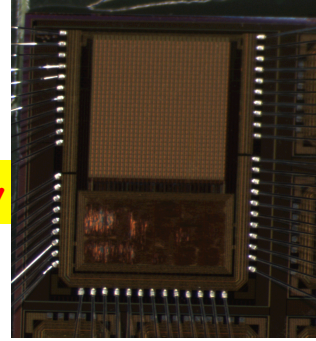
Pixel signal (mV)

^{90}Sr e- - Chip1 5 μm epi layer



Cluster signal (mV)

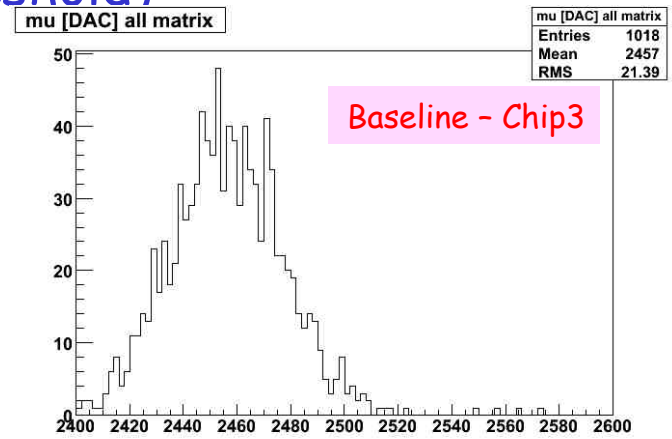
INMAPS 32x32 digital matrix



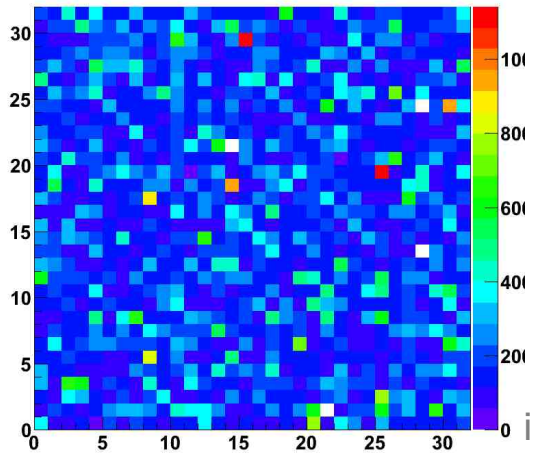
Preliminary

Noise and gain measured in pixels with Cinj and analog output

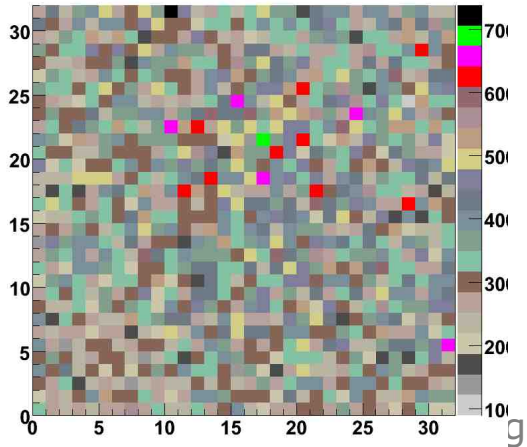
- ENC = 30 e- gain=680 mV/fC
- Threshold and noise dispersion inside matrix measured with noise scans (occupancy vs discriminator threshold)
  - Threshold dispersion = 7mV (~ 2 xσ_noise)
  - Noise (+gain) dispersion ~ 35-40%
  - Further tests to evaluate gain dispersion with Fe55 end point ongoing.
- Few dead pixels: ~ 0.3% (on 3 chips 32x32)



Noise hits – Chip3



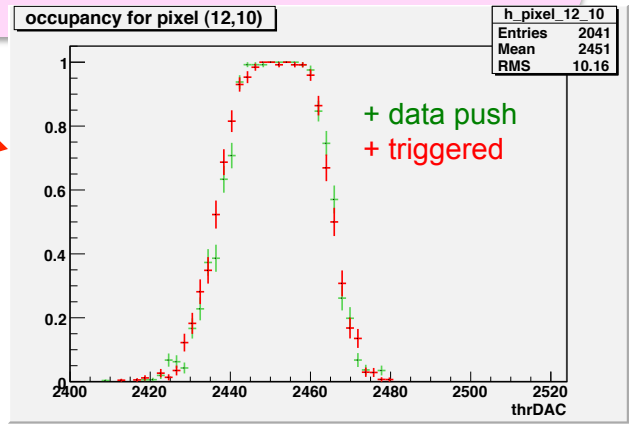
Sr90 hits – Chip1



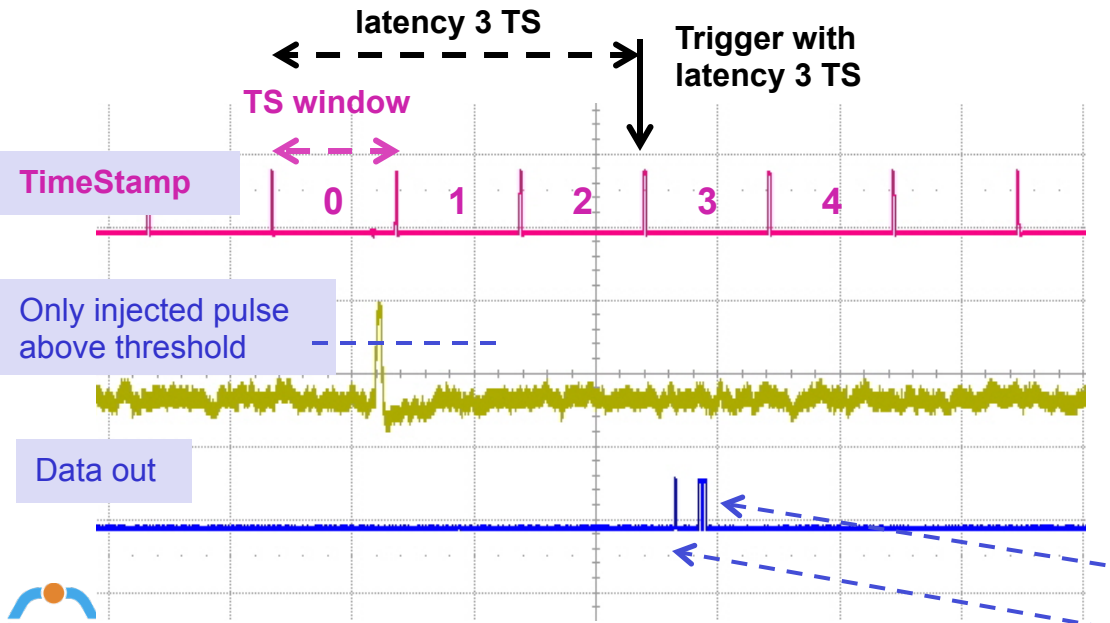
First test of the new readout architecture

- Standard functionality of new readout architecture verified in the two operation modes available on chip: data push (all TS readout) and triggered (only selected TS readout).

1. Threshold scans similar in both operation modes



2. Triggered mode also verified with specific test retrieving data injected at selected TS.



1. Pulse injection @ TS = 0
   → high threshold
   → no noise hits above threshold
2. Trigger arrives @ TS =2 with trigger latency setting = 3 TS
   → triggered event TS = 0
3. Data out stream info:
   - TS =0:1 fired pixel in submatrix1
   - TS =0: 0 pixels in submatrix0

SVT Attivita' 2012-2013

- Dopo il TDR entriamo in fase di costruzione.

Construction phases (from BaBar experience)

Design & prototype: 2013 baseline,
  - 2013 R&D on pixels for L0 upgrade: technology choice in 2013-2014?

Procure and Fabricate (+test) (2014-15)
  - 2015-2016 for pixel upgrade

Module Assembly & Det. Assembly (2016)
  - 2017 for pixel upgrade

Commissioning 2017
  - 2018 possible installation of pixel

- Per la baseline e' necessario costruire alcuni prototipi nel 2013 per finalizzare il design dell'intero rivelatore ed entrare in produzione con i vari componenti nel 2014
- Per i pixel del Layer0 nel 2013 continua R&D sulle varie opzioni per arrivare alla decisione sulla tecnologia nel 2013-14

Conclusions

- SVT TDR is almost completed
- R&D on advanced pixels is in progress, various technologies are being explored
- Concerning SVT strips, work on chip design has started (two different chips are needed) and a first submission is foreseen in November 2012.

Composizione gruppo ricerca

	Incarichi	Percentuale
RE Valerio	PO	50
RATTI Lodovico	RU	50
TRAVERSI Gianluca	RU	30
MANGHISONI Massimo	RU	80
GAIONI Luigi	Assegnista	100
MANAZZA Alessia	Dottorando	80
ZUCCA Stefano	Dottorando	40

Totale: 4.3 FTE