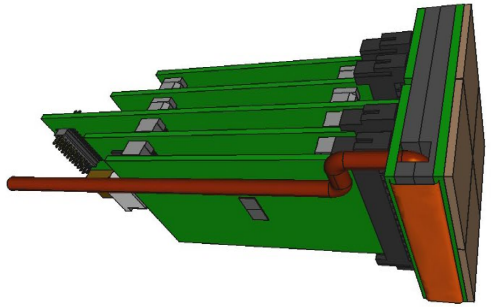
Scheda MasterLogic3

- Descrizione schema a blocchi
- Dettaglio sui singoli blocchi
- Protocollo di comunicazione RS485
- Descrizione Prototipo in corso di produzione

Il link con la documentazione del «MasterLogic3» e':
https://pandora.infn.it/public/c6f01b
password: MasterLogic3

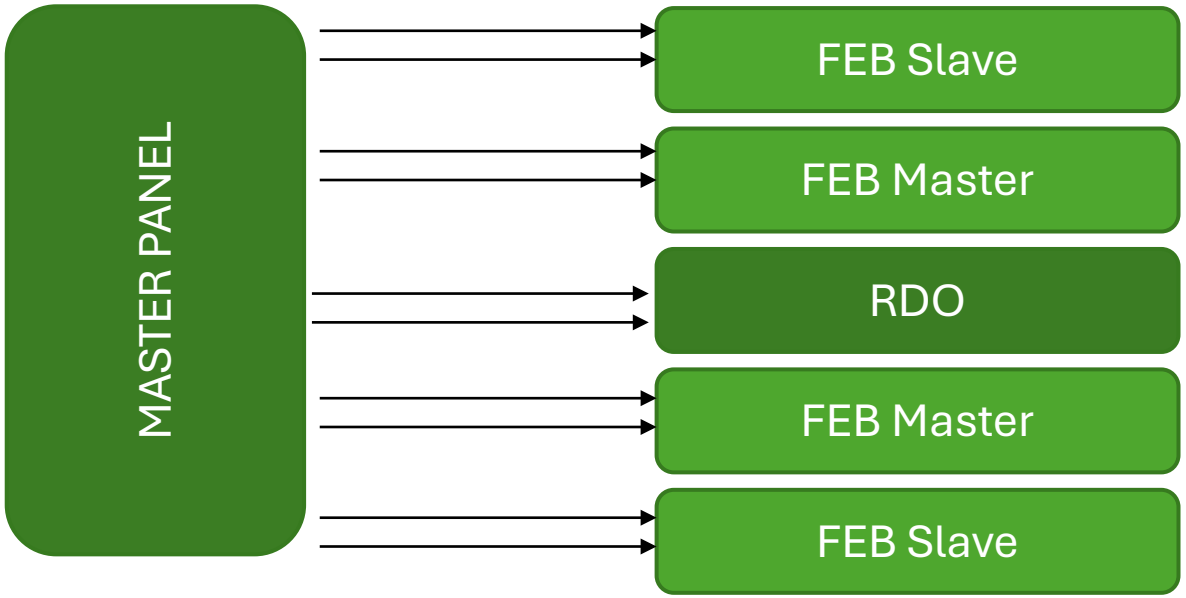
Il link con la documentazione del «MasterPanel small» e':
https://pandora.infn.it/public/05553a
password: MasterPanel_S

Schema a blocchi collegamento PDU al MasterPanel



208 PDU x settore

6 settori x 208 = 1248 PDU

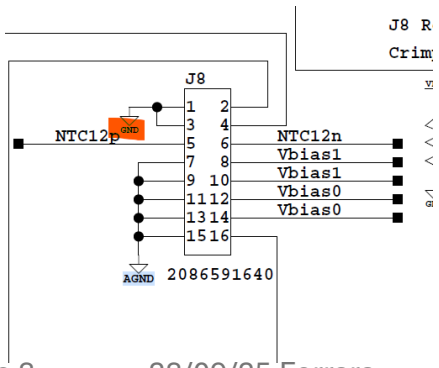


L'alimentazione dei 256 SiPM è suddivisa in 8 "segmenti" composti da 32 SiPM.

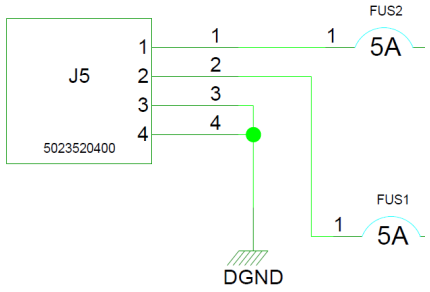
8x Vbias /Vannealing
4 Sensori temperatura

Alimentazione 1.4V Digitale
Alimentazione 2.7V Digitale
Alimentazione 1.4V Analaogica

Connettore FEB



Connettore RDO



Master Panel Block Diagram

Power supply distribution

Questi segnali non entrano nella MasterLogic3

1.4V Analog

1.4V Digital

2.7V Digital

The MasterPanel Board distribute Power supply to PDU:

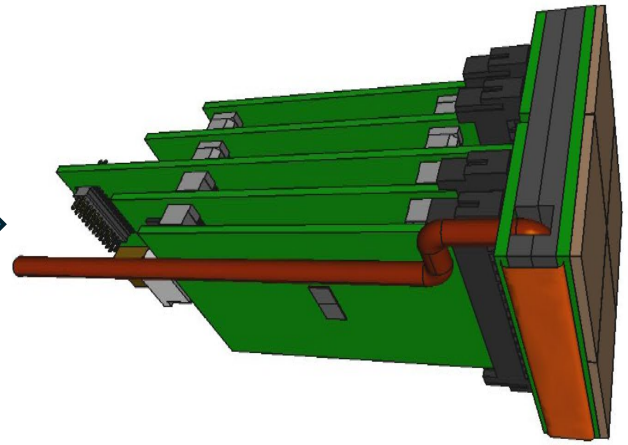
1.4V to RDO (digital)
2.7V to RDO (digital)

1.4V to FEBs (analog)
2.7V to FEBs(digital)
1.4V to FEBs (digital)

Without monitoring functions.
Only for connection function.

PDU
(Photo Detector Unit)

1 RDO Board
+
4 FEB Boards



MasterLogic3 Block Diagram

SiPM Voltage Bias supply distribution

PDU
(Photo Detector Unit)

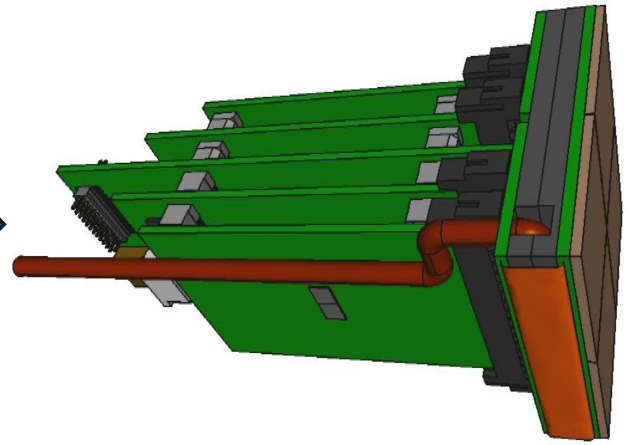
1 RDO Board
4 FEB Boards
256 SiPM

I and V measure

64V

The MasterLogic3 Board
regulate and distribute
VBias to PDU:

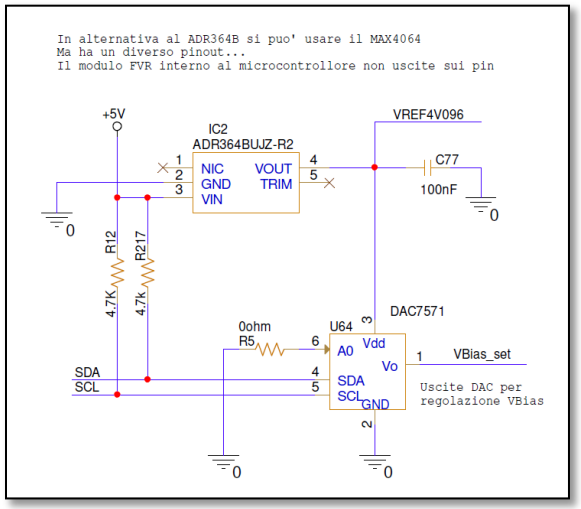
One Vbias regulator for PDU.
The current and output voltage is
measured for diagnostic purpose.



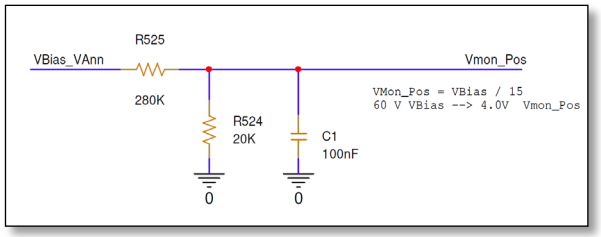
MasterLogic3 Block Diagram

- Range di regolazione VBias: 0 ... 61.44V (4.096V x15)
- Step regolazione VBias = 15mV
- Corrente massima circa 3mA
- Fondo scala misura Corrente = 0.4096mA
- Sensibilità misura Corrente = 0.1uA

VBias DAC



Misura VBias

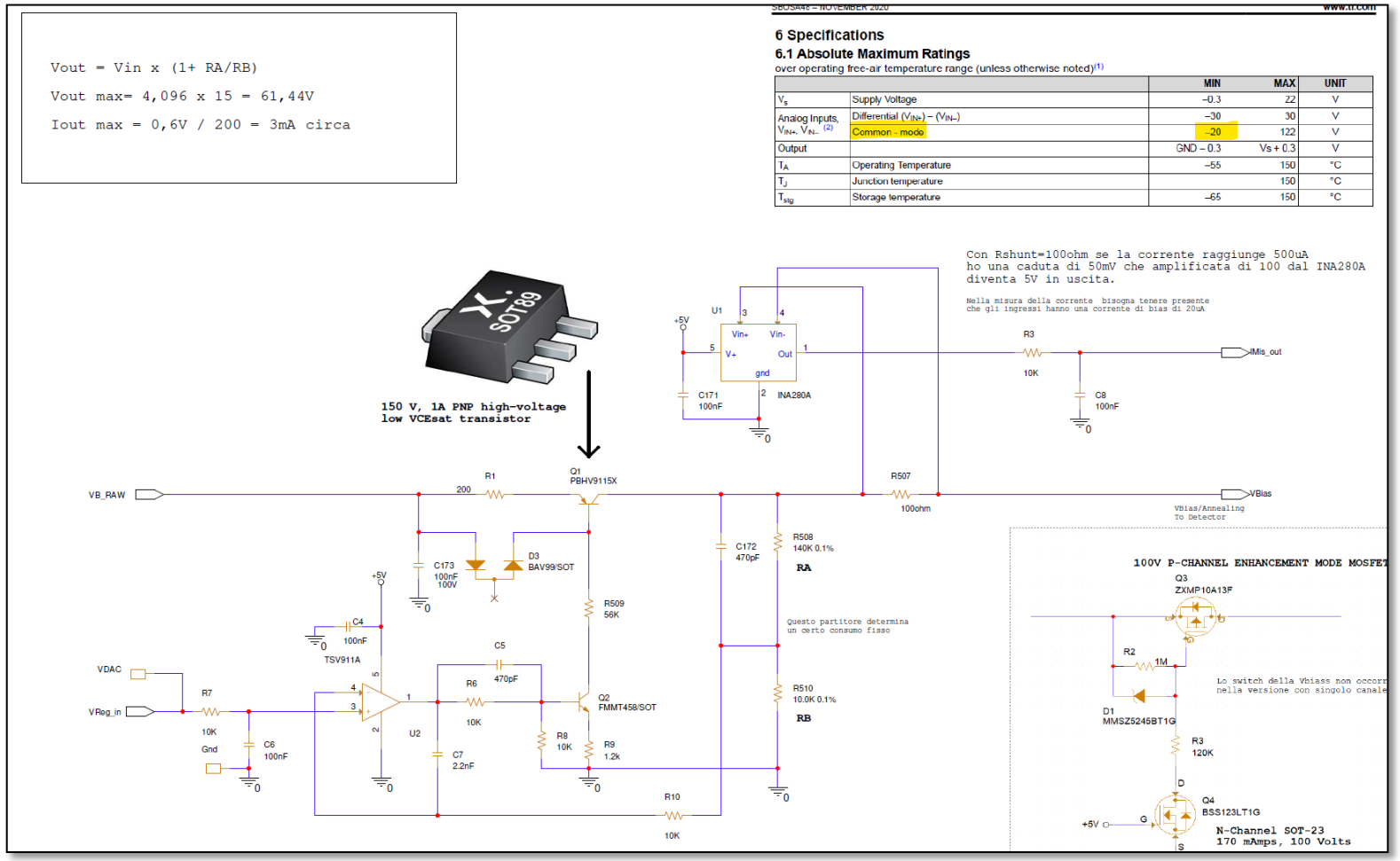


Regolatore VBias

Vout = Vin x (1+ RA/RB)

Vout max= 4,096 x 15 = 61,44V

Iout max = 0,6V / 200 = 3mA circa



MasterLogic3 Block Diagram

SiPM Voltage Annealing supply distribution

PDU
(Photo Detector Unit)

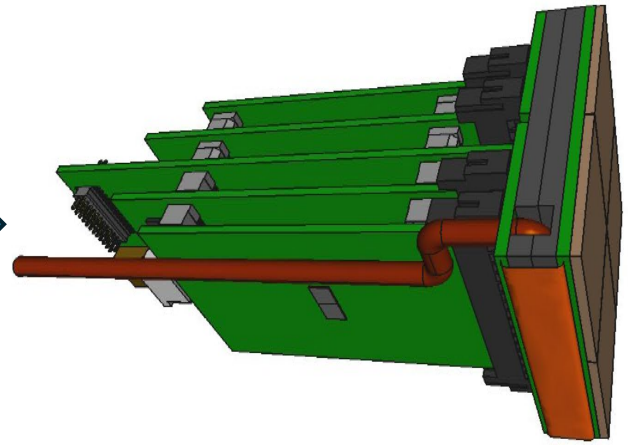
1 RDO Board
4 FEB Boards
256 SiPM

V measure

V Annealing
0 to -12V

The MasterLogic3 Board
Switch the Annealing current to SiPMs sectors.
Output voltage is measured for diagnostic purpose.

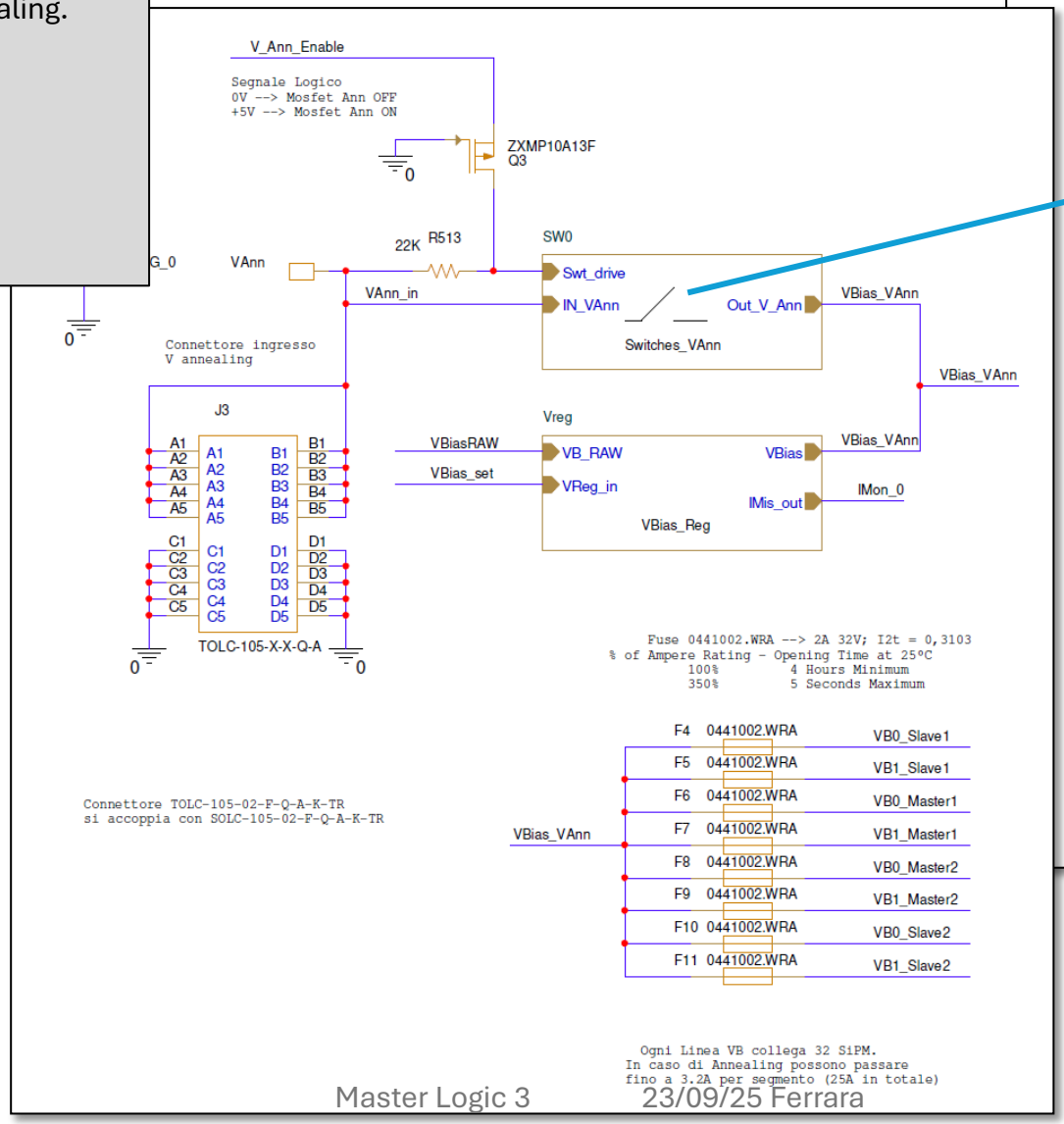
When Annealing process is active Vbias regulator is switched off.

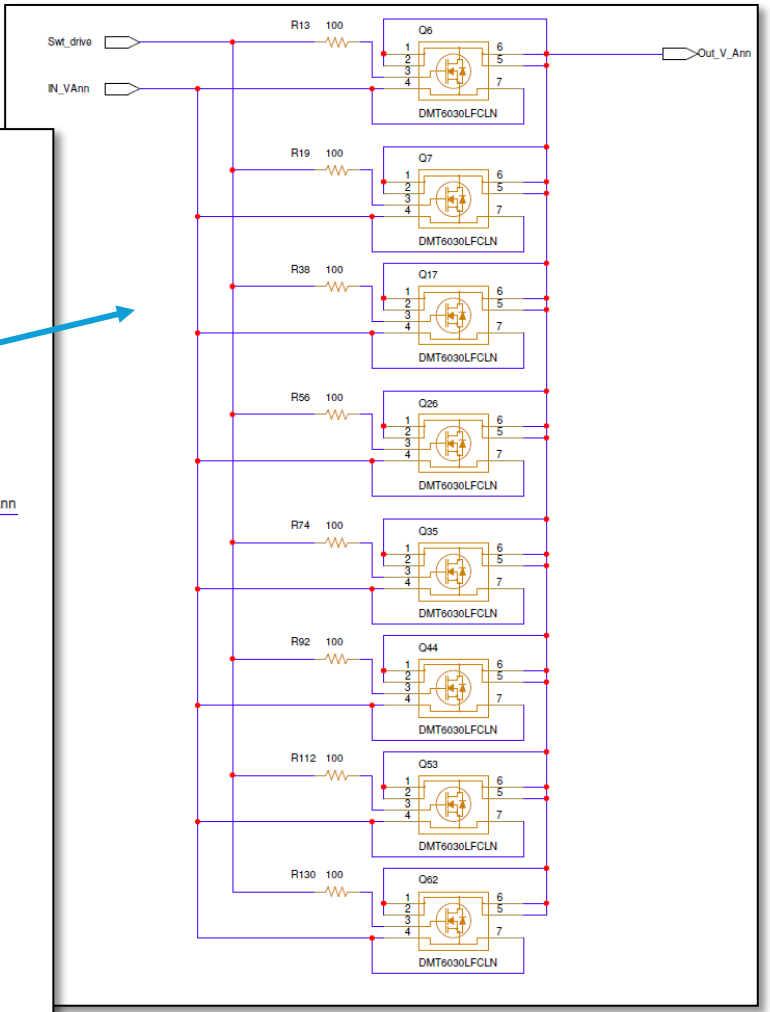


MasterLogic3 Block Diagram

- Viene eseguito l'Annealing di una PDU alla volta.
- 8 MOSFET commutano il collegamento della PDU verso la tensione dell'alimentatore di Annealing.
- Corrente massima prevista: 25A
- La Carrier e' divisa in 8 settori.
- Ogni settore e' protetto con un fusibile.
- Tensione misurabile fino a -10,24V

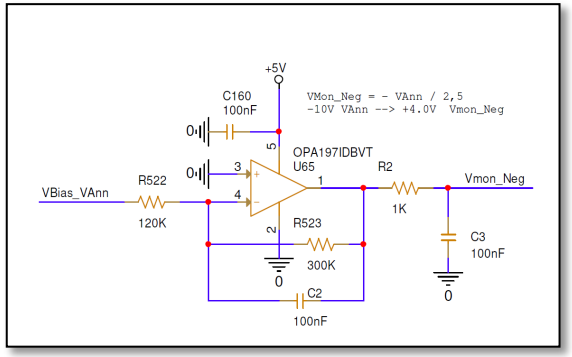
Schema di collegamento





MOSFETs per commutazione Annealing

Misura V Annealing

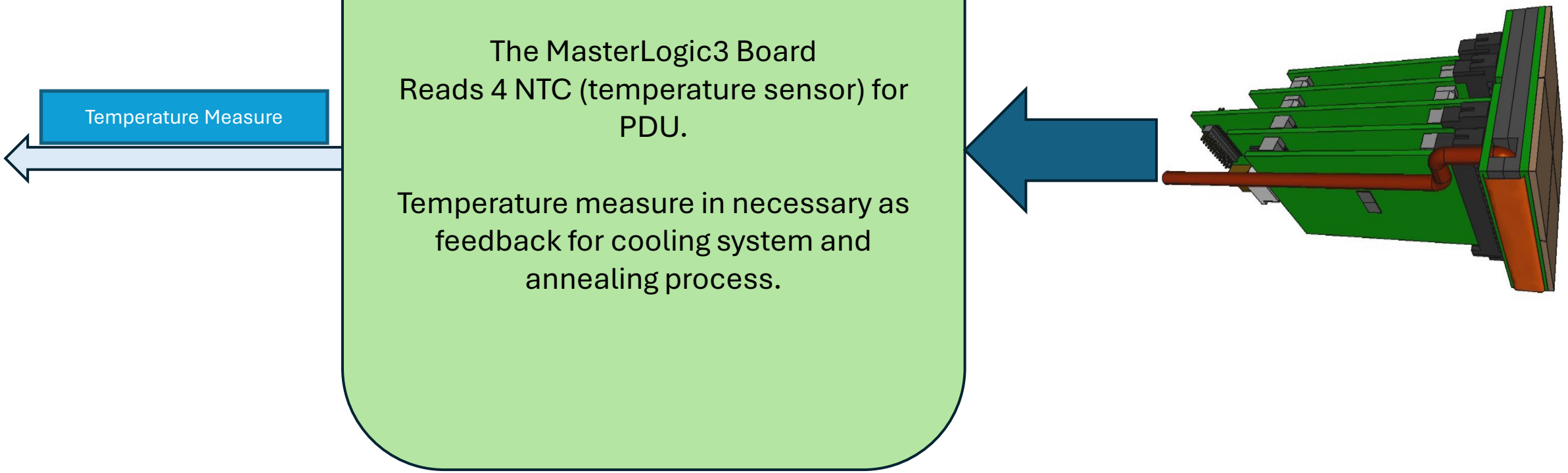


MasterLogic3 Block Diagram

Temperature Monitoring

PDU
(Photo Detector Unit)

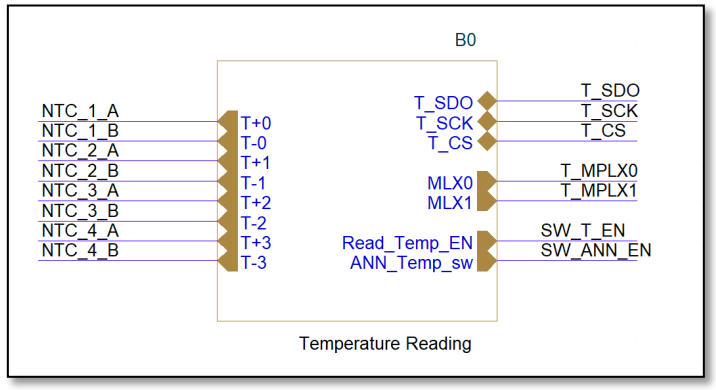
1 RDO Board
4 FEB Boards
256 SiPM



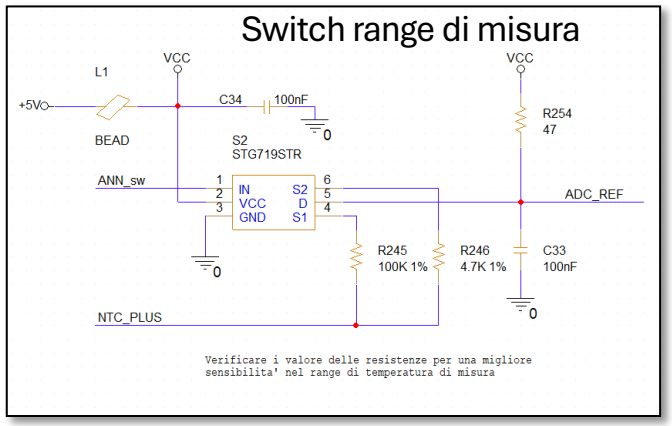
MasterLogic3 Block Diagram

- Stesso ADC 22bit (MCP3550-50) della MasterLogic2
- Aggiunto un multiplexer 4-1 per commutare fra i 4 NTC della Carrier
- Tempo di conversione 80ms: per leggere 4 sensori servono almeno 320ms
- Aggiunto circuito per verifica circuito di misura (ma forse inutile)

Schema top level

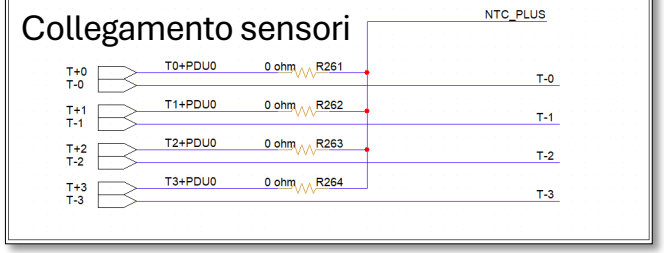


Switch range di misura

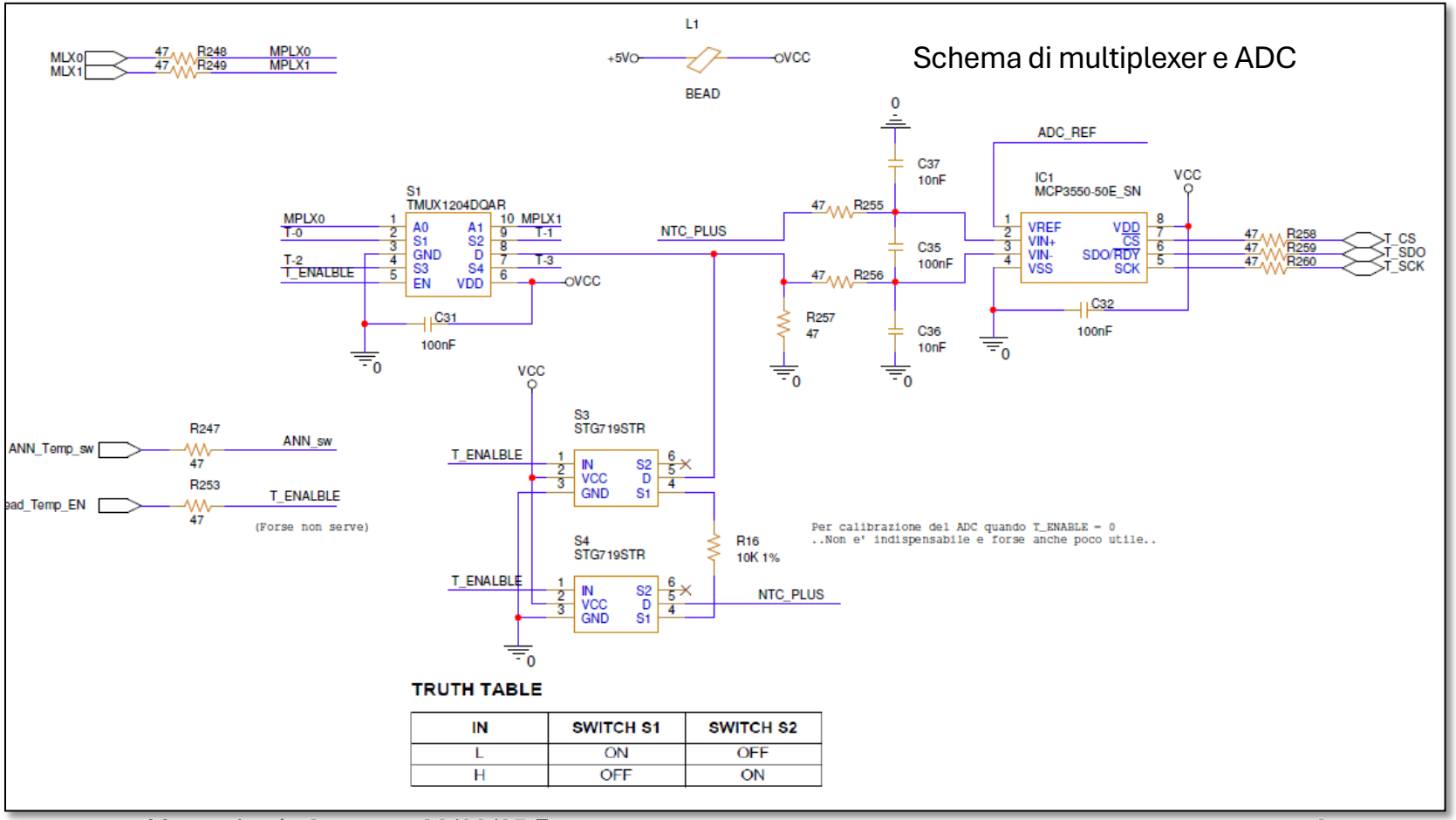


Segnali dai sensori di temperatura sulle Carrier

Collegamento sensori



Schema di multiplexer e ADC



TRUTH TABLE

IN	SWITCH S1	SWITCH S2
L	ON	OFF
H	OFF	ON

Master Panel Block Diagram

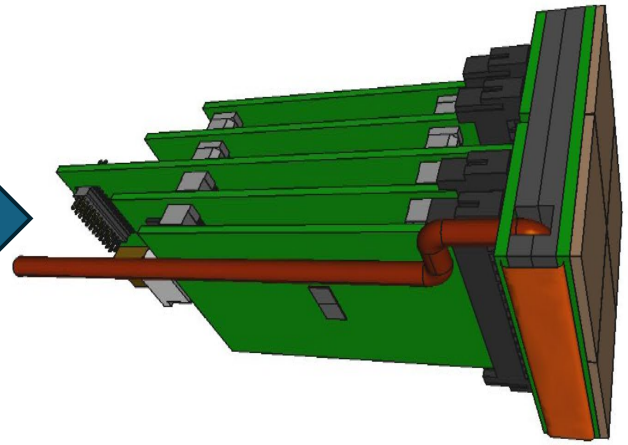
PDU
(Photo Detector Unit)

1 RDO Board
4 FEB Boards
256 SiPM

RS485
BUS

A microController PIC18F27Q43-I_STX
perform:
- voltage regulations,
- V Annealing switch,
- current measurements,
- voltage measurements,
- and temperature measurements.

Data transit on an RS485 connection.



MasterLogic3 Block Diagram (RS-485)

5 Product Selection Guide

PART NUMBER	DUPLEX	SIGNALING RATE	NODES	CABLE LENGTH
SN65HVD1785	Half	115 kbps	Up to 256	1500 m
SN65HVD1786	Half	1 Mbps	Up to 256	150 m
SN65HVD1787	Half	10 Mbps	Up to 64	50 m

1 Features

- Bus-Pin Fault Protection to:
  - > ±70 V ('HVD1785, 86, 91, 92)
  - > ±30 V ('HVD1787, 93)
- Common-Mode Voltage Range (–20 V to 25 V) More Than Doubles TIA/EIA 485 Requirement
- Bus I/O Protection
  - ±16 kV JEDEC HBM Protection
- Reduced Unit Load for Up to 256 Nodes
- Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions
- Low Power Consumption
  - Low Standby Supply Current, 1 µA Typical
  - I_{CC} 5 mA Quiescent During Operation
- Power-Up, Power-Down Glitch-Free Operation

2 Applications

- Designed for RS-485 and RS-422 Networks

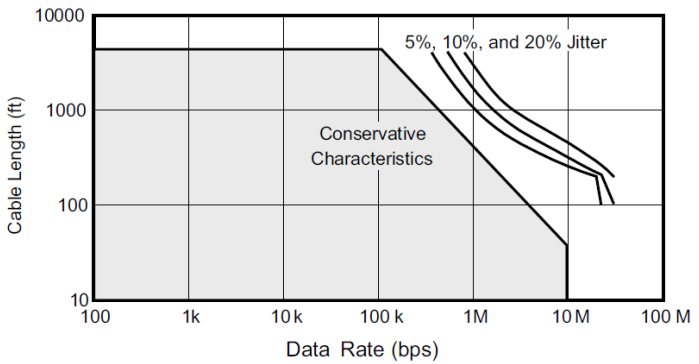


Figure 10-3. Cable Length vs Data Rate Characteristic

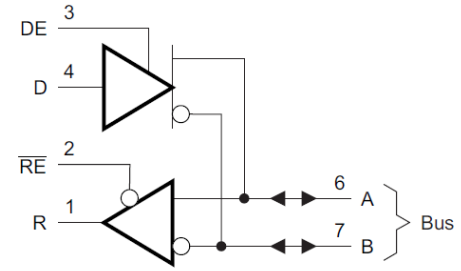


Figure 9-1. Half-Duplex Transceiver

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

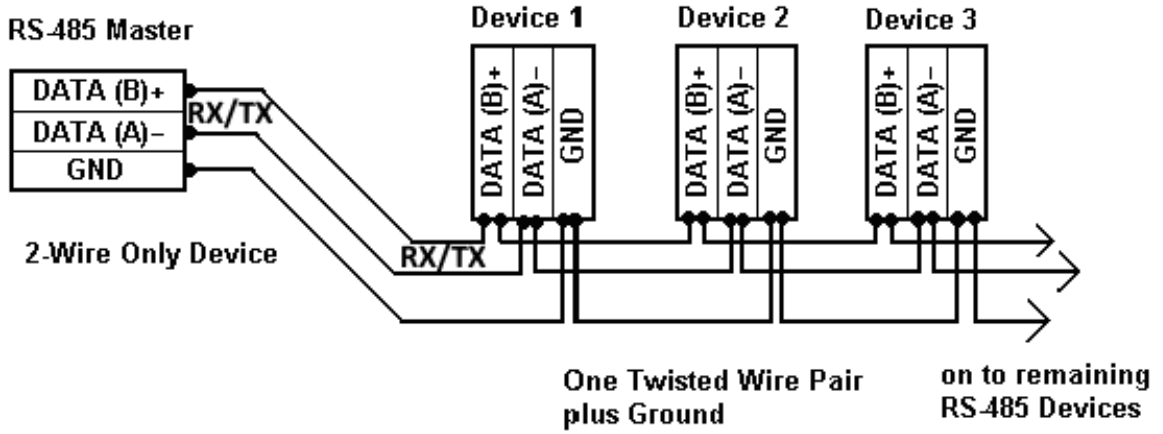
Protocollo di comunicazione

- Il “Computer” incomincia la comunicazione con “$” seguito dall’indirizzo della scheda target in HEX (3 caratteri).
- Poi vi e’ un carattere che identifica il comando (Lettura, Scrittura, Ecc…)
- Poi vi sono gli eventuali dati in esadecimale relativi al comando
- ? Cheksum ?
- Infine la terminazione del pacchetto di dati: «\n»

$	A	A	A	X	n	n	n	n	n	….	\n

- La scheda «MasterLogic3» risponde con «#» seguito dal proprio indirizzo
- Poi vi e’ lo stesso carattere del comando ricevuto
- Gli eventuali dati in esadecimale in risposta al comando
- ? Cheksum ?
- La terminazione del pacchetto di dati: «\n»
- Il carattere «#» e il carattere del comando ricevuto ripetuto durante la risposta potrebbero non essere indispensabili

#	A	A	A	X	n	n	n	n	n	….	\n



- **Solo** Il “Computer” puo’ incominciare la comunicazione con le MasterLogic3
- Il computer deve attendere la risposta della ML3 prima di iniziare una nuova comunicazione (…con timeout per evitare blocco)
- Ogni scheda ML3 deve avere un indirizzo diverso (primo carattere indentifica sestante?)
- Esiste un indirizzo Globale a cui tutte le ML3 rispondono ma con un delay proporzionale all’indirizzo per evitare collisioni di dati.

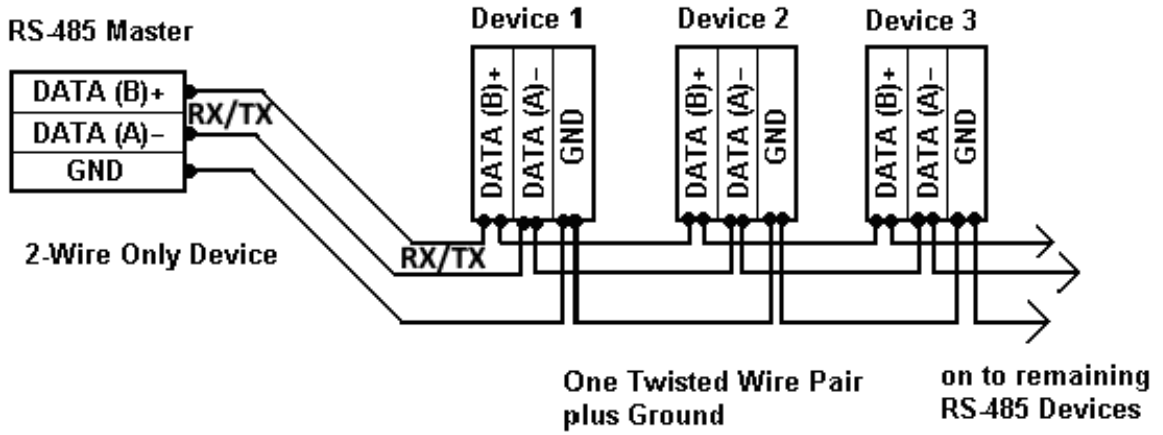
Protocollo di comunicazione

FUNZIONI DA IMPLEMENTARE

- Lettura Versione sw, ID scheda
- Lettura Stato Annealing / Normale
- Lettura Tensione Vbias Positiva
- Lettura Tensione Vbias Negativa
- Lettura Corrente VBias Positiva
- Lettura temperatura sensori CARRIER
- Lettura stato uControllore (temp. Vref, Vcc, ecc)

- Cambio Modalità fra Annealing / Normale
- Scrittura Tensione VBias
- Programmazione ID scheda
- Memorizzazione impostazioni di default
- Impostazioni correzione Guadagno/Offset VBias

- Varie ed eventuali



Features

- Operating Speed:
  - DC – 64 MHz clock input
  - 62.5 ns minimum instruction cycle
- Six Direct Memory Access (DMA) Controllers:
- Vectored Interrupt Capability:
  - Selectable high/low priority
  - Fixed interrupt latency of three instruction cycles
- 127-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):

Memory

- Up to 128 KB of Program Flash Memory
- Up to 8 KB of Data SRAM Memory
- 1024 Bytes Data EEPROM
- Memory Access Partition: The Memory can be partitioned into:
  - Application Block
  - Boot Block
  - Storage Area Flash (SAF) Block
- Programmable Code Protection and Write Protection
- Device Information Area (DIA) Stores:
  - Temperature indicator factory calibrated data
  - Fixed Voltage Reference measurement data
  - Microchip unique identifier
- Device Characteristics Information (DCI) Area Stores:
  - Program/erase row sizes
  - Pin count details
  - EEPROM size
- Direct, Indirect and Relative Addressing modes

Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 5.5V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Digital Peripherals

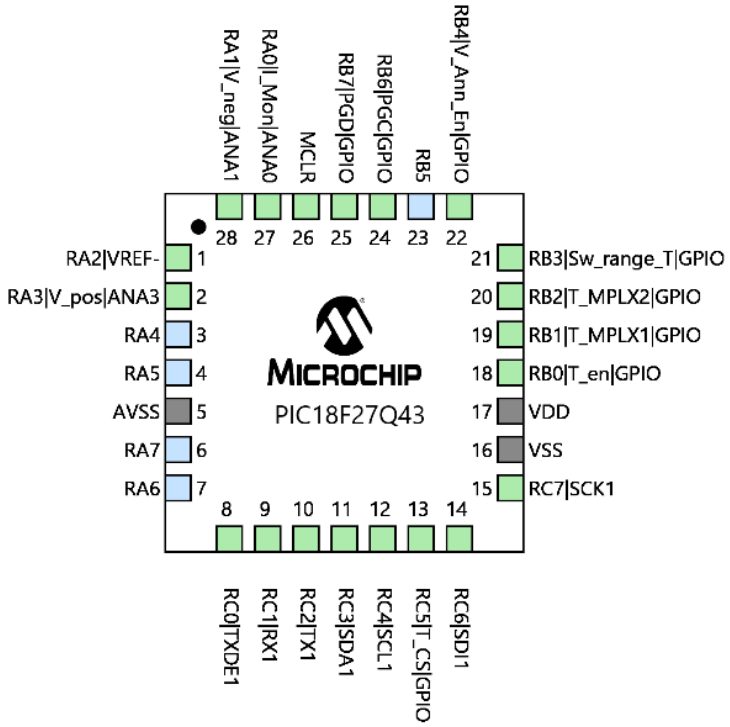
- Three 16-Bit Pulse-Width Modulators (PWM):
- Four 16-Bit Timers (TMR0/1/3/5)
- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT)
- Eight Configurable Logic Cell (CLC):
- Three Complementary Waveform Generators (CWG)

Three Capture/Compare/PWM (CCP) modules:

- Three Numerically Controlled Oscillators (NCO):
- Signal Measurement Timer (SMT):
- Data Signal Modulator (DSM):
- Programmable CRC with Memory Scan:
  - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
  - Calculate 16-bit CRC over any portion of Program Flash Memory
- Five UART modules:
- Two SPI modules:
- One I2C module, SMBus, PMBus™ Compatible
- 25 I/O pins (PIC18F25/26/27Q43)
- Analog-to-Digital Converter with Computation (ADCC):
  - Up to 140 ksps
  - Automated math functions on input signals:
    - Averaging, filter calculations, oversampling and threshold comparison
- 8-Bit Digital-to-Analog Converter (DAC):
  - Buffered output available on two I/O pins
  - Internal connections to Analog-to-Digital (ADC) and Comparators
- Two Comparators (CMP):
- Zero-Cross Detect (ZCD):
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels
- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequencies up to 64 MHz

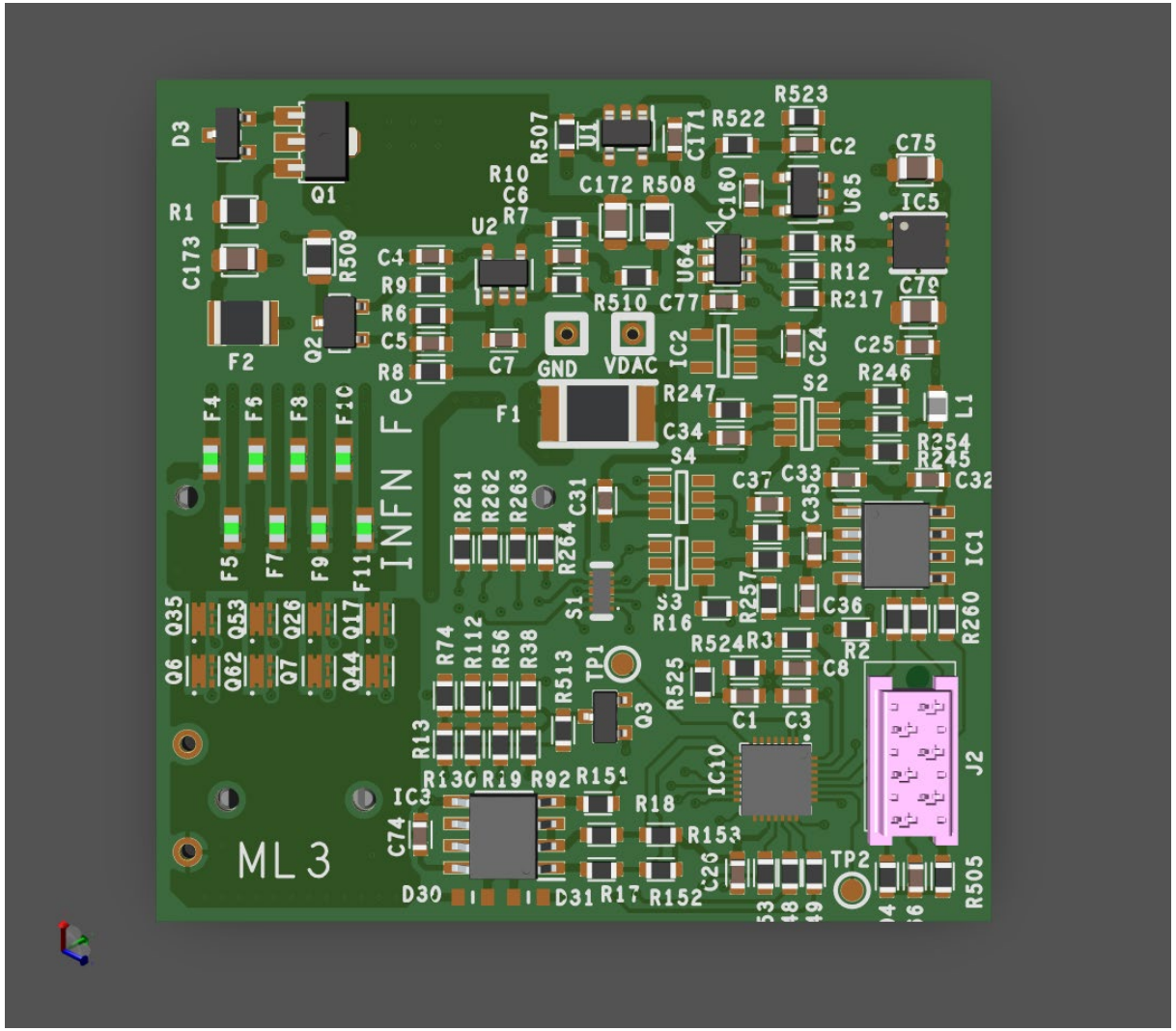
Il uControllore dellaMasterLogic3

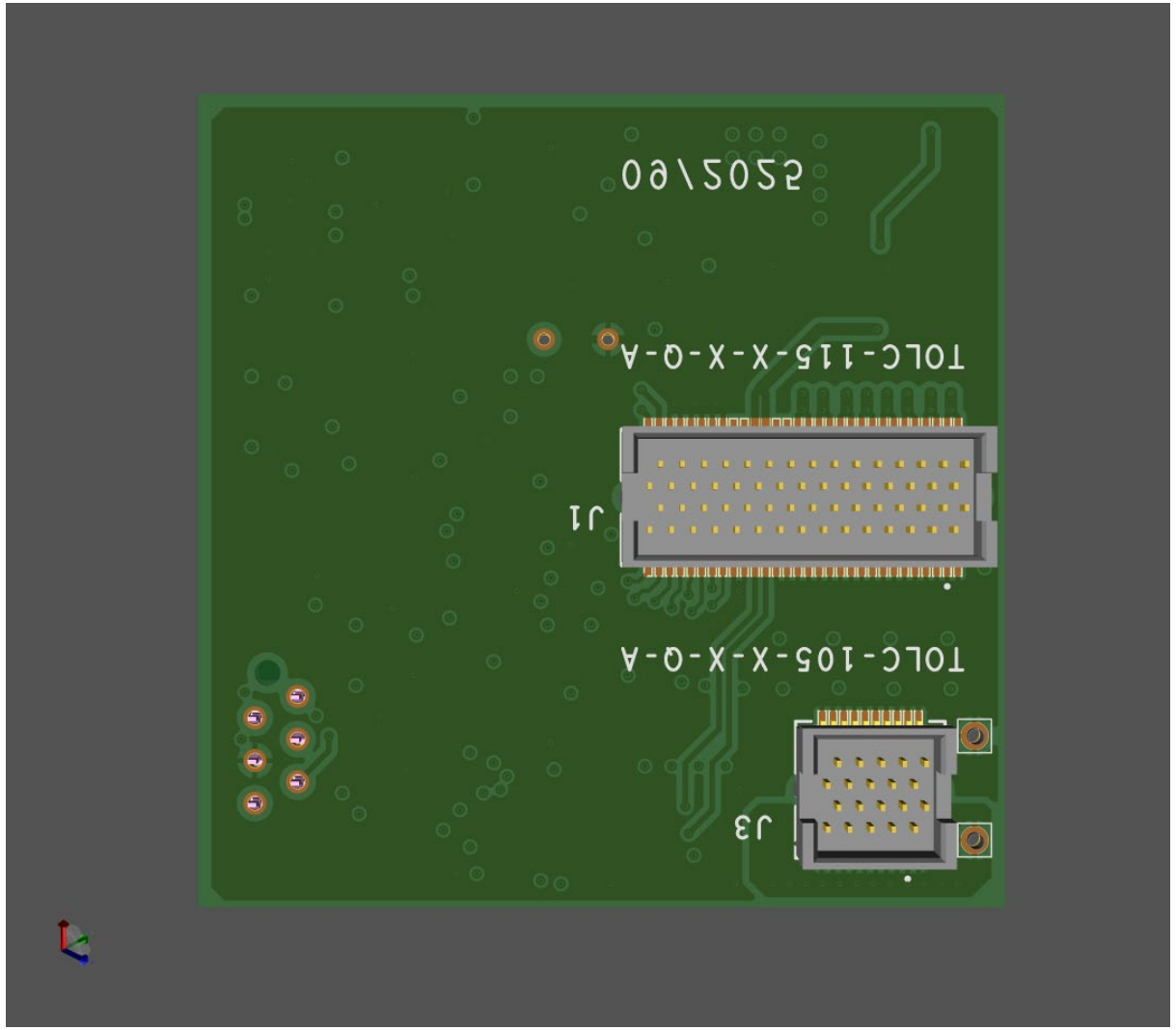
28-Pin, Low-Power, High-Performance Microcontroller with XLP Technology PIC18F27Q43



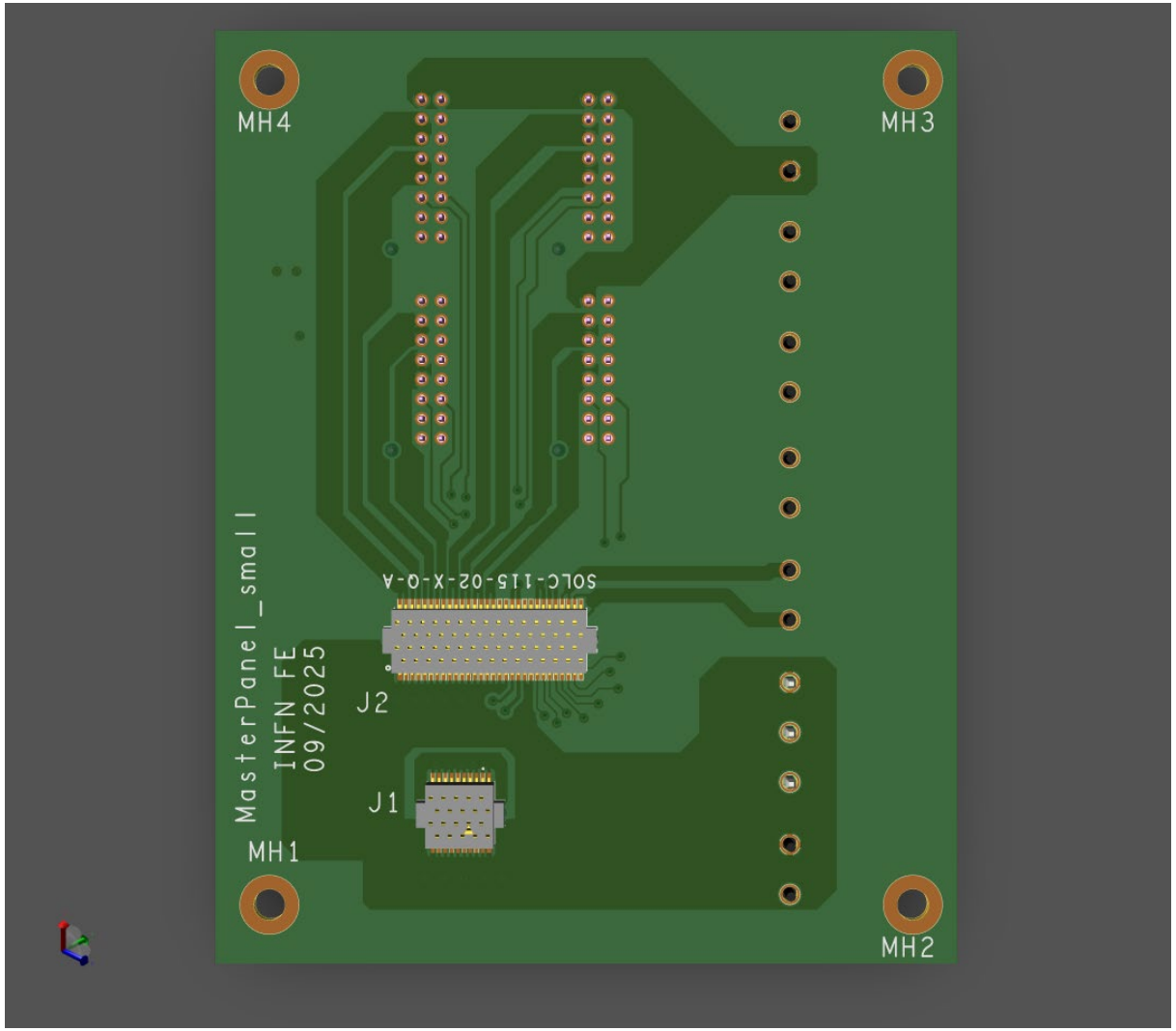
28-Lead Very Thin Plastic Quad Flat, No Lead (STX) - 4x4x1.0 mm Body [VQFN]

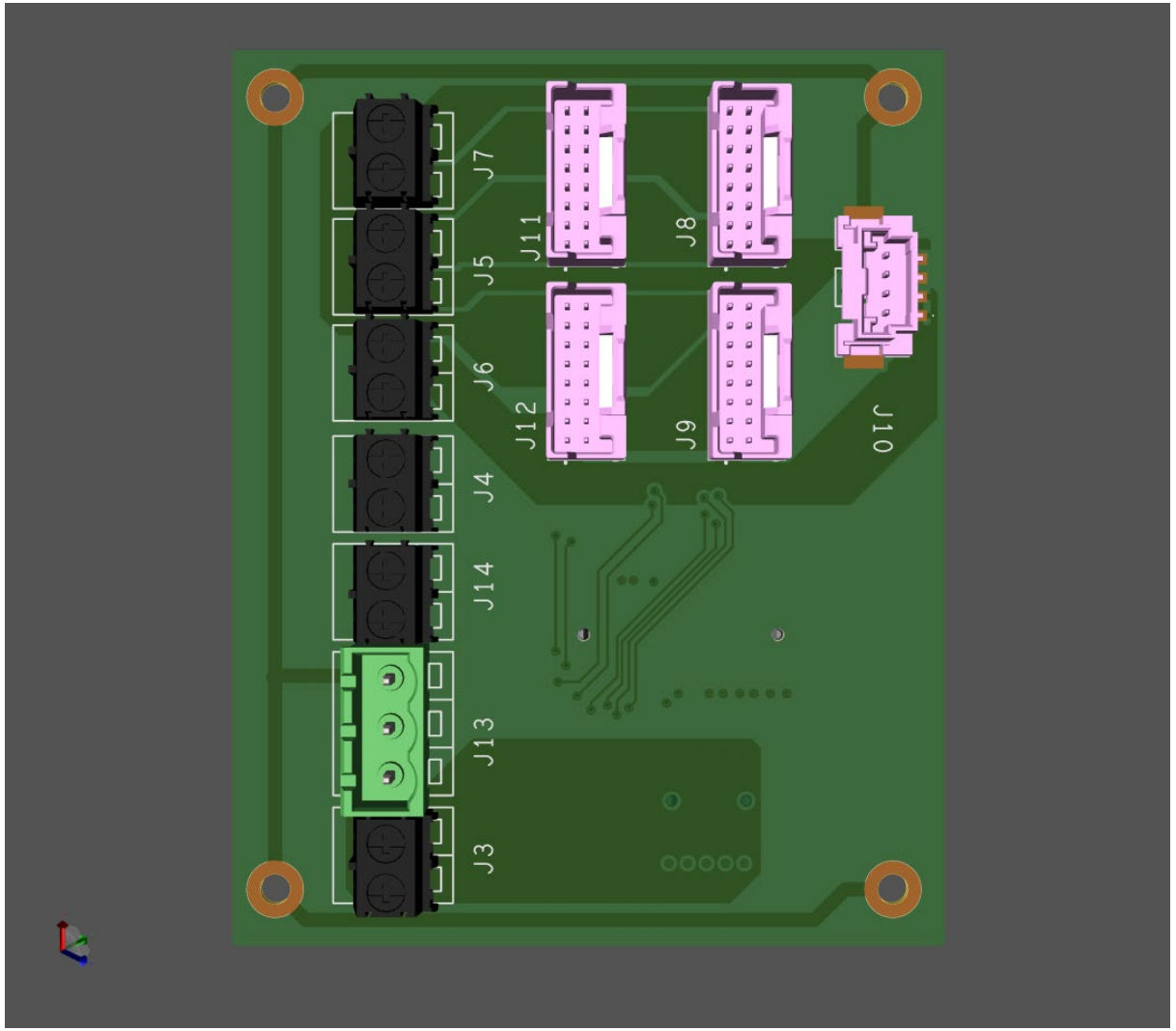
Scheda MasterLogic3 prototipo (48 x 48.5mm)





Scheda MasterPanel prototipo (75,5 x 95mm)





Fine

Grazie per l’attenzione