Test setup for the fully-digital SiPM

Davide Falchieri, Luigi Rignanese

INFN Bologna

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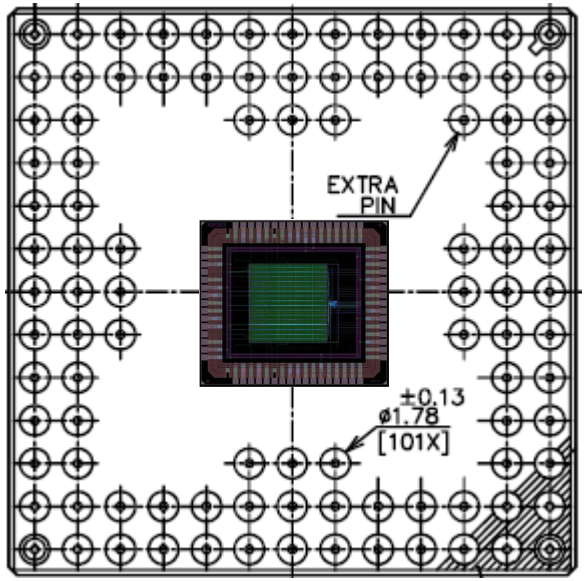
Aspides prototype chip



package CPGA100

ASIC I/O pinout:

- 5 mm²
- 66 total pads
  - 28 digital pads
    - 14 outputs
    - 14 inputs
  - 36 analog pads
    - 8 bias voltages
    - 24 power supply
    - 4 SPAD bias
  - 2 breakers

Aspides prototype chip: pinout

NAME	PAD	PIN							
DATA_D	6	D1	digital	input	slow				serial data for column register
DATA_P	7	E2	digital	input	slow				serial data for programming register
VSS_CORE1v2	8	E1	analog	low voltage	0 V				
CATHODE	9	F3	analog	high voltage	25 V	PowerSupply	15V - 25V		
DATA_W	10	F2	digital	input	slow				serial data for row register
VDD_CORE1v2	11	F1	analog	low voltage	1,2 V				
VDD_IO1v2	12	G2	analog	low voltage	1,2 V				
EN_D	13	G3	digital	input	slow				enable column register output
EN_W	14	G1	digital	input	slow				enable row register output
VSS_IO1v2	15	H1	analog	low voltage	0 V				
VSS_CORE1v2	16	H2	analog	low voltage	0 V				
EN_P	17	H3	digital	input	slow				enable programming register output
CATHODE	18	J1	analog	high voltage	25 V	PowerSupply	15V - 25V		
VDD_CORE1v2	19	J2	analog	low voltage	1,2 V				
VSS_CORE1v2	20	K1	analog	low voltage	0 V				
VbiasU	30	M4	analog	high voltage	3,3 V	Trim	3V:100mV:3.3V		bias voltage quencing network
VDD_IO3v3	31	N4	analog	high voltage	3,3 V				
Vclamp	32	M5	analog	high voltage	1,9 V	Trim	1.8V:100mV:2V		gate voltage clamping transistor in quencing network
VSS_IO3v3	33	N5	analog	high voltage	0 V				
VbiasD	34	L6	analog	high voltage	1 V	Trim	0.9V:100mV:1.1V		bias voltage quencing network
CATHODE	35	M6	analog	high voltage	25 V	PowerSupply	15V - 25V		
Vp	36	N6	analog	low voltage	0 V	DAC	0V:10mV:0.6V		TDC bias voltage P-side
VDD_IO1v2	37	M7	analog	low voltage	1,2 V				
VSS_IO1v2	38	L7	analog	low voltage	0 V				
PCNT<0>	39	N7	digital	output	fast	Probe			parallel counter output
PCNT<1>	40	N8	digital	output	fast	Probe			parallel counter output
VDD_CORE1v2	41	M8	analog	low voltage	1,2 V				
STOP	42	L8	digital	input	very fast	EXT			TDC stop signal
SHIFT	43	N9	digital	input	slow				PISO register shift mode
LATCH	44	M9	digital	input	slow				PISO register sampling mode
PCNT<2>	45	N10	digital	output	fast	Probe			parallel counter output
PCNT<3>	46	M10	digital	output	fast	Probe			parallel counter output

ToT	56	K13	digital	output	very fast	Probe			Time-over-Threshold trigger
TDClast	57	J12	digital	output	slow				TDC last PISO register output
VSS_CORE1v2	58	J13	analog	low voltage	0 V				
TDCfirst	59	H11	digital	output	slow				TDC first PISO register output
ROW3	60	H12	digital	output	very fast	Probe			3 row coincidence trigger
VDD_CORE1v2	61	H13	analog	low voltage	1,2 V				
VDD_IO1v2	62	G12	analog	low voltage	1,2 V				
ROW2	63	G11	digital	output	very fast	Probe			2 row coincidence trigger
PCNT	64	G13	digital	output	slow				parallel counter PISO register output
VSS_IO1v2	65	F13	analog	low voltage	0 V				
VSS_CORE1v2	66	F12	analog	low voltage	0 V				
NAND	67	F11	digital	output	very fast	EXT		>400ps	NAND tree trigger output
FINISH	68	E13	digital	output	fast	EXT		>5ns	finish signal for counting operation
VDD_CORE1v2	69	E12	analog	low voltage	1,2 V				
CNT	70	D13	digital	output	slow				serial counter PISO output
STARTfirst	80	B10	digital	output	very fast	EXT		>400ps	TDC first trigger output
CLK	81	A10	digital	input	clock				system clock signal
HRST_N	82	B9	digital	input	fast				hard reset
GATE	83	A9	digital	input	fast				global GATE signal
TEST	84	C8	digital	input	fast	EXT			global TEST signal
SRST_N	85	B8	digital	input	fast				soft reset
VDD_CORE1v2	86	A8	analog	low voltage	1,2 V				
VSS_CORE1v2	87	B7	analog	low voltage	0 V				
VSS_IO1v2	88	C7	analog	low voltage	0 V				
VDD_IO1v2	89	A7	analog	low voltage	1,2 V				
Vn	90	A6	analog	low voltage	1,2 V	DAC	0.6V:10mV:1.2V		TDC bias voltage N-side
CATHODE	91	B6	analog	high voltage	25 V	PowerSupply	15V - 25V		
VbiasD	92	C6	analog	high voltage	1 V	Trim	0.9V:100mV:1.1V		bias voltage quencing network
VSS_IO3v3	93	A5	analog	high voltage	0 V				
Vclamp	94	B5	analog	high voltage	1,9 V	Trim	1.8V:100mV:2V		gate voltage clamping transistor in quencing network
VDD_IO3v3	95	A4	analog	high voltage	3,3 V				
VbiasU	96	B4	analog	high voltage	3,3 V	Trim	3V:100mV:3.3V		bias voltage quencing network

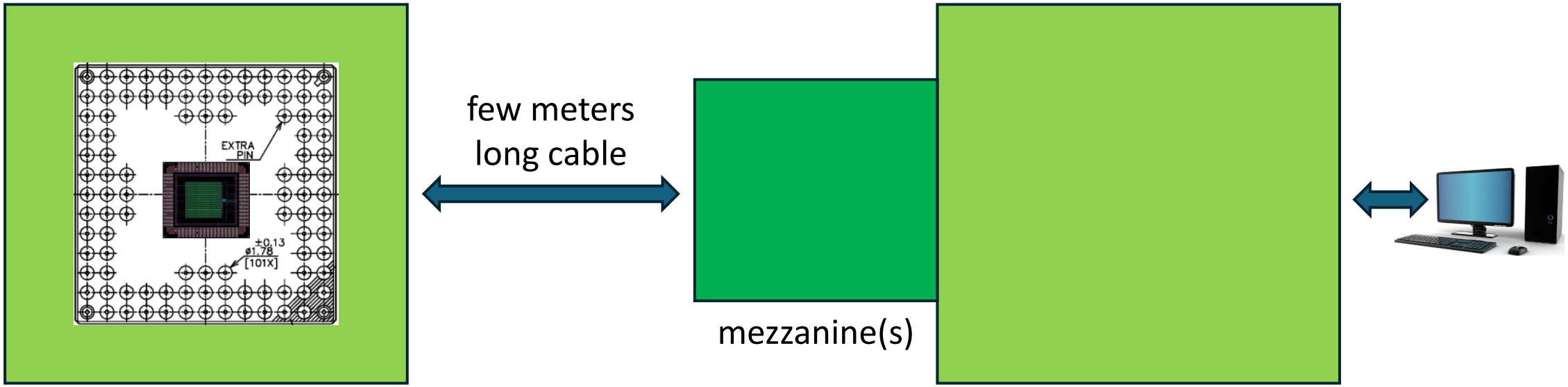
28 digital single-ended 1.2 V signals:

- 5 to be monitored with a scope (SMA connector)
- 7 via probes

These signals need to be converted to 1.8 V

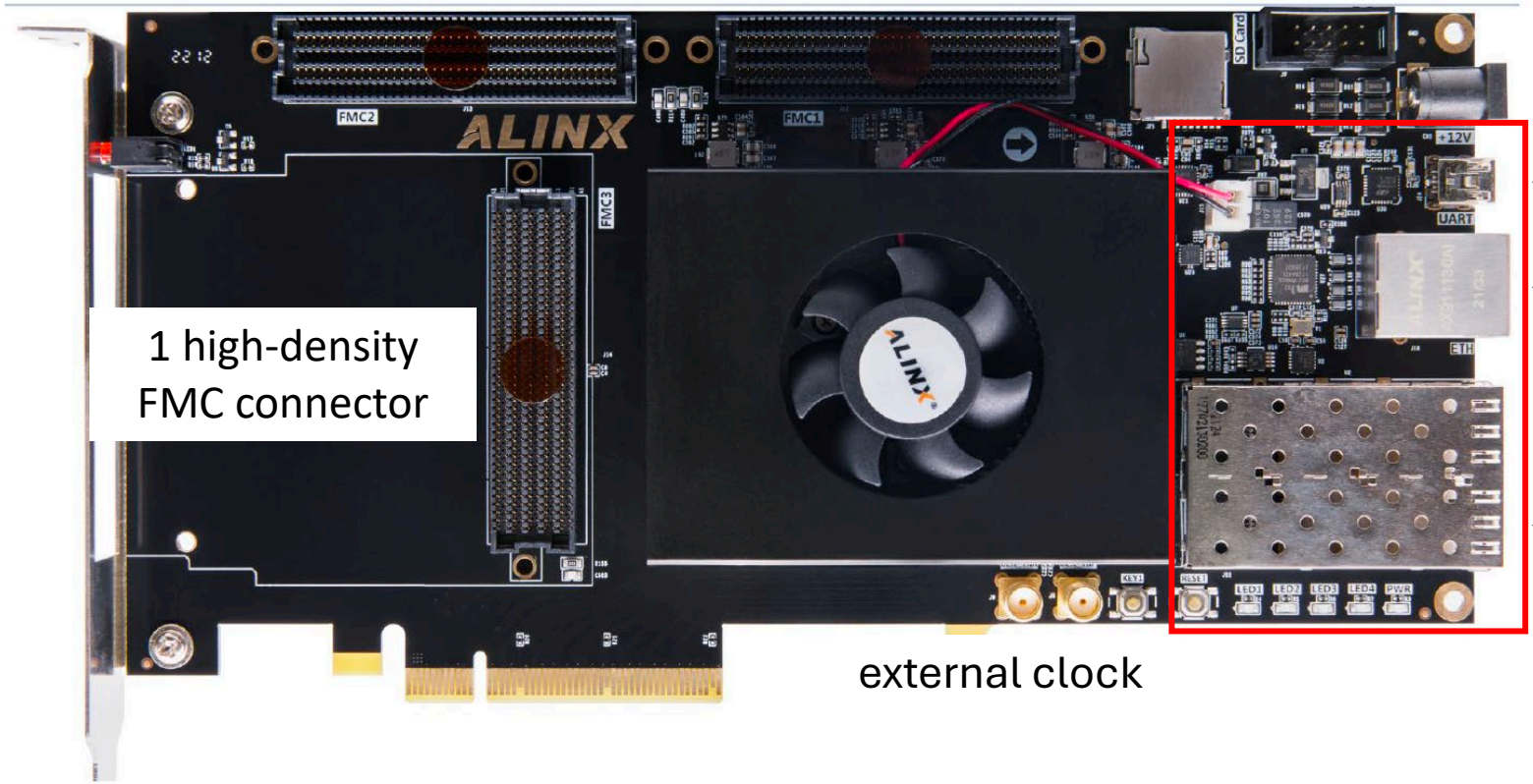
2-6 critical signal shall be converted in differential LVDS (400 ps) for both external and FPGA readout

DAQ conceptual scheme



FPGA board: Kintex Ultrascale+ AXKU062

2 low-density FMCs



1 high-density FMC connector

external clock

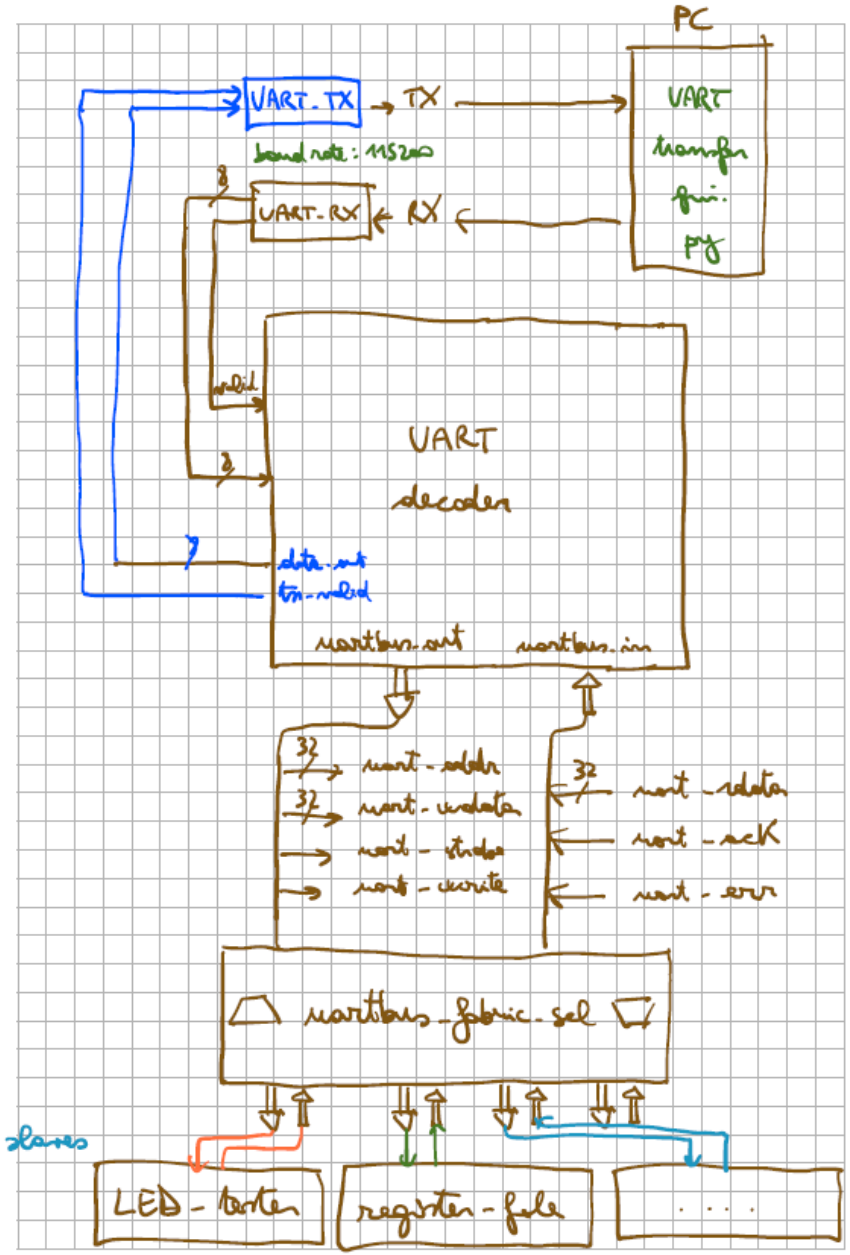
USB-UART

Gigabit Ethernet

2 optical transceivers

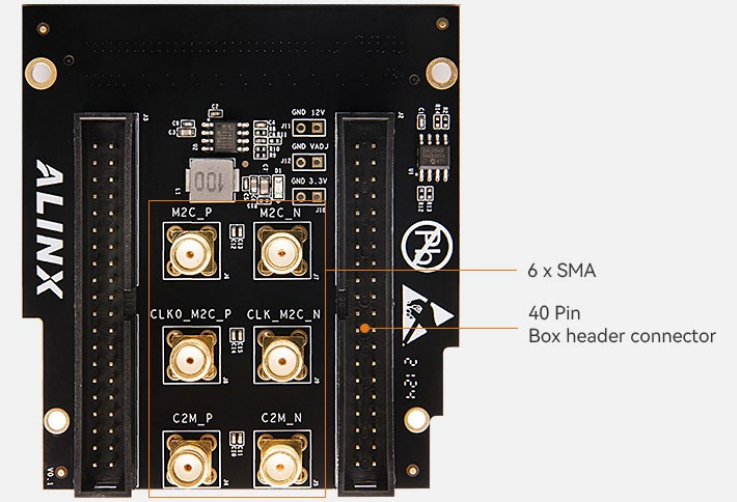
https://www.en.alinx.com/Product/FPGA-Development-Boards/Kintex-UltraScale/AXKU062.html

From UART bus to IPbus ?

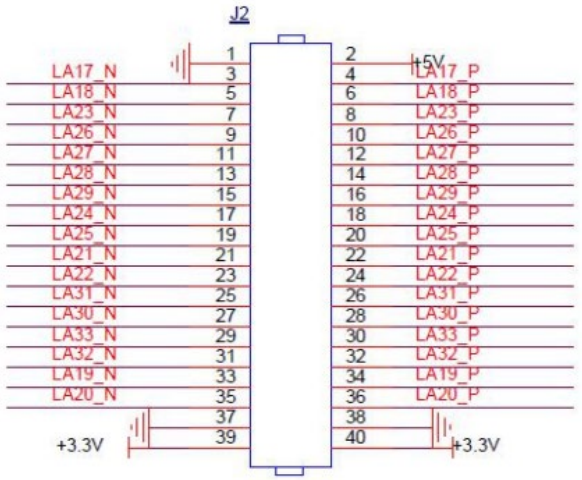


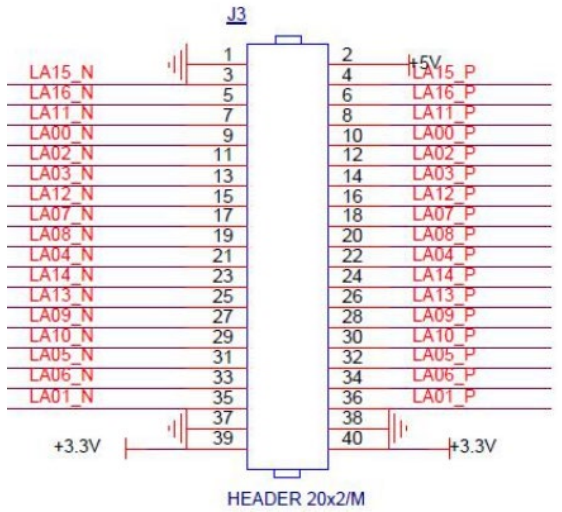
For the DAQ of the first test chip we used the UART bus.
If needed, we can move to CERN Ipbus:
the firmware structure is very similar, but the data throughput to the PC is much higher

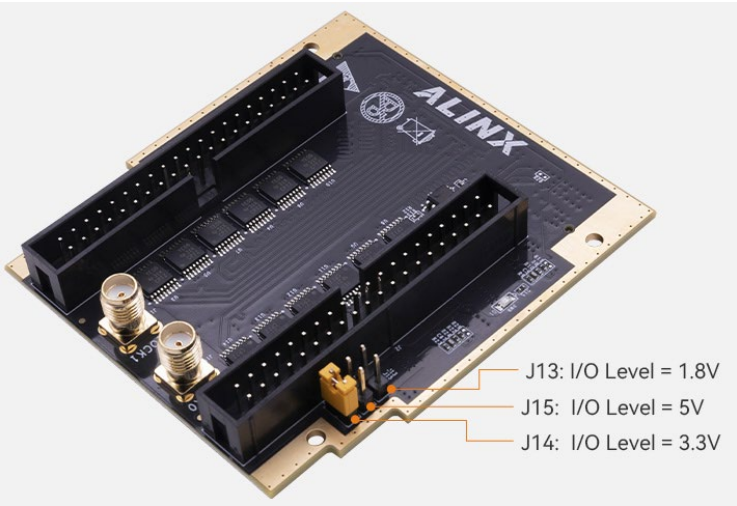
FMC breakout boards



https://www.en.alinx.com/Product/FMC-Cards/Other/FL1010.html
Proposal 1, 4







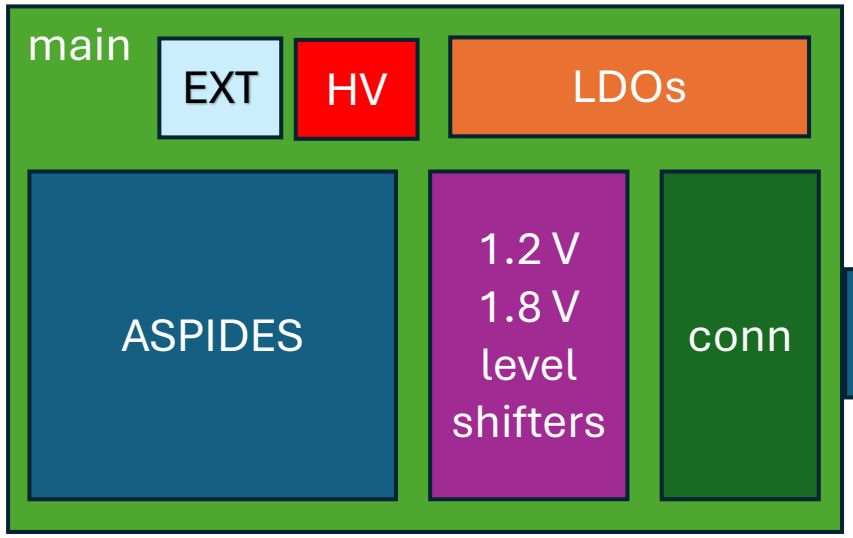
https://www.en.alinx.com/Product/FMC-Cards/Other/FL1010-V.html
Proposal 2 with modification

The market offers low-cost FMC breakout boards that could be useful in out DAQ readout chain

The level shifters on Alinx board are very slow … probably not acceptable

Proposal 1

mainboard with all the services and a 40-pin connector to FPGA



flat cable

mainboard

pros:

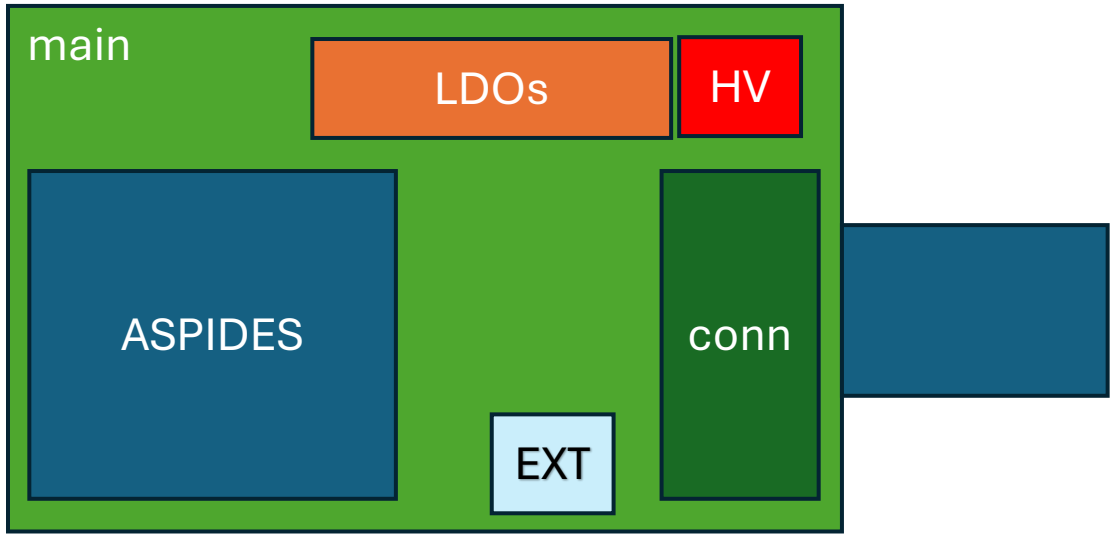
- just 1 board to design

cons:

- active components on the mainboard

Proposal 2

breakout with only level shifter



pros:

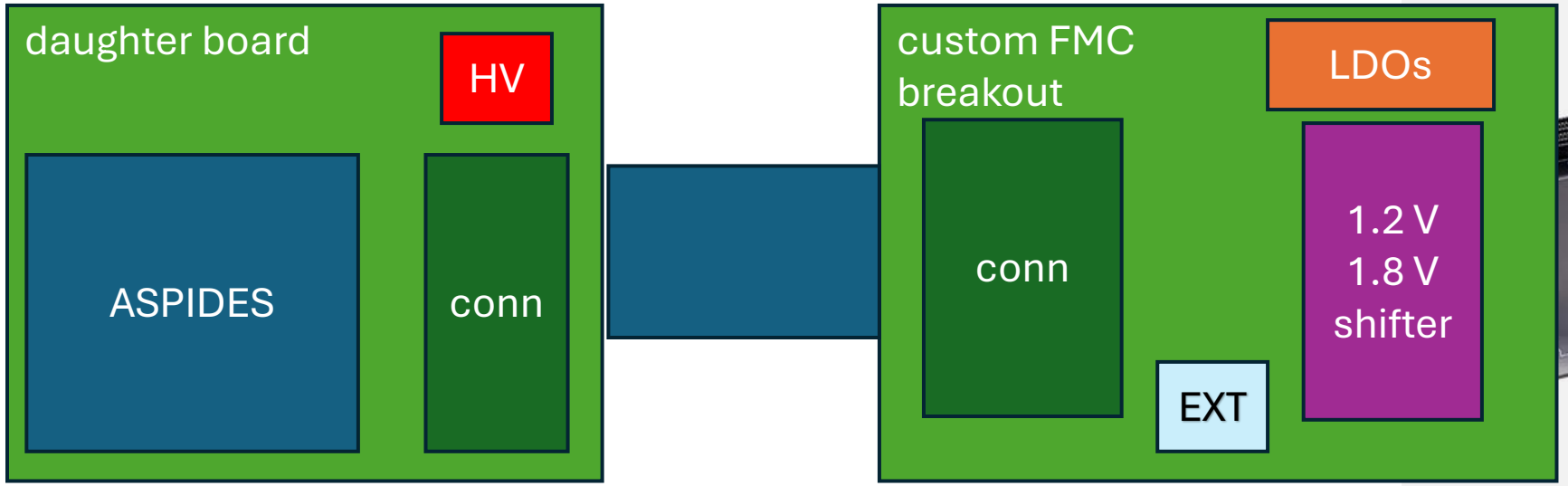
- just 1 board to design

cons:

- still active components on the mainboard

Proposal 3

custom breakout board with LDOs and level shifters



pros:

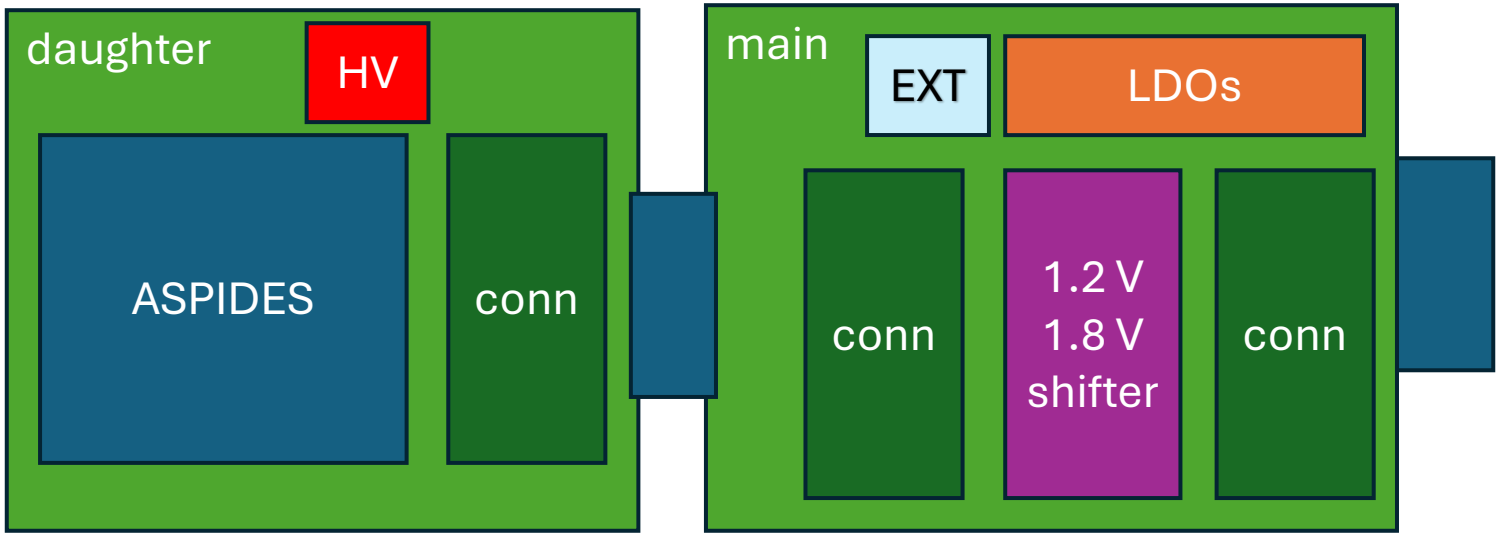
- no active components on the daughter

cons:

- 2 boards to be develop

Proposal 4

Daughter-board with only HV connector and all the pins are connected to a connector to the mainboard with all the services and a 40 pin connector to FPGA



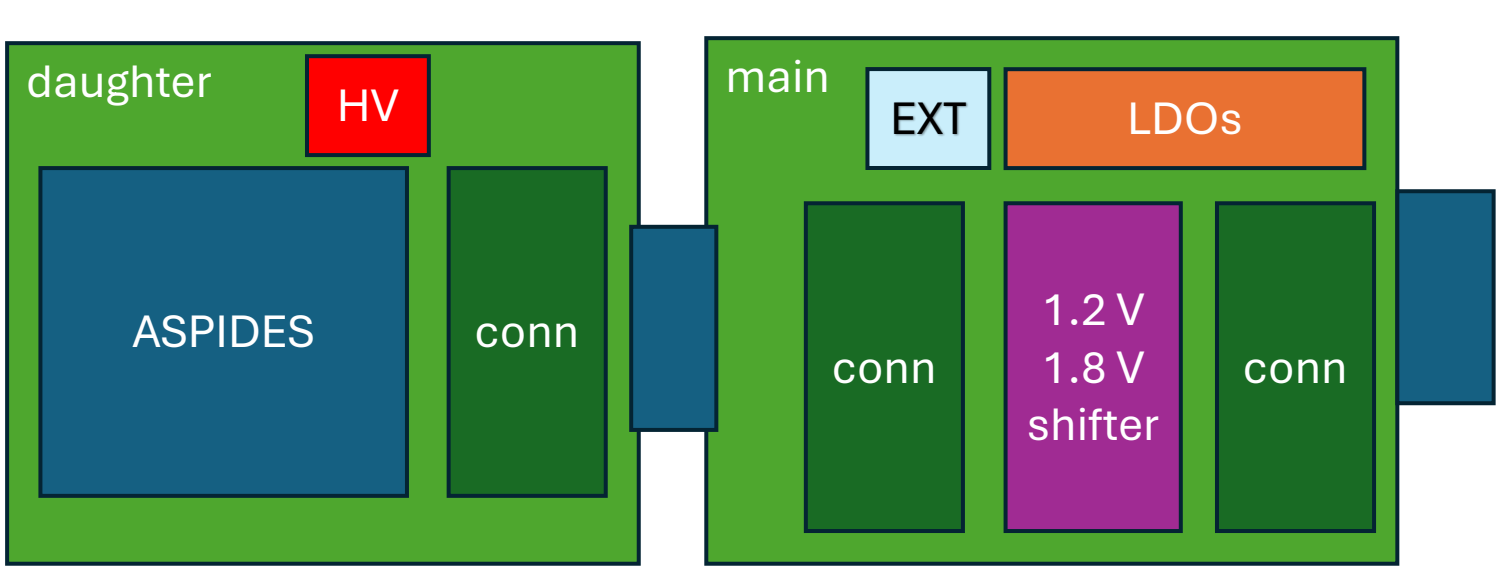
pros:

- no active components on the daughter

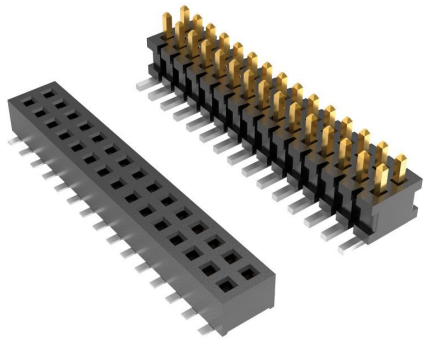
cons:

- 2 boards to be develop

Evaluating Samtec connectors



micro pitch board-to-board terminal and socket strips



samtec

- Series up to 10,000 cycles
- Wide array of board stacking heights
- Various mating orientations
- Rugged options
- Numerous contact styles
- Stack heights .235" (5.91 mm) - .754" (19.15 mm)
- Available up to 100 pins

https://www.samtec.com/flex-stacking/low-profile/050-pitch-terminals-sockets/

Outlook

- We are currently aiming at **proposal 4** as our baseline target architecture.

- What do we need to do:
  - buy a FMC breakout board from Alinx
  - design the daughter board
  - design the main-board
  - start designing the firmware for ASIC configuration and readout