ASPIDES
WP1- ASIC design and verification

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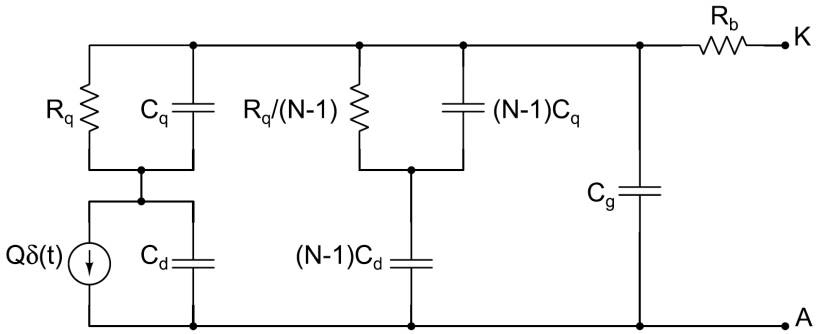
Macro-pixel Architecture

Basic ideas:

1. Design an analogue SiPM directly connected to the ReadOut Electronics (ROE);
2. Exploit the voltage step produced by the avalanche process at the SiPM output to perform a low jitter time measurement;
3. ToT at constant current applied at the SiPM output (SiPM considered as a capacitor) to measure the number of detected photons.

SiPM equivalent electric model

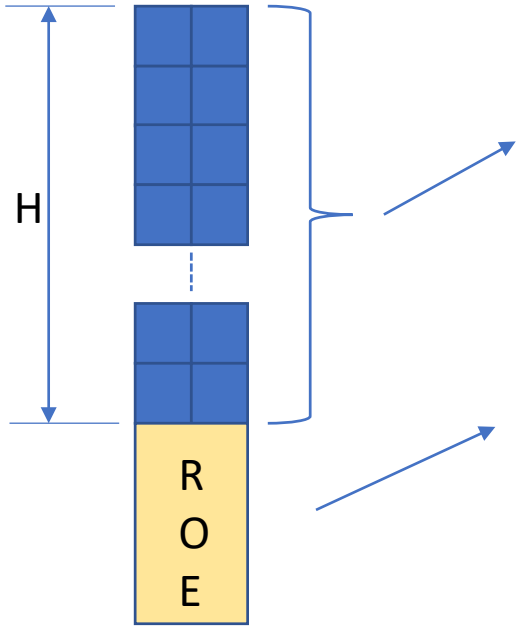


The avalanche process produces at the SiPM output a voltage step followed by the recovery tail. The voltage step amplitude is about:

$$V_{step} \approx \frac{V_{OV}}{\frac{N}{1+{C_q}/{C_d}} + \frac{C_g}{C_q}}$$

- V_{ov}: SiPM bias overvoltage;
- C_d: photo diode capacitance;
- C_g: grid parasitic capacitance;
- C_q: queching resistor (Rq) parasitic capacitance;
- N: number of microcells

Macro-pixel



SiPM:

- Number of microcells depends on the required height (H)

ReadOut Electronics:

- Low jitter ToA measurement;
- Linear measurement of detected photon by means of ToT.

Design criteria:

1. Microcell dimension (C_d): dynamic and radiation hardness;
2. SiPM dimension (N, C_g): height of sensitive area;
3. C_q value can be chosen in order to get a voltage step high enough to be directly discriminated -> no amplifier -> no BWT, no noise

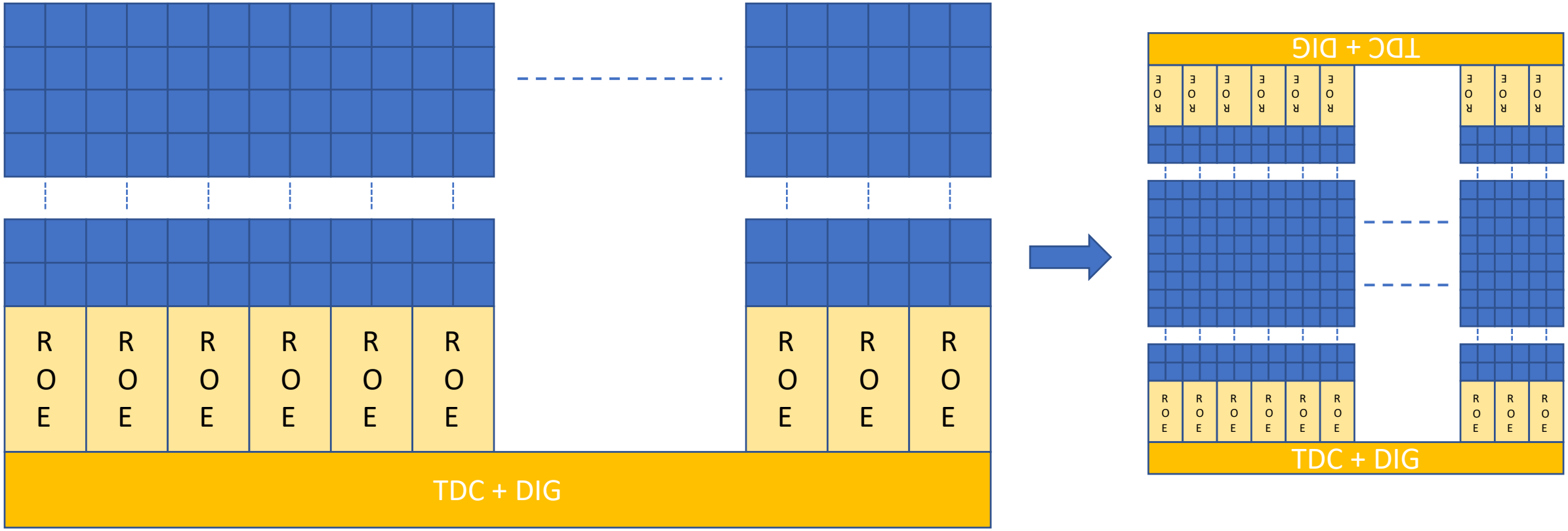
SiPM architecture

HALF MODULE:

- macro-pixels can be horizontally abutted in order to realize an array of the required length, at the bottom of the ROE line the TDC + digital section can be placed.

FULL MODULE:

- mirroring the HALF MODULE respect to the x – axis the whole SiPM is obtained



HALF MODULE

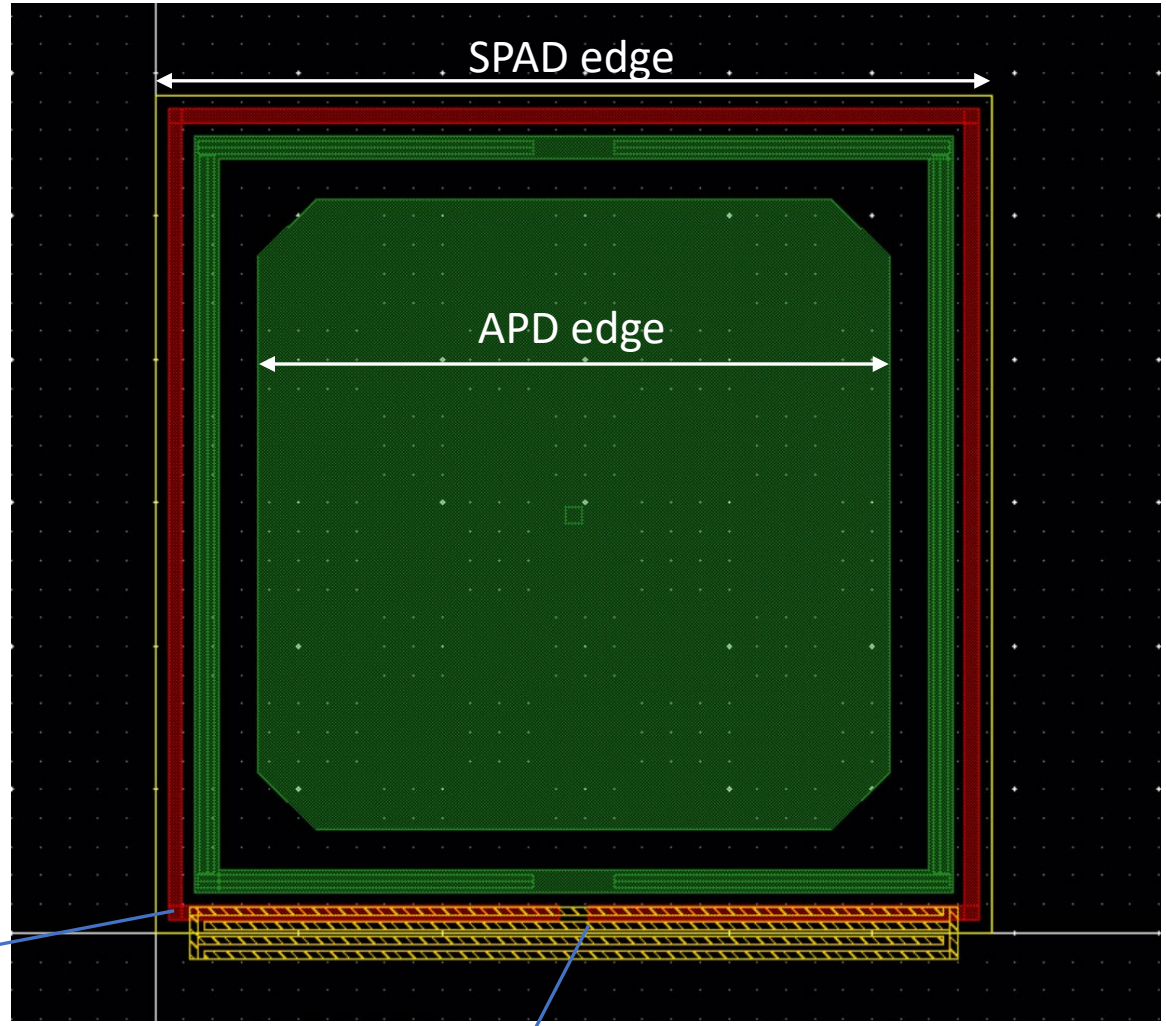
FULL MODULE

Microcell

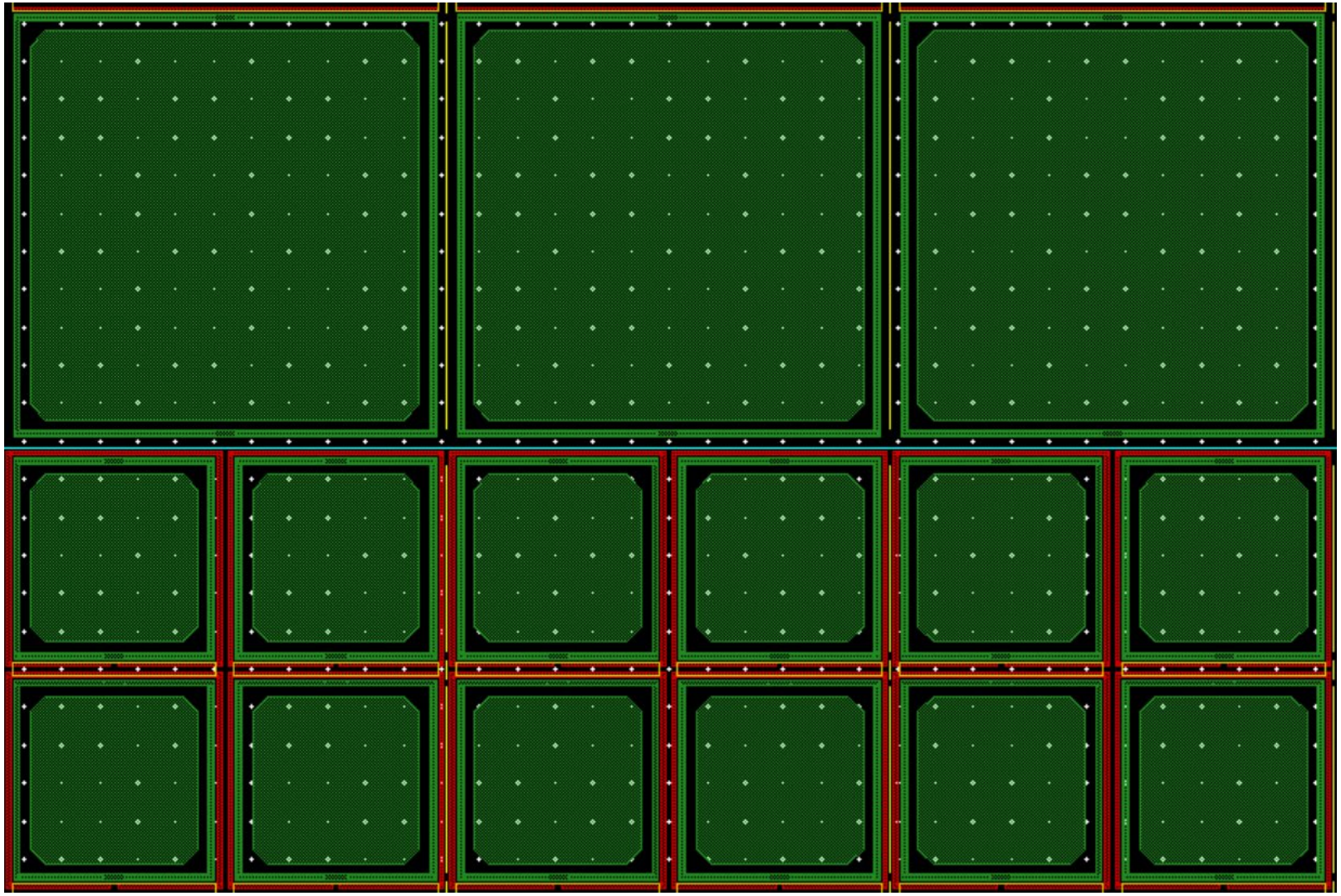
Microcell (SPAD):

- **Small size:**
  - APD (designed by L. Pancheri):
    - Edge: 22 um;
    - Area: 476 um^2;
    - Cd about 47.6 fF;
  - Quenching resistor:
    - Resistance about 400 kOhm;
    - Cq about 20 fF;
  - SPAD
    - Edge: 29.2 um;
    - Fill factor: 55.8%.
- **Big size:**
  - APD:
    - Edge: 51 um;
    - Area: 2613.44 um^2;
    - Cd about 261.344 fF;
  - Quenching resistor:
    - Resistance about 200 kOhm;
    - Cq about 42 fF;
  - SPAD:
    - Edge: 58.4 um;
    - Fill factor: 76.6%.

Cq optimized to work from 0.5 V of over-voltage



Microcell: small size vs big size



Microcell layout optimized to have one common NTUB for all the pixels –> No PSUB -> higher fill factor

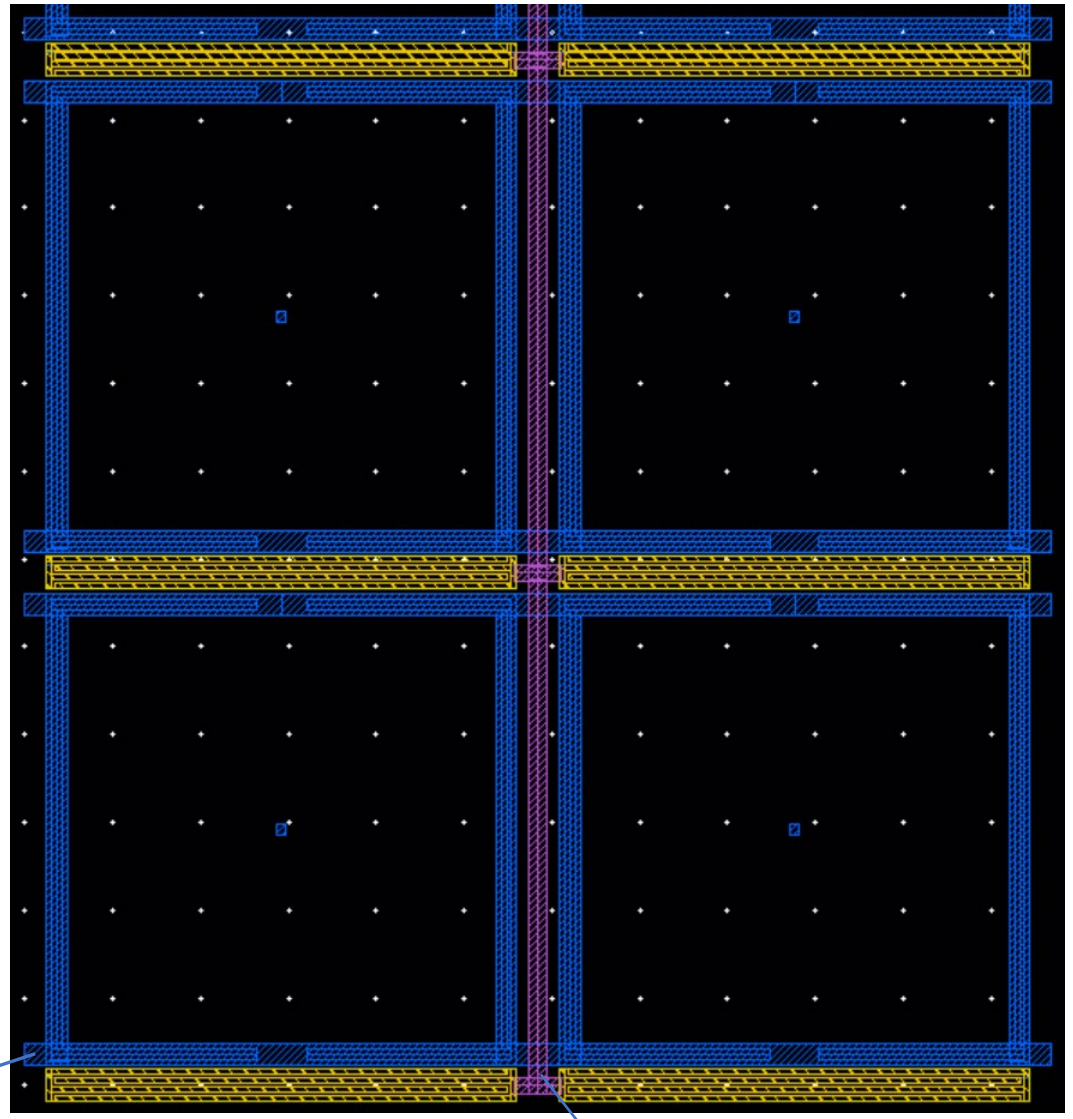
Macropixel

Macropixel (SiPM):

- **Small microcell size (22 um):**
  - Number of microcells: 68;
  - Array: 34 rows x 2 columns;
  - Height: 992.8 um;
  - Width: 58.4 um;
  - Fill factor: 55.8%.

- **Big microcell size (51 um):**
  - Number of microcells: 17;
  - Array: 17 rows x 1 column;
  - Height: 992.8 um;
  - Width: 58.4 um;
  - Fill factor: 76.6%.

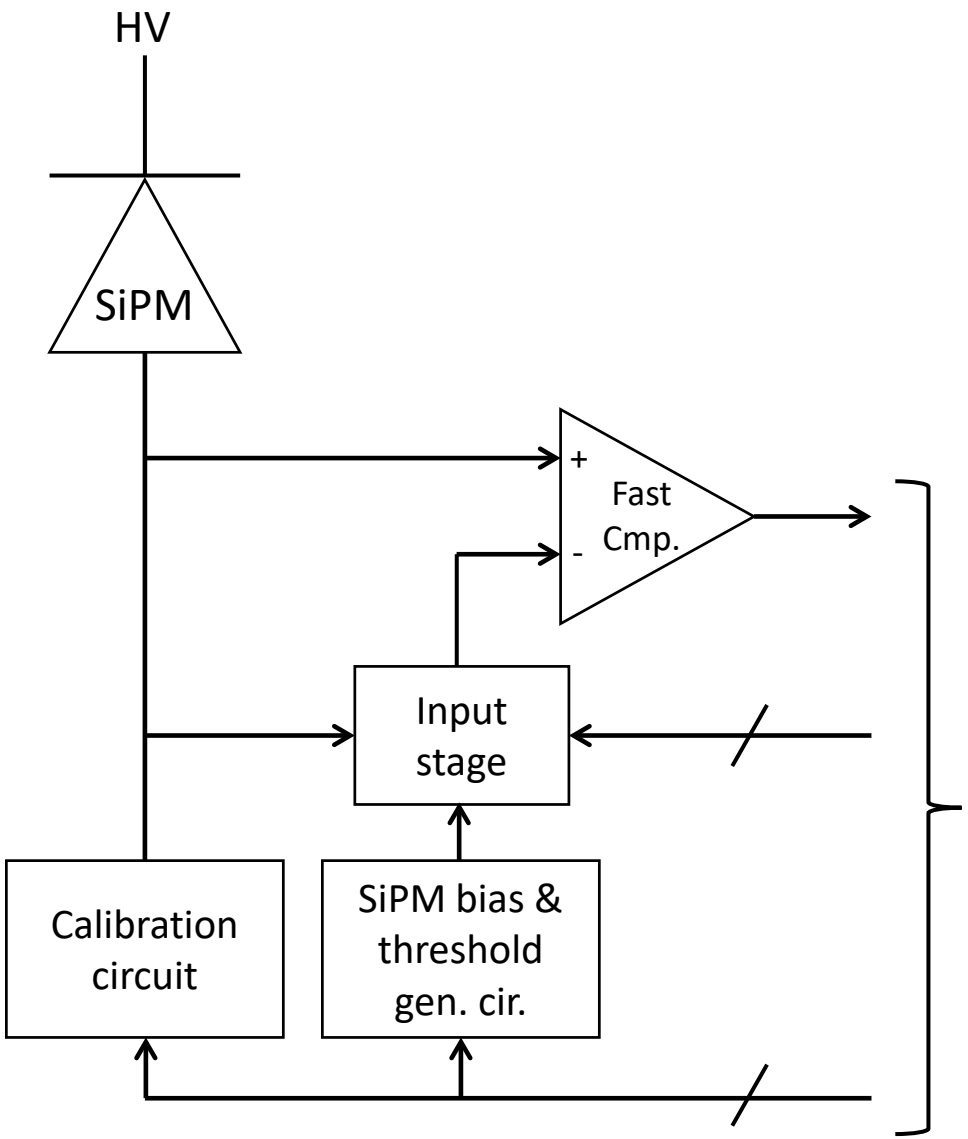
SiPM small microcell size (zoom on 4 pixels, only metal layers)



HV bias grid (blue shape)

SiPM output line (violet shape): top metal, width adjusted according to parasitic capacitance and resistance

ReadOut Electronics



Input stage:

- Provides the equivalent small signal resistance to read the SiPM;
- Controls the SiPM bias for a fine adjustment of the SiPM gain;
- Performs the discharge at constant current of the input node (SiPM anode) in order to measure the number of detected photons (ToT), global adjustment 5 bits;
- Provides the negative input to the fast comparator.

Fast comparator:

- Produces an output pulse whose rising edge marks the arrival time of the incoming event and whose duration is proportional to the number of detected photons.

Calibration circuit:

- Provides a calibration pulse (fixed pulse) for threshold adjustment.

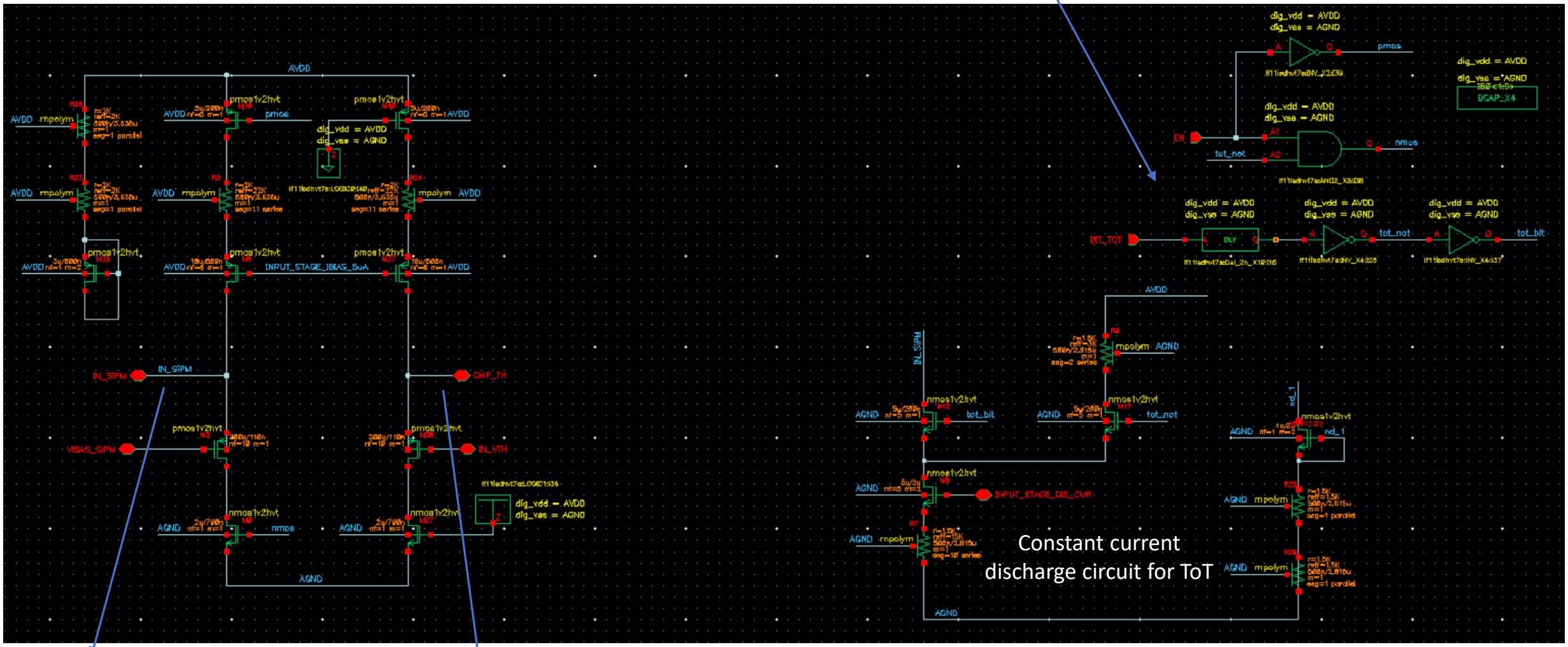
SiPM bias & threshold generation circuit:

- SiPM bias adj.: 8 global bits + 6 local bits (1 sign + 5 polarity);
- Fast cmp threshold adj: SiPM bias + 6 local bits (1 sign + 5 polarity).

ROE: Input Stage architecture

Digital inputs:

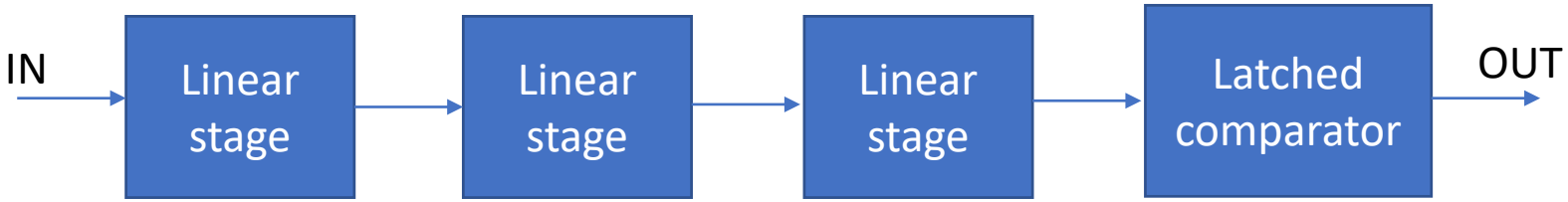
- EN: channel enable
- EN_TOT: enables the discharge at constant current

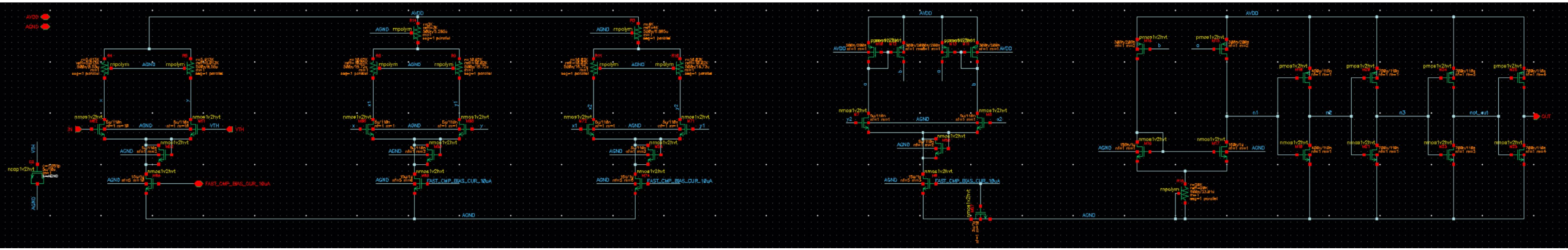


Input connected to SiPM, calibration circuit and fast comparator positive input.

Input connected to fast comparator negative input.

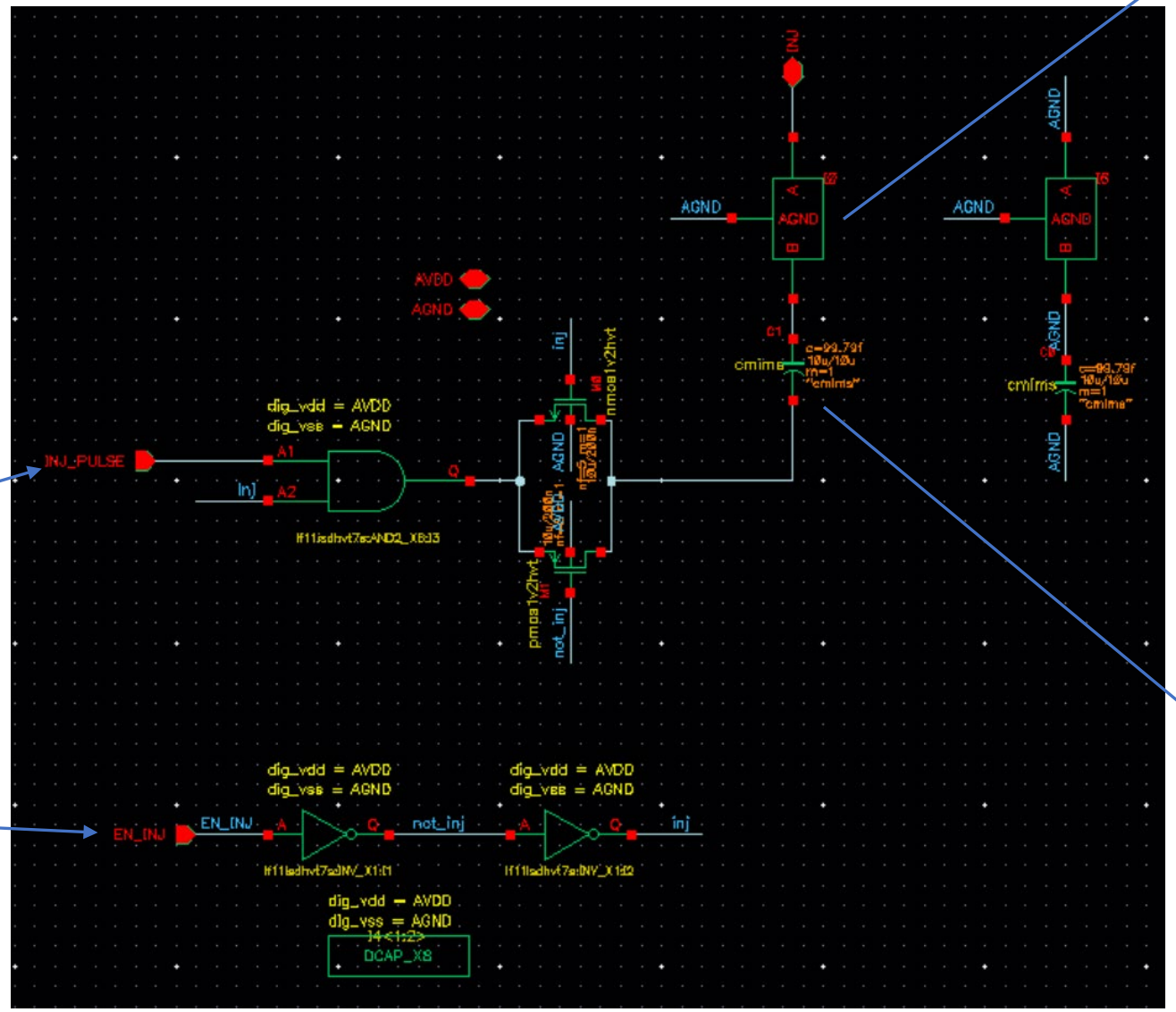
ROE: Fast comparator architecture





ROE: Calibration circuit

SPAD quenching resistor and capacitor



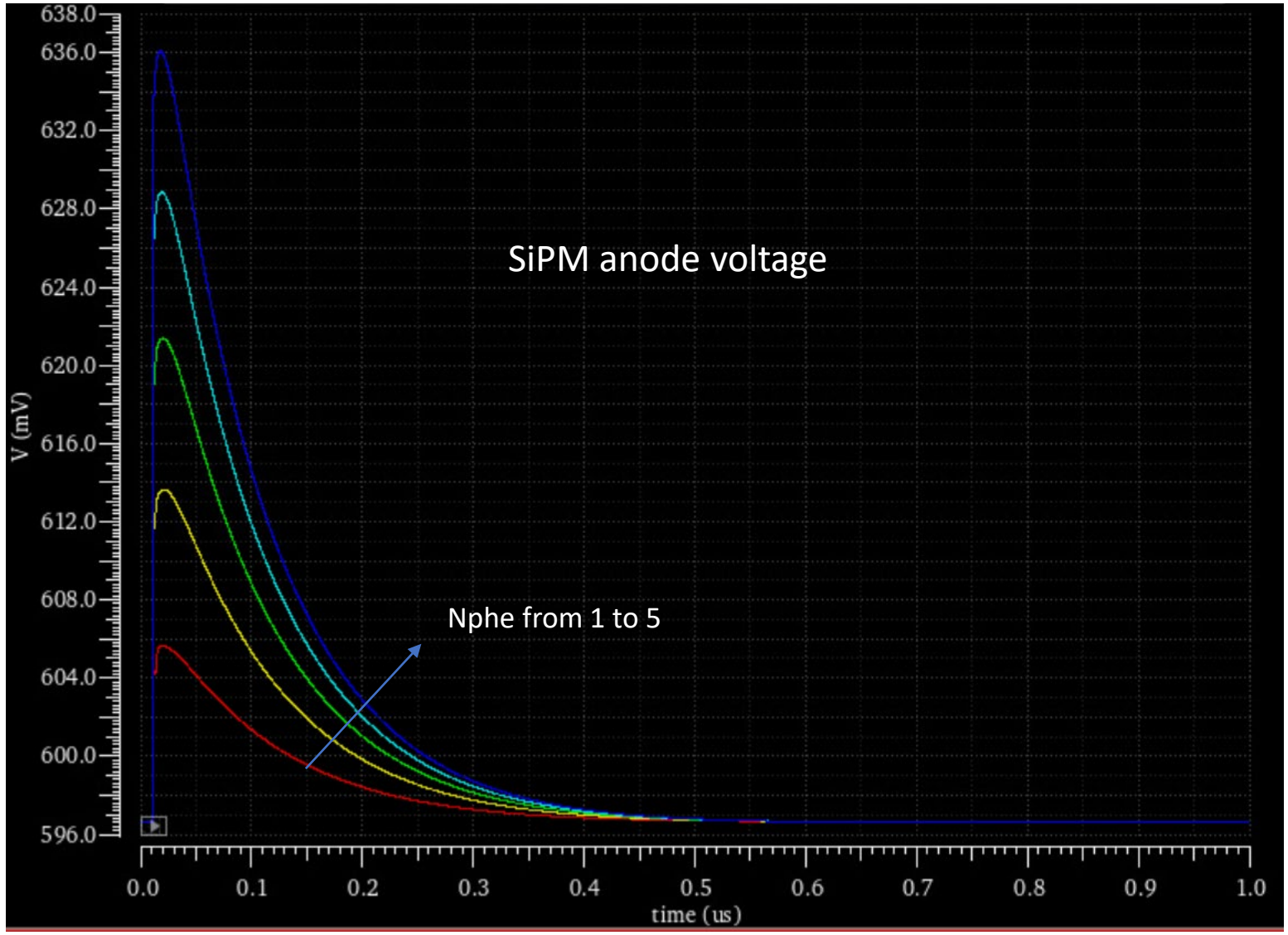
Digital injection pulse

Injection enable

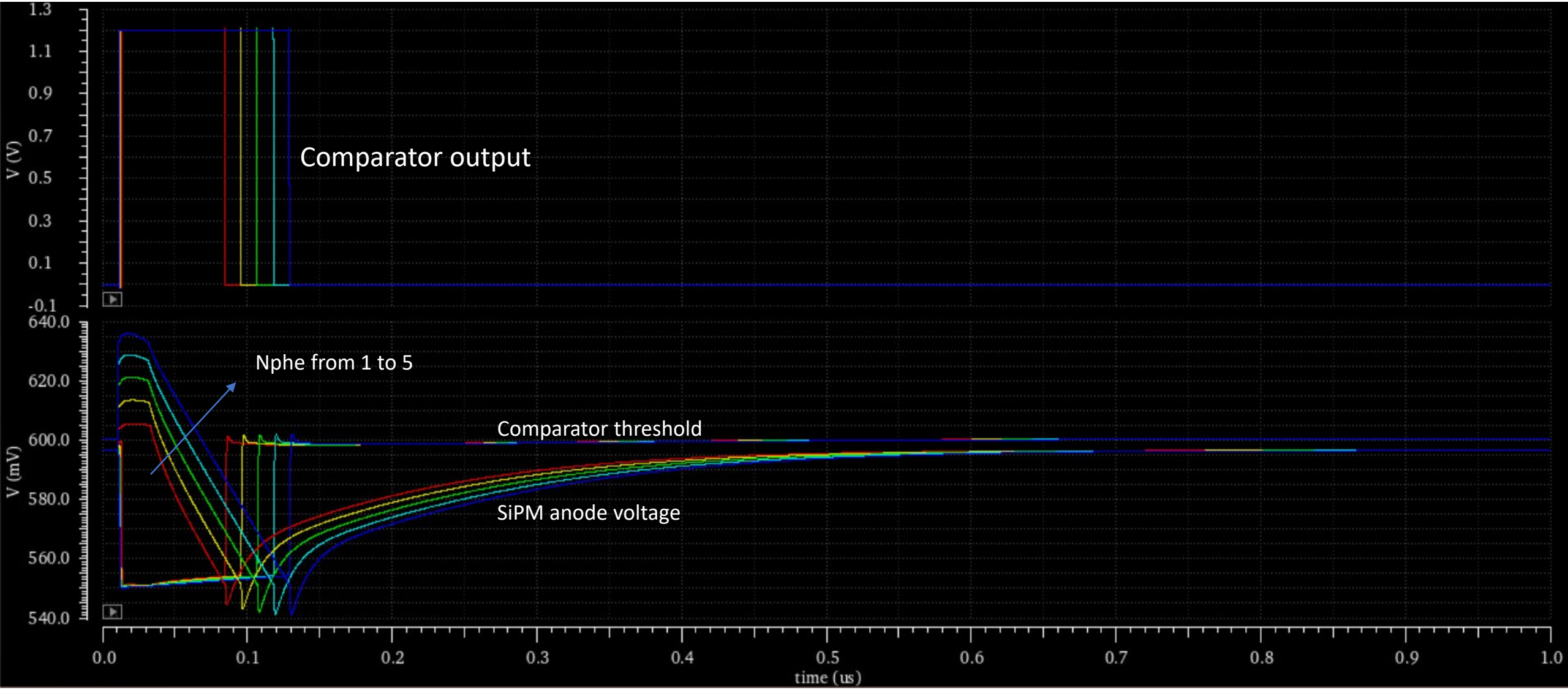
Injection capacitance:

- Adjusted to inject a charge equivalent @ Vov = 0.5 V

Simulation: transient time – no ToT

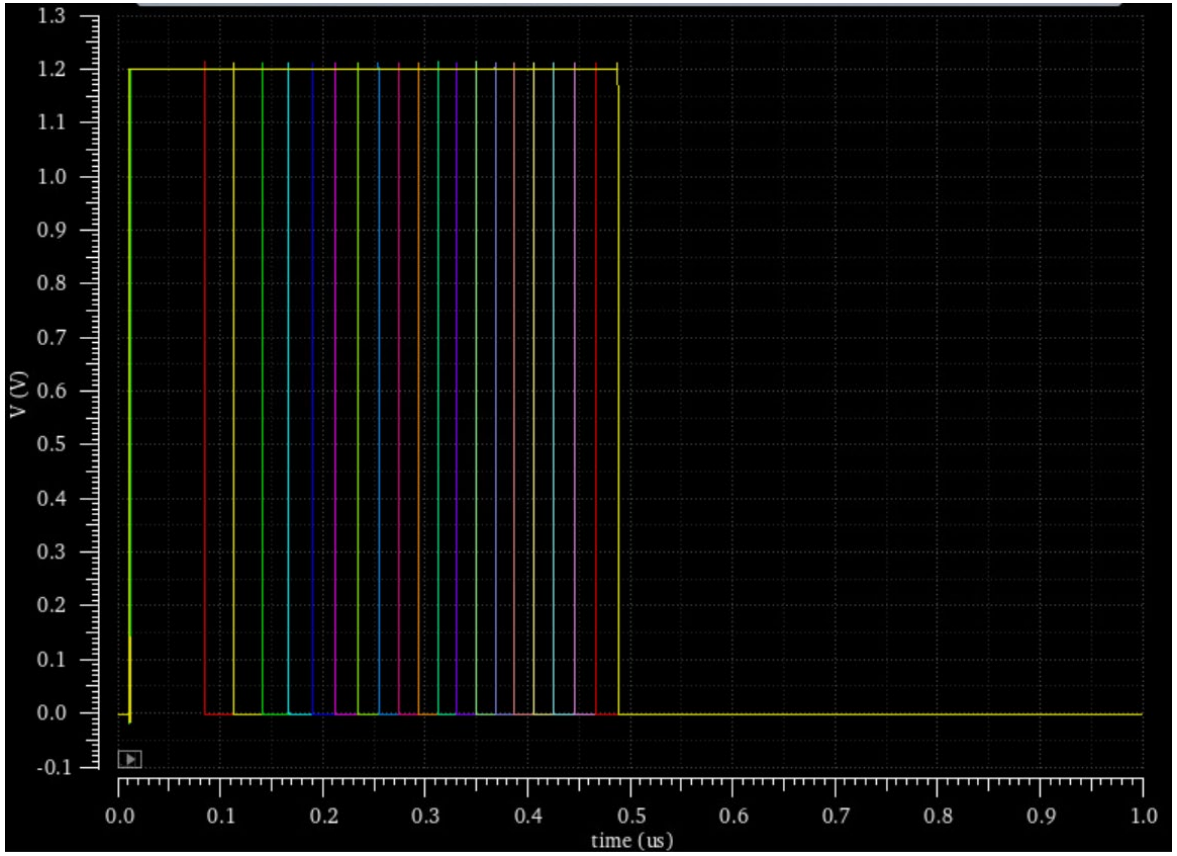


ROE simulation: transient time – ToT for 1 - 5 phe

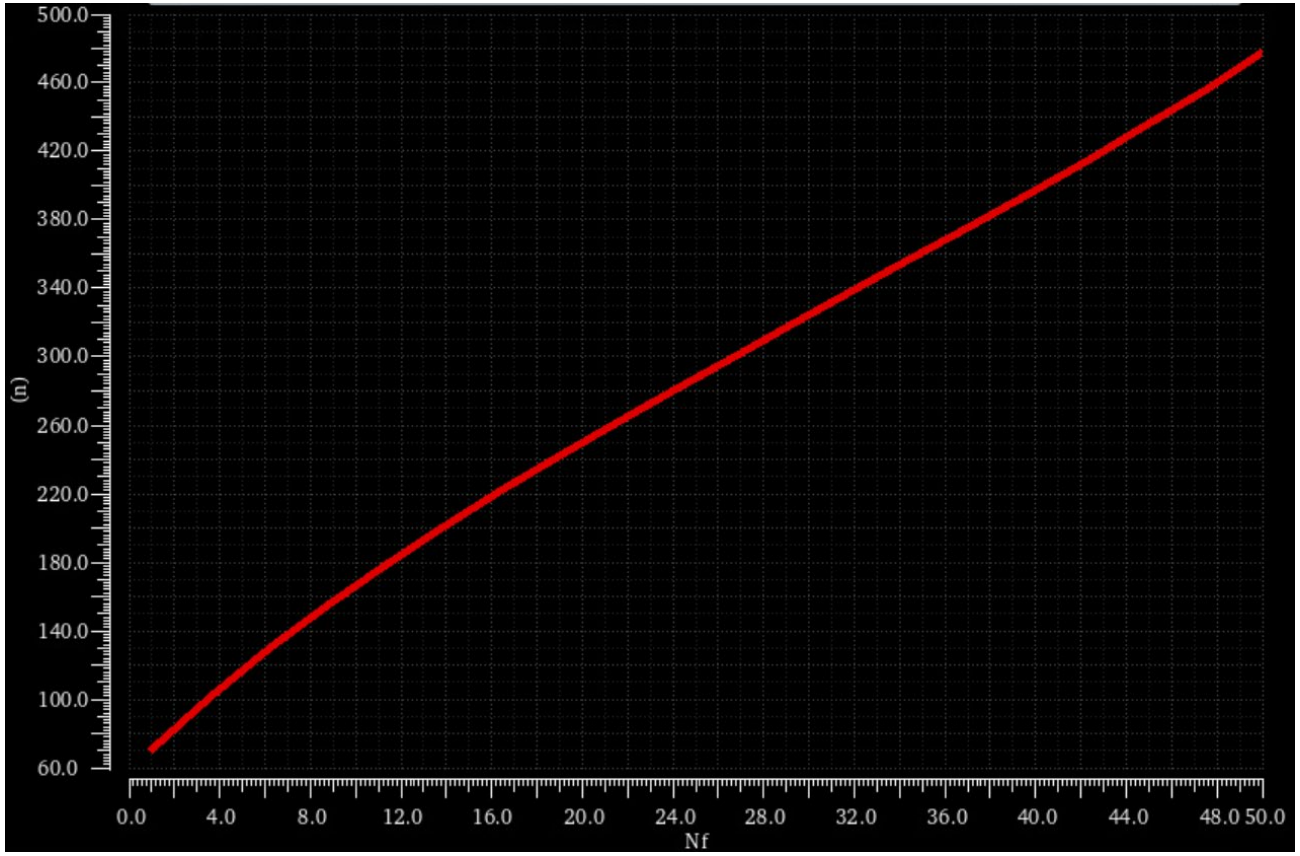


ToT active – measurement for input event from 1 to 5 photons

ROE simulation: transient time – ToT for 1 – 50 phe

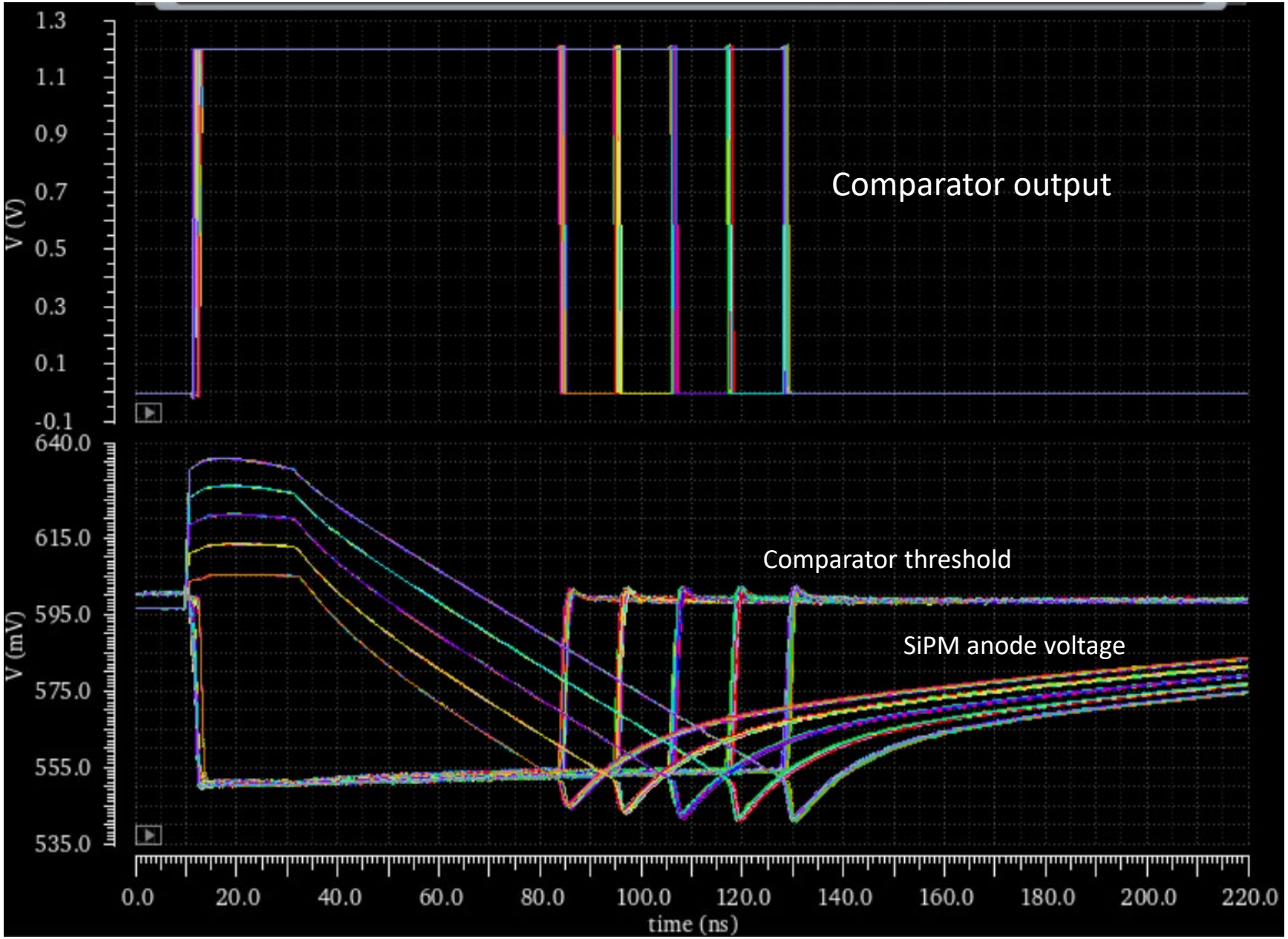


Comparator output for Nf from 1 to 50



Comparator output duration for Nf from 1 to 50

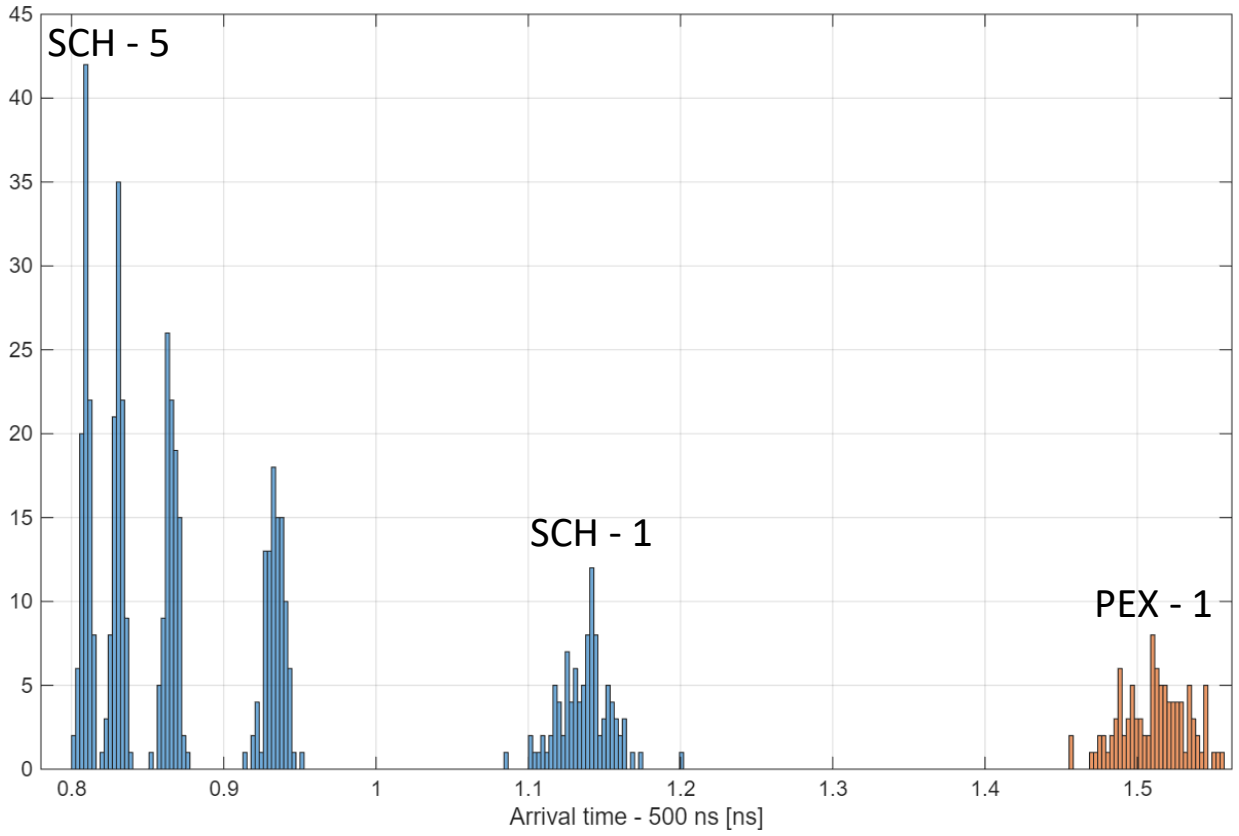
ROE simulation: transient noise – 1 to 5 phe



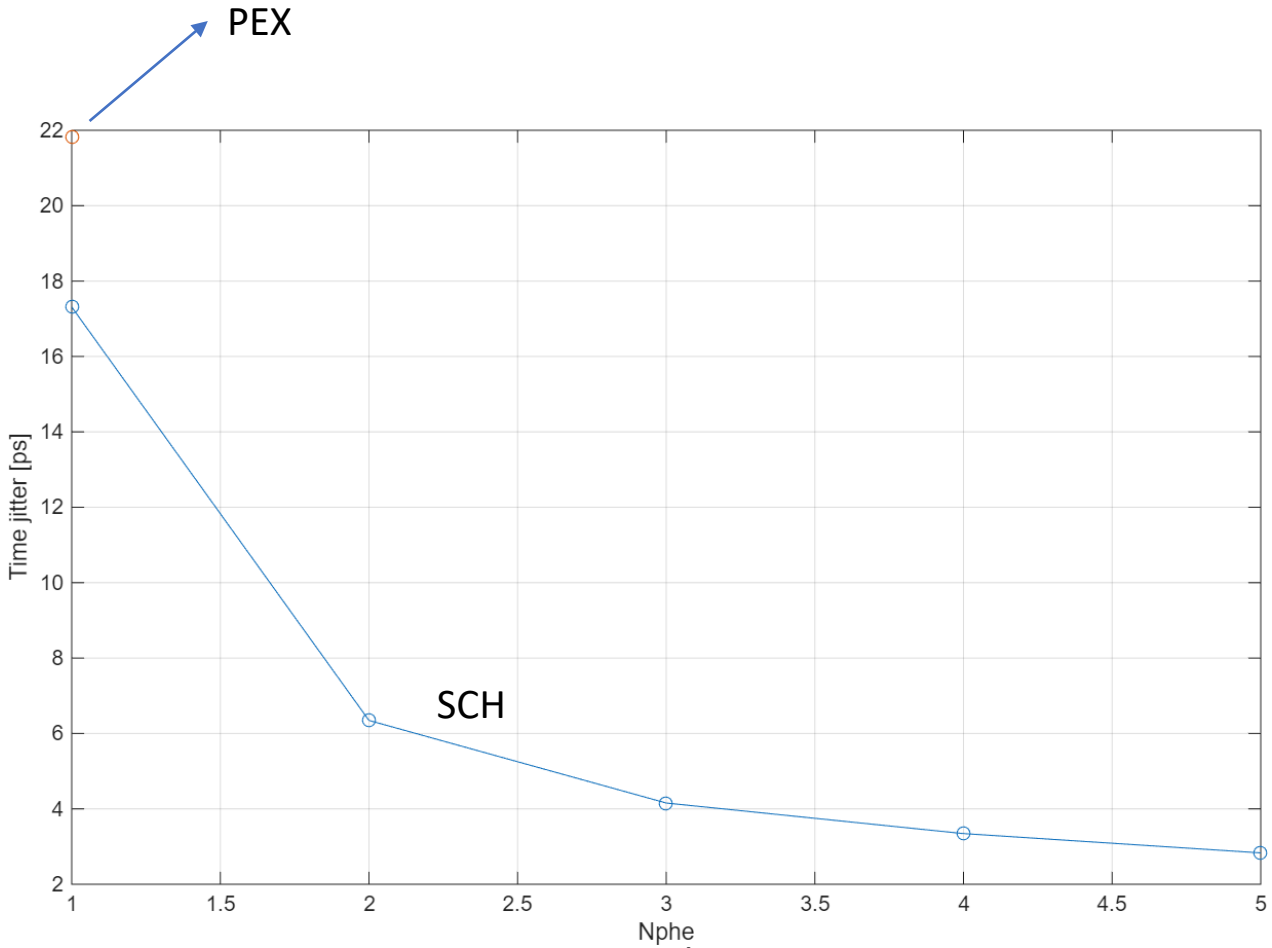
ROE simulation: transient noise - jitter

Monte Carlo transient noise (100 runs):

- The two flavours of macropixels are equalized in terms of jitter due to electronics noise;
- Vov = 0.5 V
- Schematic (SCH): 1 – 5 phe
- Post-layout (PEX): 1 phe



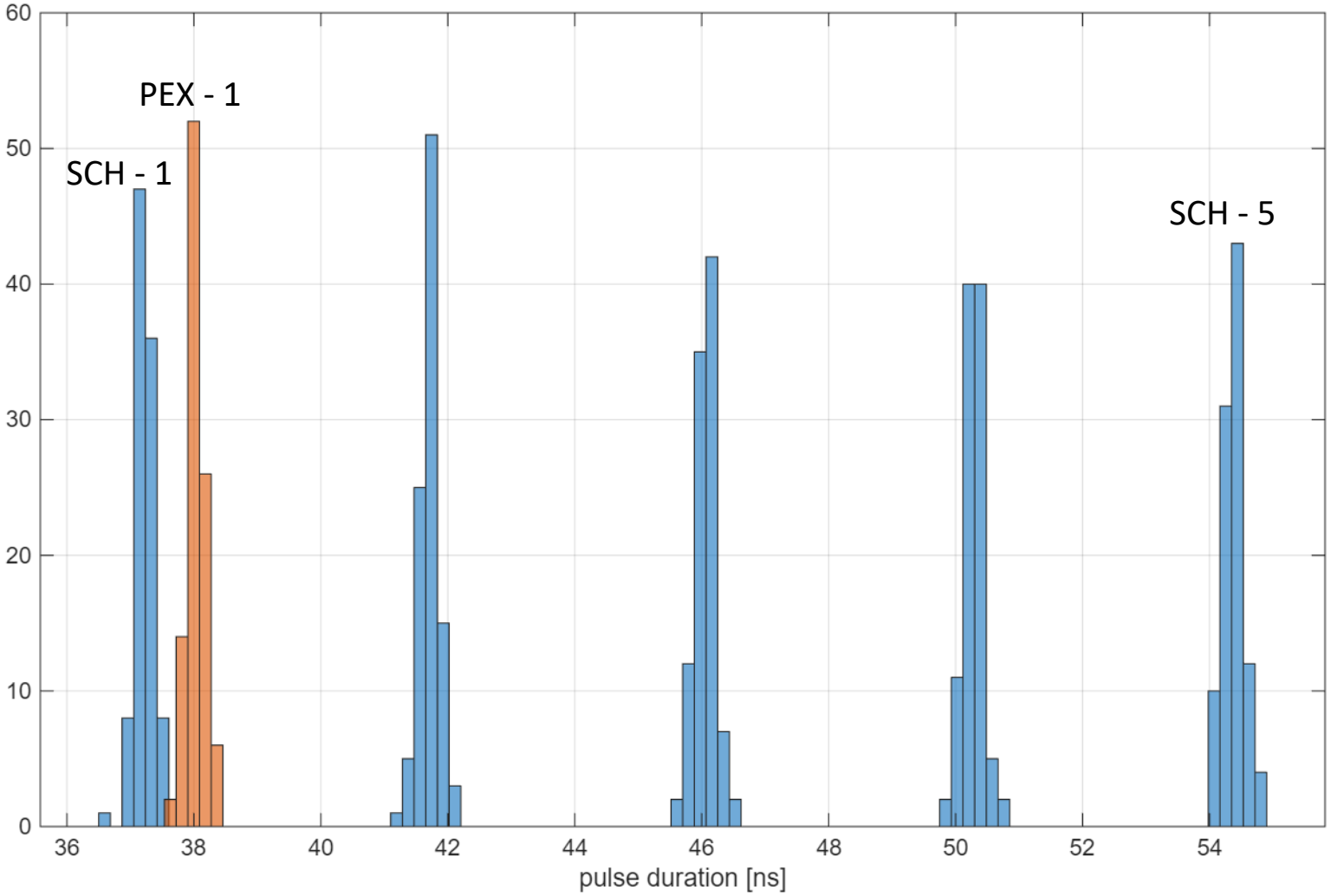
Arrival time distributions Vov = 0.5 V



Time jitter 1phe:

- Schematic: 16.6 ps
- Post-layout: 21.8 ps

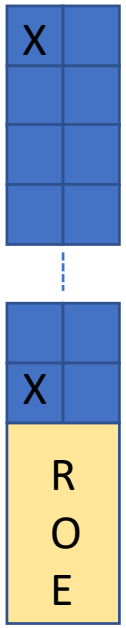
ROE simulation: transient noise – photon counting



Pulse duration

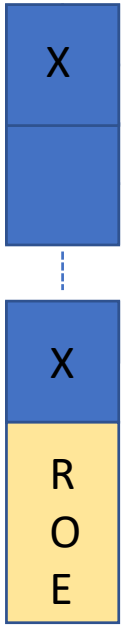
ROE simulation: post-layout – micropixel propagation delay

- Post-layout simulation: parasitic includes;
- Vov = 0.5 V;
- Measurement: propagation time difference according to firing microcell position.



Macro-pixel (22 um SPAD):

- Dt = 84 ps
- Sigma = 84/sqrt(12) ps ≈ 24 ps
- Sigma_t = 22 ⊕ 24 ≈ 33 ps



Macro-pixel (51 um SPAD):

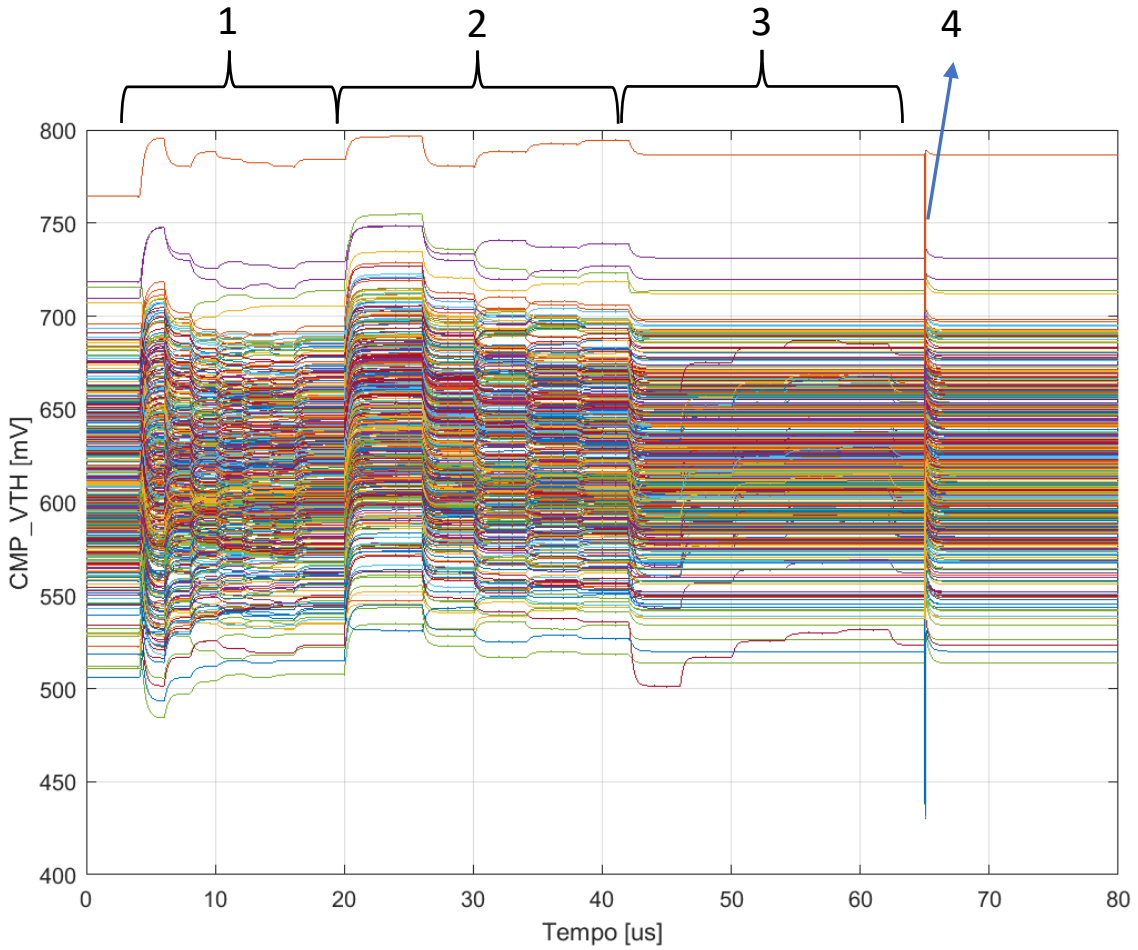
- Dt = 22 ps
- Sigma ≈ 6.35 ps
- Sigma_t = 22 ⊕ 6.35 ≈ 23 ps

More parasitic is present the 22 um solution -> more propagation delay

ROE simulation: fast cmp threshold calibration

Monte Carlo simulation (proc. + mis.): fast local threshold tuning for channel equalizzation (5 bit local DAC)

1. Base line search;
2. Calibration pulse search (positive DAC polarity);
3. Calibration pulse search (negative DAC polarity);
4. SiPM signal firing for check.

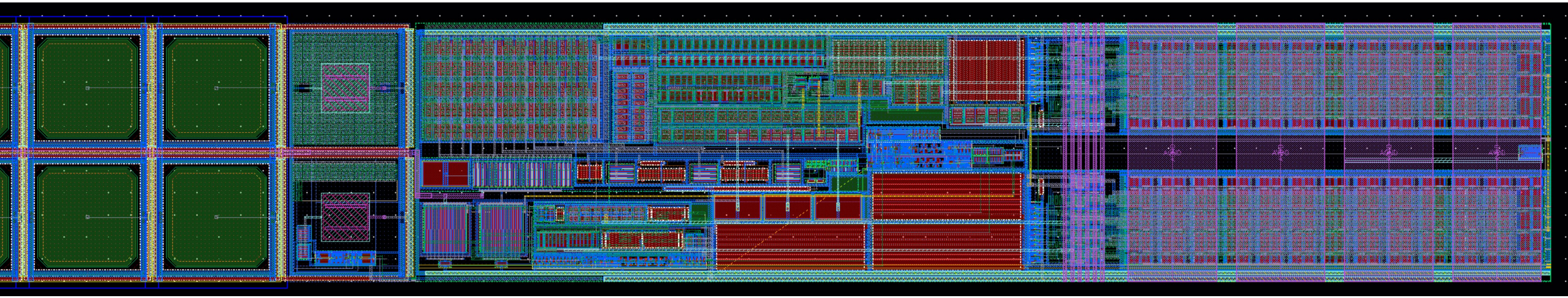


ROE layout

SiPM base

Calibration circuit

Input stage – Fast comparator – SiPM bias & threshold gen. Cir.

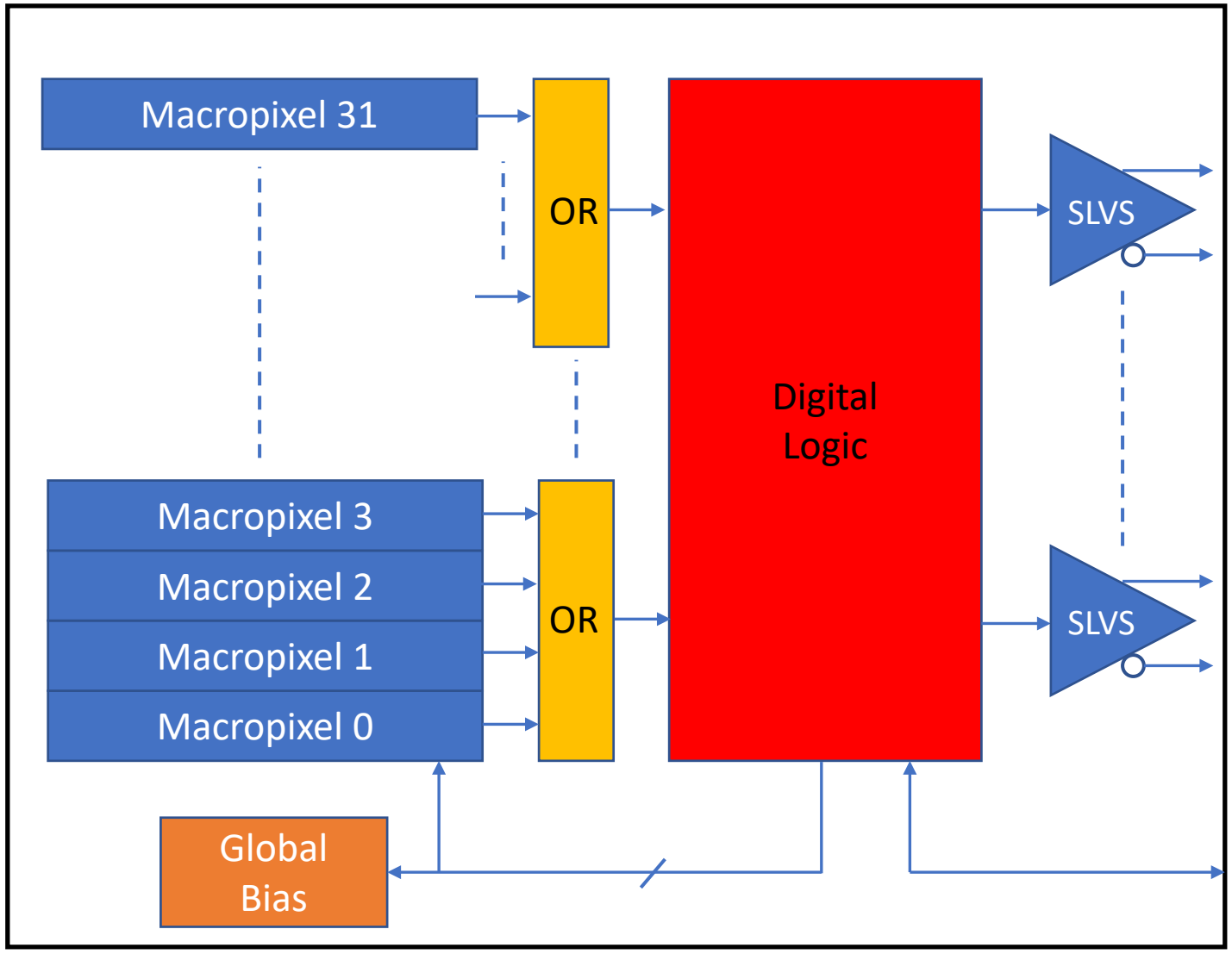


Dimensions:

- Length: 287.5 um
- Height: 58.4 um

Current consumption: 280 uA

HALF MODULE (prototype version): architecture



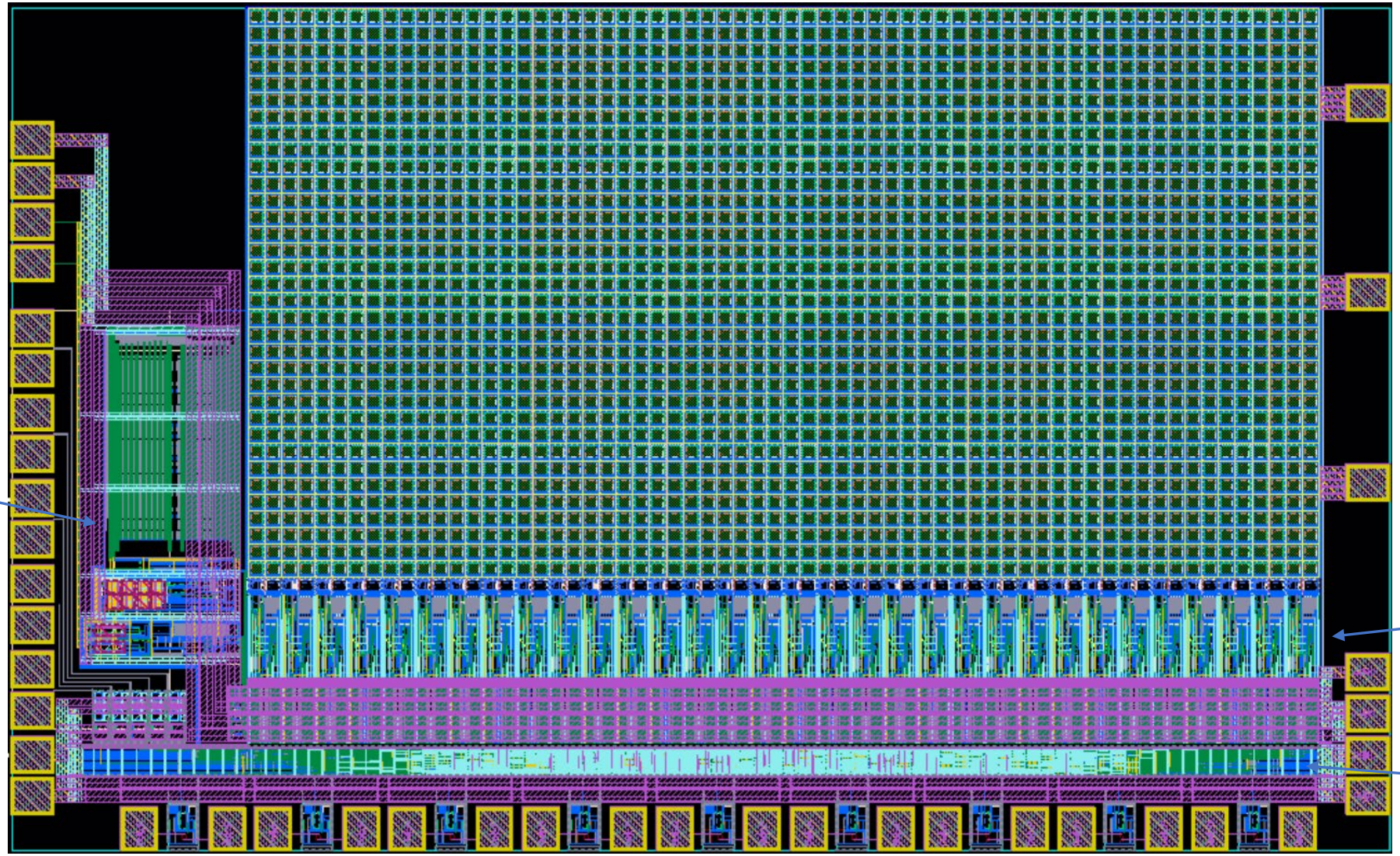
HALF MODULE:

- 32 macropixels divided into 8 groups;
- 8 delay equalized OR gates;
- 8 SLVS drivers for ROE outputs;
- Global bias: provides bias currents and voltages from a bandgap reference;
- Digital logic:
  - Slow control;
  - 1 MHz SLVS SPI link for data I/O

➢ Macropixels are organized into groups to reduce the area and power consumption of the SLVS drivers.

➢ No TDC in this prototype, timing measurements will be done by means of the oscilloscope.

HALF MODULE (prototype version): layout



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Features:

- LF110nm technology node;
- Power supply: 1.2 V;
- Area: about 7 mm^2;
- Double pixel flavour: 22 um and 51 um:
  - 2176 microcells for the 22 um;
  - 544 microcells for the 51 um;
- 32 channels per flavour;
- Whole SiPM area: about 1.9 mm^2 x 2 mm^2;
- Current consumption: 64 mA (62% due to SLSV driver for ROE);
- SiPM Bias adjustment:
  - About 460 mV range;
  - 8 global bits: 3.5 mV/LSB;
  - 6 local bits (1 sign + 5 pol.): 15 mV/LSB;
- Threshold adjustment:
  - 6 local bits (1 sign + 5 pol.): 1.8 mV/LSB (1/3 of 1phe @ Vov = 0.5 V);
- Internal injection for calibration;
- ToT current adjustment:
  - 5 global bits: 750 nA/LSB -> 1 phe pulse duration from 16 ns to 127 ns;
- Digital I/O: 1 MHz SLVS SPI link
- Package: CPGA 144