INFN/AExxx, LAL-xxx, SLAC-R-xxx

Super$B$ Detector Technical Design Report

Abstract

This report describes the technical design detector for Super$B$.

Contents

6 Silicon Vertex Tracker

6.1 Vertex Detector Overview

G.Rizzo - 12 pages

The Silicon Vertex Tracker, as in *BABAR*, together with the drift chamber (DCH) and the solenoidal magnet provide track and vertex reconstruction capability for the Super$B$ detector. Precise vertex information, primarily extracted from precise position measurements near the IP by the SVT, is crucial to the measurement of time-dependent CP asymmetries in B^0 decays, which remains a key element of the Super$B$ physics program. In addition, charged particles with transverse momenta lower than 100 MeV/c will not reach the central tracking chamber, so for these particles the SVT must provide the complete tracking information.

6.1.1 SVT and Layer0

These goals have been reached in the *BABAR* detector with a five-layer silicon strip detector. The *BABAR* SVT provided excellent performance for the whole life of the experiment, thanks to a robust design that took into account the physics requirements as well as enough safety margin, to cope with the machine background, and redundancy considerations. The Super$B$ SVT design is based on the *BABAR* vertex detector layout with the addition of an innermost layer closer to the IP (Layer0) as shown the in Fig. 6.3. The Layer0 close-in position measurements lead to an improved vertex resolution, which is expected to largely compensate for the reduced boost at the Super$B$, thus retaining the Δt resolution for B decays achieved in *BABAR*. Physics studies and background conditions, as explained in detail in the next sections, set stringent requirements on the Layer0 design: radius of about 1.5 cm; high granularity ($50 \times 50\,\mu\text{m}^2$ pitch); low material budget (about 1% X_0); and adequate radiation resistance.

Several options are under study for the Layer0 technology, with different levels of maturity, expected performance and safety margin against background conditions. These include striplets modules based on high resistivity sensors with short strips, hybrid pixels and other thin pixel sensors based on CMOS Monolithic Active Pixel Sensor (MAPS).

The current baseline configuration of the SVT Layer0 is based on the striplets technology, which has been shown to provide the better physics performance, as detailed in the next sections. However, options based on pixel sensors, which are more robust in high background conditions, are still being developed with specific R&D programs in order to meet the Layer0 requirements, which include low pitch and material budget, high readout speed and radiation hardness. If successful, this will allow the replacement of the Layer0 striplets modules in a "second phase" of the experiment. For this purpose the Super$B$ interaction region and the SVT mechanics will be designed to ensure rapid access to the detector for fast replacement of Layer0.

The external SVT layers (1-5), with a radius between 3 and 15 cm, will be built with the same technology used for the *BABAR* SVT (double sided silicon strip sensor), which is adequate for the machine background conditions expected in the Super$B$ accelerator scheme (*i.e.*with low beam currents).

The SVT angular acceptance, constrained by the interaction region design, will be 300 mrad in both the forward and backward directions, corresponding to a solid angle coverage of 95% in the center-of-mass frame.

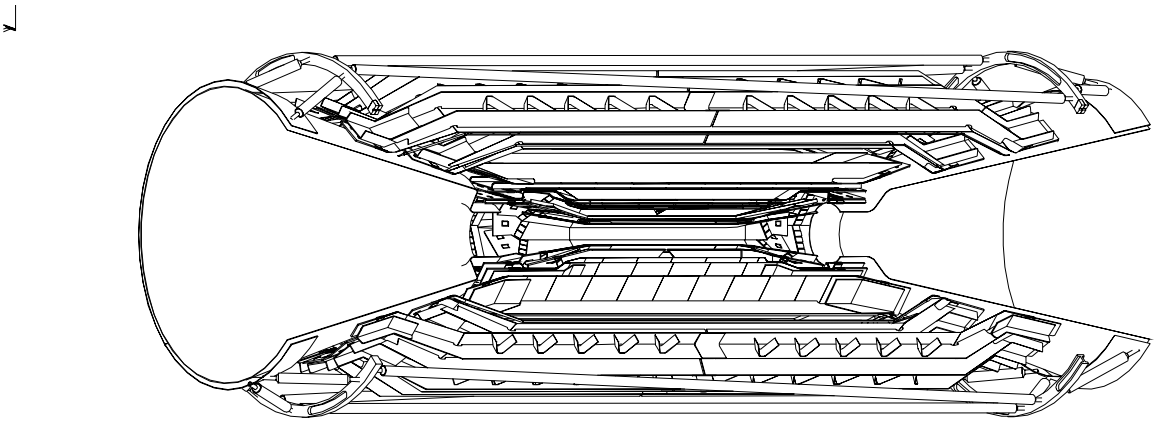

Figure 6.1: Three dimensional cutaway of the SVT.

6.1.2 Requirements

6.1.3 Baseline Detector Concept

6.1.3.1 Technology

6.1.3.2 Layout

6.1.3.3 Electronics

6.1.3.4 Mechanical Support

6.1.4 Layer0 Pixel Upgrade

6.1.4.1 Technology Options

6.1.4.2 Pixel Module Design

6.1.4.3 Mechanical Support and Cooling

6.1.5 R&D Main Activities

6.2 Backgrounds R.Cenci - 4 pages

6.3 Detector Performance Studies N.Neri - 6 pages

6.3.1 Introduction *(about 1/2 page)*

- write some considerations about the main differences between BaBar and SuperB (i.e. luminosity, boost, beampipe, beamspot);
- describe the main idea behind the new detector design focusing on performances;
- cite BaBar TDR and BaBar NIM paper as reference for strip detectors.

6.3.2 Impact of Layer0 on detector performances *(about 2 pages)*

- definition of Layer0 requirements for physics (material budget, inner radius vs boost, outer radius, intrinsic resolution, coverage);
- B^0 decay and tag vertex and B^0 proper time resolution for different solutions;
- baseline solution performances;
- discussion of pro and cons.

6.3.3 Sensitivity studies for time-dependent analyses *(about 2 pages)*

- studies of benchmark channels $B^0 \to \phi K^0_S$, $B^0 \to \pi^+\pi^-$, etc.;
- include time-dependent sensitivity studies at charm threshold?
- impact of background on detector performances.

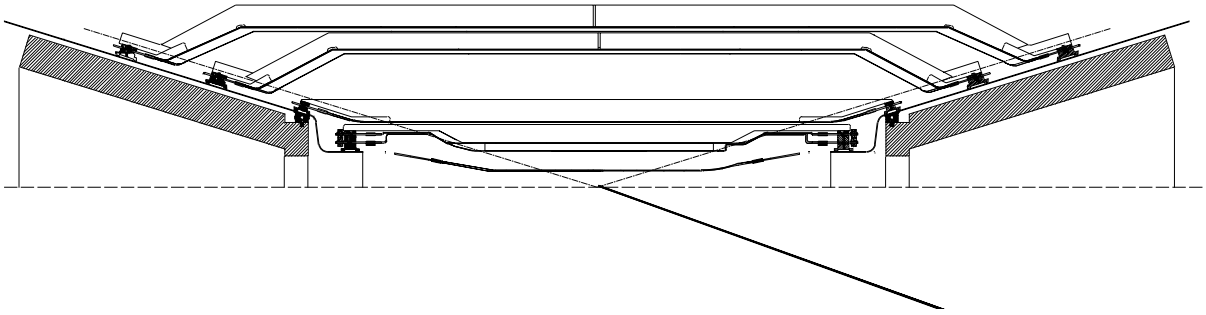

Figure 6.2: Cross section of the SVT in the plane containing the beam axis.

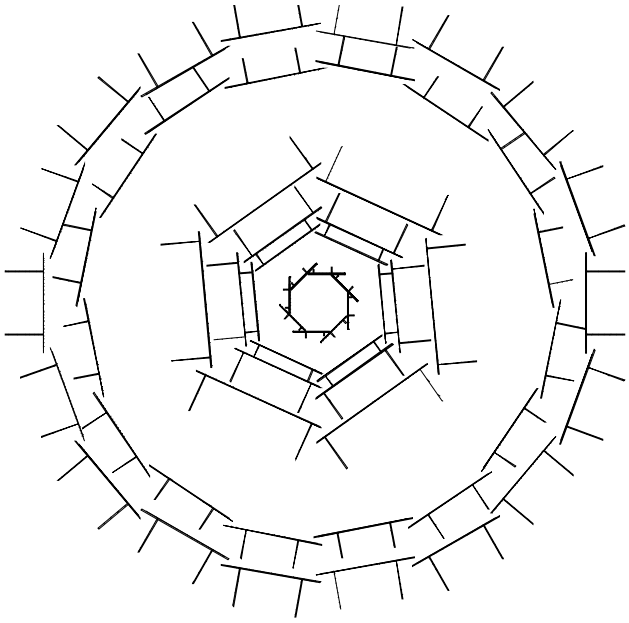

Figure 6.3: Cross section of the SVT in the plane perpendicular to the beam axis. The lines perpendicular to the detectors represent structural support beams.

6.3.4 Vertexing and Tracking performances *(about 1 pages)*

- track parameter resolutions;
- considerations for pattern recognition, efficiency vs numbers of layers, reconstruction capabilities for low momentum tracks, K^0_S reconstruction.

6.3.5 Particle Identification *(about 1/2 pages)*

- dE/dx resolution and relevance for QED pairs suppression.
- discussion of relevance of ToT information and number of bits of the FEE.

6.4 Silicon Sensors L. Bosisio - 8 pages

(Striplets will be discussed together with the other sensors)

Layers 1 to 5 of the SVT will be based on 300 μm thick double-sided silicon strip detectors, with integrated AC-coupling capacitors and polysilicon bias resistors. These devices are a technically mature and conservative solution to the requirements the SVT must meet to provide precise, highly segmented tracking near the interaction point. For the new layer 0, the baseline option also foresees double-sided silicon strip detectors, but with a thickness reduced to 200 μm. The detailed requirements which the detectors must meet are discussed below.

6.4.1 Requirements

To achieve good vertex resolution, it is especially important to minimize the material up to and including the first measurement. This requirement, and the need to provide precise vertexing in both z and ϕ, leads to the choice of double-sided detectors. Given the increased module length with respect to the BaBar SVT, in order to minimize the number of sensors required, the complexity of the assembly and the insensitive area between adjacent sensors and to ease the alignment task, we foresee to have the sensors fabricated on 150 mm diameter wafers, which is by now a widely available option from sensor suppliers. For layers 1 to 5 we plan to use 300 μm-thick silicon wafers, which are a standard choice and present acceptable handling properties. For layer 0, given the very stringent limitations on the amount of material we will be forced to go to 200 μm thick silicon. Processing double sided sensors on thin, 150 mm wafers is a significant challenge, which very few manufacturers are willing to tackle. Unfortunately, while the other layers could also be assembled from smaller sensors, fabricated on 100 mm wafers, layer 0 sensors do not fit in 100 mm wafers. This is due to the requirement to have only one sensor per layer 0 module, which in turn is dictated by the need to avoid insensitive regions and mechanical support structures, and also by limitations on the available number of readout channels. These difficulties are mitigated by the very small number of Mod. 0 sensors required and the fact that five of them can fit in a single 150 mm wafer. Because of this, a low fabrication and assembly yield can be tolerated.

6.4.1.1 Efficiency

The silicon detectors must maintain high single-point efficiency in order to achieve the requirements given in Section xxx for high overall track reconstruction efficiency and good tracking resolution. Loss of efficiency can occur from intrinsic strip inefficiencies, from bad interconnections, or from faulty electronics channels. Intrinsic strip inefficiencies can occur due to production defects which result in strips with unacceptably large leakage currents, from accidents during assembly causing the strip to be physically damaged, or from a breakdown in the AC-coupling capacitor. The latter problem is referred to as a pinhole and is due to a small hole in the oxide separating the implant from the metal readout strip above it. Pinholes can occur during fabrication, or they can be generated later on. Understanding and controlling the level of pinholes is one of the primary concerns in our program of silicon detector R&D.

Our goal is to achieve an overall single detector strip failure rate of less than 1%. Data from a large production of double-sided DC-coupled detectors (ALEPH) show that 60–70% can be achieved with a maximum inefficiency of 1%. On this basis, we expect that a 50% yield can be achieved for double-sided AC-coupled detectors while maintaining similar standards.

6.4.1.2 Resolution

As described in Section xxx, we have determined from Monte Carlo simulations [xxx] that the intrinsic point resolution should be 15μm or better in both z and ϕ for the inner layers. These are the point resolutions for tracks at near-normal incidence. As the angle between the track and the plane normal to the strip increases, the resolution degrades. We require the resolution to degrade by no more than a factor of approximately 3 for angles up to 75° ($\lambda \sim 1.3$) from normal.

6.4.1.3 Radiation hardness

A further requirement is that the quoted resolution values hold up to an integrated dose of ∼2 Mrad of ionizing radiation (electromagnetic in origin). This requirement leads to the use of AC-coupled detectors in order to avoid the problems associated with direct coupling of the large leakage currents which can occur at such large doses. It also has implications in the choice of the biasing scheme.

6.4.2 Sensor design

From the above requirements and from the discussion in Sections xxx, we have arrived at the detector specifications and design parameters which are described in this section. A more complete discussion can be found in Reference xxx.

Substrate and implant type. The wafers will be n-type, with a resistivity in the range 4–8 kΩ cm, corresponding to a depletion voltage of 40 to 80 V. These values seem to be a reasonable compromise between the need to have a low depletion voltage and the need to avoid type inversion in the presence of radiation damage.

We will employ p^+ strips on the junction side and n^+ strips on the ohmic side, with p^+-blocking implants in between; see Figure xxx for a cross-sectional view. This choice has proven to be a reliable technology xxx] which is directly available without extensive R&D.

Coupling to preamplifier. The strips are connected to the preamplifiers through a decoupling capacitor. AC coupling prevents the amplifier from integrating the leakage current with the signal; handling high leakage currents due to radiation damage imposes an additional burden on the preamplifier design and hasother undesirable operational implications.

The value of the decoupling capacitance must be much larger than the total strip capacitance, which is as large as 35 pF. Capacitors integrated on the detectors are the most compact solution, yielding a value for the decoupling capacitance of 30–80 pF/cm [xxx], depending on the implant width.

Bias resistors. The bias resistors must be between 4 and 20 MΩ. The lower limit is determined by two factors. The noise has a $1/\sqrt{R_B}$ dependence, and if several strips are ganged together, the effective resistance is correspondingly decreased. Another factor is the requirement that, for floating strips, the product $R_B \cdot C_{TOT}$ must be much larger than the amplifier peaking time (100–400 ns) to allow for capacitive charge partition. The upper limit (20) is dictated by the allowable potential drop due to the strip leakage current, which is taken to be 100 nA at maximum. A good target value is 8 MΩ. A final requirement is that the bias resistor be quite stable for the expected radiation doses.

To meet these requirements, we plan to use polysilicon bias resistors. Values of 50 kΩ/square for the sheet resistance of polysilicon can be achieved. Thus, it is possible to fabricate an 8 MΩ resistor with a 6 μm-wide, 960 μm-long polysilicon resistor. With a suitable shaping of the polysilicon line, the space required by the resistor will be 480 μm for a 25μm implant pitch.

Considering the space needed to accommodate the biasing resistors and to gracefully de-

Table 6.1: Physical dimensions, number of strips and pitches for the nine different sensor models.

Sensor Type	0	I	II	III	IVa	IVb	Va	Vb	VI
Dimensions (mm)									
z Length (L)	105.2	111.7	66.4	96.4	114.6	119.8	102.2	106.0	68.0
ϕ Width (W)	15.1	41.3	49.4	71.5	52.8	52.8	52.8	52.8	52.8-43.3
Thickness	0.20	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
PN junction side reads	u	z	z	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ
Strip Pitch (μm)									
z (u for Layer 0)	54	50	50	55	105	105	105	105	105
ϕ (v for Layer 0)	54	50	55	50	50	50	50	50	$50 \rightarrow 41$
Readout Pitch (μm)									
z (u for Layer 0)	54	100	100	110	210	210	210	210	
ϕ (v for Layer 0)	54	50	55	100	100	100	100	100	$100 \rightarrow 82$
Number of Readout Strips									
z (u for Layer 0)	1536	1104	651	865	540	565	481	499	318
ϕ (v for Layer 0)	1536	799	874	701	512	512	512	512	512

grade the electric field close to the edge with a guard ring structure, we specify the active region of the detectors to be 1.4 mm smaller than the physical dimensions (700 μm on each edge).

Optimization of z and ϕ readout strips. A major issue is which side of the detector (junction or ohmic) should read which coordinate (z or ϕ). The capacitance, and consequently, the noise is somewhat smaller on the junction side than on the ohmic side, and the strip pitch on the junction side can be 25μm, while on the ohmic side, it is limited to about 50μm because of the pre$p$-stop implant. For these reasons and because the z vertex measurement is more important from the point of view of physics, we use the junction side for the z strips on the inner layers. The better performance of the junction side also helps compensate for the additional resistance and capacitance imposed by the longer z fanout circuit.

In order to maintain acceptable signal-to-noise ratios for tracks at large dip angles, we employ a 100μm readout pitch for these z strips with one floating strip in between every two readout strips. We have considered using a wider readout pitch, for example, 200μm for the very forward and backward regions in order to increase the signal at large dip angles. However, this would involve yet another detector design, and based on our present estimates of achievable electronic noise, it does not appear to be necessary.

Acceptable resolution can be obtained for the ϕ strips on the inner layers using the ohmic side. Two solutions are possible; either a 50μm readout pitch without floating strips, since there is no room for them on the ohmic side, or a 100μm readout pitch with one floating strip. Either solution is feasible, and they should give roughly equivalent position resolution for single tracks. Double-track resolution is better for the first solution, and the noise contribution due to detector leakage currents is doubled in the latter solution. Therefore, preference goes to a 50μm readout pitch without floating strips. Although this choice has twice as many readout channels, the cost implications are not very important because the electronics cost is dominated by the development effort and consequently the per channel incremental cost is not significant.

Using the numbers in Table xxx, we see that the current design employs seven different types

Table 6.2: Number of the different sensor types per module, area of the installed sensors, number of installed sensors and number of sensors including spares. Spare sensors include one spare module per module type (two for layer 0) plus additional sensors accounting for possible losses during assembly of SVT.

Sensor Type	0	I	II	III	IVa	IVb	Va	Vb	VI	All
Layer0	1	-	-	-	-	-	-	-	-	1
Layer1	-	2	-	-	-	-	-	-	-	2
Layer2	-	-	4	-	-	-	-	-	-	4
Layer3	-	-	-	4	-	-	-	-		4
Layer4a	-	-	-	-	4	-	-	-	2	6
Layer4b	-	-	-	-	-	4	-	-	2	6
Layer5a	-	-	-	-	-	-	6	-	2	8
Layer5b	-	-	-	-	-	-	-	6	2	8
Silicon Area (m^2)	0.0127	0.0554	0.0787	0.166	0.194	0.203	0.201	0.302	0.222	1.51
Nr. of Sensors	8	12	24	24	32	32	54	54	68	308
Nr. Including Spares	20	20	40	35	44	44	72	72	92	439

of detectors (*i.e.* seven sets of masks) and needs 36 fabrication batches, for a total of 340 installed detectors. Having so many types of detectors complicates both the design and production phases, especially for prototype and spare production. A reduction in the number of detector types would be most welcome; however, this represents the minimum which we have been able to achieve in our present baseline design.

6.4.2.1 Technology choice

6.4.2.2 Optimization of strip layout

6.4.2.3 Wafer sizes and quantities

6.4.3 Prototyping and tests

6.5 Fanout Circuits L.Vitale - M.Prest4+4 pages

(Layer0 will be treated separately from the other ones)

6.5.1 Fanouts for layer0

6.5.1.1 Requirements

6.5.1.2 Technology

6.5.1.3 Design

6.5.1.4 Prototyping and tests

6.5.2 Fanouts for outer layers

6.5.2.1 Requirements

The requirements will be fixed by the detector designs. From the production point of view, the minimum line width is 15 μm with a space between the lines of 15 μm. With the present technology, it is not possible to go below these numbers. No constraints are present on the fanout length given the same machines used for the micropattern gas detector production will be used.

6.5.2.2 Material and production technique

The BaBar fanouts were produced on 50 μm Upilex (by UBE) with a deposit of 150 nm of Cr, 4.5 μm of copper followed by a layer of 150 nm of Cr and 1.5 μm of amorphous gold. The SuperB SVT fanouts will be produced on a similar material by UBE (50 μm of polyamide with 5 μm of copper directly deposited on the base material) which should ensure less defects and thus a better yield. This material will be tested in the prototype phase. The old Upilex is anyway still available if the new material would prove not adequate.

Table 6.3: List of different mask sets for 150 mm wafers, specifying the content of each wafer layout, the minimum value of the distance between the sensors and the wafer edge, the number of wafer required for each design and the total number of wafer. Quoted numbers include the spare sensors, but not the fabrication yield.

Mask Design	Wafer content	Min. Clearance to Wafer Edge (mm)	Number of Wafers
A	5×Mod 0	10.2	5
B	Mod I + Mod VI	8.2	20
C	Mod III	15.0	35
D	Mod IVa	11.9	44
E	Mod IVb	9.5	44
F	Mod IVb + Mod VI	9.8	72
G	Mod IVa + Mod II	6.9	72
Total			287

Table 6.4: Electrical parameters for the different detector types *Numbers to be updated.*

Detector Type	z-readout Side			ϕ-readout Side		
	C_{int} (pF/cm)	C_{AC} (pF/cm)	R_{series} (Ω/cm)	C_{int} (pF/cm)	C_{AC} (pF/cm)	R_{series} (Ω/cm)
I	1.3	40	7	2.8	40	7
II	1.3	40	7	2.8	40	7
III	1.3	40	7	2.8	40	7
IVa	1.5	80	3.5	1.3	40	7
IVb	1.5	80	3.5	1.3	40	7
Va	1.5	80	3.5	1.3	40	7
Vb	1.5	80	3.5	1.3	40	7
VI	1.5	80	3.5	1.3	30	9.2

A new technique for the production will be implemented in order to reduce the production times. In the BaBar production line, the photoresist was impressed through a mask after its being deposited on the Upilex requiring to work in a clean room. For SuperB, the idea is to impress the photoresist directly with a laser; this means the photoresist is solid and allows to complete the procedure in a much faster way. This technique has already been tested on the same pitches foreseen for the SVT fanouts.
The increase in the production speed allows to repeat the production of pieces with defects without delaying the SVT assembly. All the pieces will be gold plated with 1.5 μm of amorphous gold for the bonding.

6.5.2.3 Design

The design will follow the same rules of the BaBar fanouts adapting it to the different length of the modules. Differently from the BaBar pieces, no test-tree is foreseen (see next section). To allow the gold plating, all the lines will be shorted. A suitable cutting device will be developed to cut the shorting line after the visual inspection.

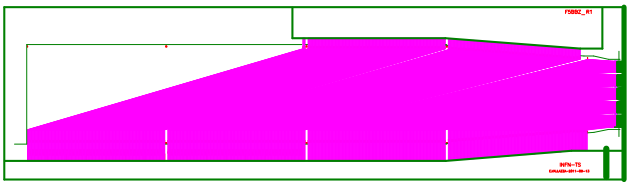

Figure 6.5: Design of a z fanout prototype.

The Table 6.5 summarizes the geometrical parameters as well as number of readout strips and channels, typical pitch and total number of required circuits per layer and type.

Figure 6.4 ...

Ganging vs pairing to be discussed (is this the proper place?).

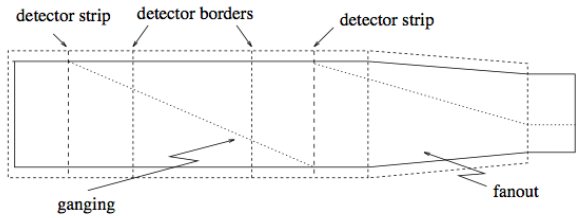

Figure 6.4: Schematic view of two z strips ganged with the fanout circuit.

6.5.2.4 Tests and prototyping

All the fanouts will be automatically optically checked by a dedicated machine which will use the gerber files of the fanouts to find shorts or open lines. The machine can work with 25 μm lines. The region with smaller lines (15 μm with a 15 μm space) corresponding to the bonding area (1.5 mm long and around 6 mm wide) will have to be controlled manually.
Given the much shorter time needed for the production, no correction is foreseen for shorts or open lines; the damaged pieces will be produced again. On the other hand, if a short is present in the larger pitch region, the same correction procedure used for BaBar (the use of a microprobe) can be implemented.

As far as the tests are concerned, a batch of fanouts will be produced starting from the BaBar design to check the whole production and test chain. These fanouts in principle can be used with working detectors to test also the assembly procedures.

Figure 6.5 shows the design of a z fanout prototype ... These prototypes were also used to measure the typical capacitance and average radiation thickness ...

6.6 Electronics Readout 28 pages

6.6.1 Readout chips V.Re - 10

6.6.1.1 Electronic Readout for Strip and Striplet Detectors

The front-end processing of the signals from the silicon strip detectors will be performed by custom-designed ICs mounted on hybrid circuits that distribute power and signals, and thermally interface the ICs to the cooling system. As discussed below, the very different features of inner (Layer 0-3) and outer layers (4 and 5) of the SVT set divergent requirements to the readout chips, which most probably makes it necessary to develop two distinct integrated circuits. This obviously holds also in the case a different technology (pixels) is adopted for Layer 0 instead of short strips (striplets). Generally speaking, both types of ICs will consist of 128 channels, each connected to a detector strip. The signals from the strips, after amplification and shaping will be compared to a preset threshold. If a signal exceeding the threshold is detected, a 3-4 bit analog information about the signal amplitude will be provided by an ADC: this will mostly serve for calibration and monitoring purposes in the innermost layers, whereas in outer layers it will be essential for dE/dx measurements. The dimensions of the readout IC are

Table 6.5: Summary of fanout circuit characteristics.

Layer	Fanout Type	Length (cm)	Number of Readout		Typical Pitch at		Number of Circuits
			Strips	Channels	Input(μm)	Output (μm)	
1	z					ROchip	12
	ϕ					50?	12
2	z						12
	ϕ						12
3	z						12
	ϕ						12
4a	z						16
	ϕ						16
4b	z						16
	ϕ						16
5a	z						18
	ϕ						18
5b	z						18
	ϕ						18

expected to be about 6×4 mm^2. As discussed in the SVT HDI subsection of this TDR, the dimensions of the HDI set a 6 mm upper limit on the side of the chip with the bonding pads for the interconnection with the strip sensors. The power dissipation will be about 4 mW/channel including both analog and digital sections. For each channel with a signal above threshold, the strip number, the amplitude information, the chip identification number and the related time stamp will be stored inside the chip waiting for a trigger signal for a time corresponding to the trigger latency (about 6 μs). When a trigger is received, data will be read out and transmitted off chip, otherwise they will be discarded. The data output from the microstrip detector will be sparsified, i.e. will consist only of those channels generating a hit. The readout integrated circuits must remain functional up to 5 times nominal background. The option of operating in a data push fashion could be preserved for the external layers, where this will be allowed by the low strip hit rate. This will give the possibility to feed data from these layers to the trigger system.

6.6.1.2 Readout chips requirements

The microstrip electronics must ensure that the detector system operates with adequate efficiency, but also must be robust and easy to test, and must facilitate testing and monitoring of the microstrip sensors. AC coupling is assumed between the strips and the readout electronics.

- **Mechanical Requirements:**
  Number of channels per chip: 128
  Chip size: width ≤6 mm, length ≤4 mm
  Pitch of input bonding pads: <45 μm

- **Operational Requirements:** Operating temperature: <40 °C
  Radiation tolerance: >3 Mrad/year, >5·10^{12} n_{eq}/cm^2/year
  Power dissipation: <4 mW/channel

- **Dynamic range:** The front-end chips must accept signals from either P and N-side of the strip detectors. A linear response of the analog processing section is required from a minimum input charge corresponding to 0.2 MIP up to a full dynamic range of 10-15 MIP charge for dE/dx measurements.

- **Analog Resolution:** The front-end chips have to provide an analog information about the charge collected in the detector, which will be also used for calibrating and monitoring the system. A resolution of 0.2 MIP charge is required for dE/dx measurements. In case of a compression-type ADC characteristic, this may translate in 3-4 bits of information.

- **Efficiency:** At design luminosity, the microstrip readout must have a hit efficiency of at least 95% during its entire operational lifetime. This includes any loss of data by readout electronics or readout dead time.

- **Readout bandwidth:** Data coming out of the chip will be substantially reduced by operating in a triggered mode. The chips can use up to 4 output LVDS lines, as it is needed to handle the higher data throughput in inner SVT layers.

- **Radiation Tolerance:** All the components of the microstrip readout system must remain operational up to 10 years of SuperB running at the nominal luminosity.

- **Peaking Time:** The constraints for the peaking time of the signal at the shaper output are dictated by different needs in inner and outer layers. In Layer 0, the high occupancy due to background and the need to avoid pulse overlap and consequent hit inefficiencies set the maximum peaking time at t_p=25 ns, which also allow for a high timing resolution (see below). In the external layers, where background hit frequency is much smaller and where strips are longer and have a larger capacitance, the peaking time will be mostly determined by the need of reducing series noise contributions and has to be in the range of 0.5-1.0 μs.

- **Signal-to-Noise Ratio:** Concerning the signal, this requirement has to take into account the different thickness of silicon detectors in inner (200 μm) and outer (300 μm) layers, as well the signal spread among various strips that depends on the track angle inside detectors and that, again, may vary in different SVT layers. Noise-related parameters (strip capacitance and distributed resistance) also sizably vary across the SVT. A signal-to noise ratio of 20 has to be ensured across the whole SVT and should not increase significantly after irradiation. Here are the two extreme cases (where the equivalent noise charge ENC includes the thermal noise contribution from the distributed resistance of the strips):

  – Layer 0 striplets: ENC ≈700 e- at C_D=10 pF and at t_p=25 ns

  – Layer 5 strips: ENC ≈1000 e- at C_D=70 pF and at t_p=1 μs

- **Threshold and Dispersion:** Each microstrip channel will be read out by comparing its signal to a settable threshold around 0.2 MIP. Threshold dispersion must be low enough that the noise hit rate and the efficiency are degraded to a negligible extent. Typically, this should be 300 rms electrons at most and should be stable during its entire operational lifetime.

- **Comparator Time Resolution:** The comparator must be fast enough to guarantee that the output can be latched in the right time stamp period.

- **Time Stamp:** 30 ns time stamp resolution is required for inner layers to get a good hit time resolution in order to reduce the occupancy in the offline time window (50-100 ns). In the outer layers the time stamp resolution is less critical since the hit time resolution will be dominated by the long pulse shaping time. A single 30 ns time stamp clock in all layers will be used.
- **Chip clock frequency:** Two main clocks will be used inside the readout chip, the time stamp clock (33 MHz) and the readout clock (132 MHz or 198 MHz). These clocks will be synchronized with the 66 MHz SuperB system clock. In case the analog-to-digital conversion is based on the Time-Over-Threshold (TOT) method, a ToT clock has to be generated inside the chip. The TOT clock period should at least match the pulse shaping time to get a good analog resolution. A faster TOT clock could slightly improve the analog resolution but an upper limit (≈3.5) on the ratio between TOT clock frequency and the shaping time frequency is imposed by the required dynamic range needed for low momentum particle dE/dx measurements (≈10-15 MIP) and the number of bits available for TOT. With the experience of the BaBar Atom chip a TOT clock frequency 3 times higher than the pulse shaping frequency could be used: 120 MHz (*60 MHz are probably ok too??*) for L0, 60 MHz for L1-2, 15 MHz for Layer3 and 6-3 MHz for L4-5.
- **Mask, Kill and Inject:** Each micro-strip channel must be testable by charge injection to the front-end amplifier. By digital control, it shall be possible to turn off any micro-strip element from the readout chain.
- **Maximum data rate:** Simulations show that machine-related backgrounds dominate the overall rates. At nominal background levels, the maximum hit rate per strip is 2 MHz/strip in Layer 0 (45 MHz/cm^2), 0.7 MHz/strip in Layer 1, 0.4 MHz/strip in Layer 2. These numbers include a safety factor of 5.
- **Deadtime limits:** The maximum total deadtime of the system must not exceed 10 % at a 150 kHz trigger rate and background 5 times the nominal expected rate.
- **Trigger specifications:** The trigger has a nominal latency of 7 μs, a maximum jitter of 0.1 μs, and the minimum time between triggers is 70 ns. The maximum Level 1 Trigger rate is 150 kHz.
- **Cross-talk:** Must be less than 2 %.
- **Control of Analog Circuitry on Power-Up:** Upon power-up, the readout chip shall be operational at default settings.
- **Memory of Downloaded Control of Analog Circuitry:** Changes to default settings shall be downloadable via the readout chip control circuitry, and stored by the readout chip until a new power-up cycle or additional change to default settings.
- **Read-back of Downloadable Information:** All the data that can be downloaded also shall be readable. This includes data that has been modified from the default values and the default values as applied on each chip when not modified.
- **Data Sparsification:** The data output from the microstrip detector shall be only of those channels that are above the settable threshold.
- **Microstrip output data content:** The microstrip hit data must include the time stamp, chip identification number, and the microstrip hits (strip number and relevant signal amplitude) for that time stamp. The output data word for each strip hit should contain 25-30 bits (7 strip address, 9 TS, 1 data valid, 4 chip address, 4 TOT or 7 ADC, 2 additional bits).

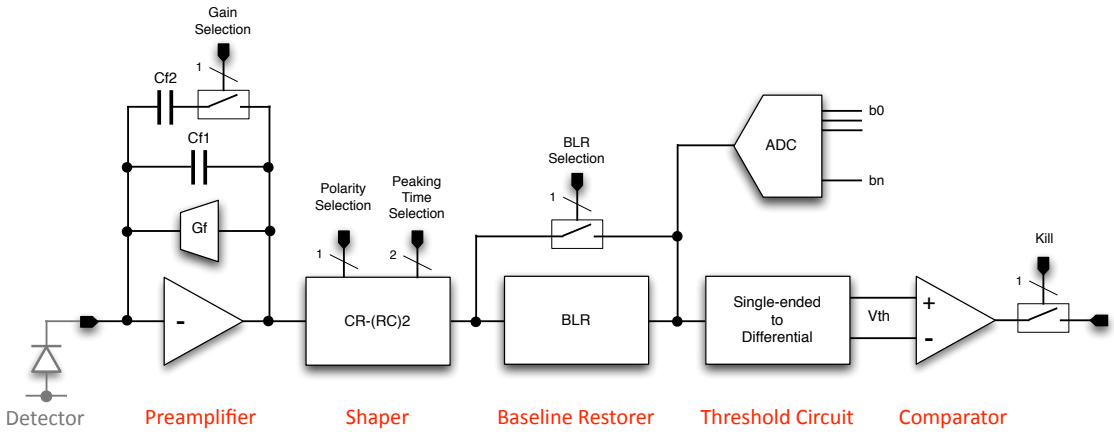

Figure 6.6: Analog channel block diagram.

6.6.1.3 Readout Chip Implementation

The SuperB SVT readout chips are mixed-signal integrated circuits in a 130 nm CMOS technology and are being designed to comply with the requirements discussed above. Each chip comprises 128 analog channels, each consisting of a charge-sensitive preamplifier, a unipolar semi-Gaussian shaper and a hit discriminator. A polarity selection stage will allow the chip to operate with signals delivered both from n- and p-sides of the SVT double-sided strip detectors. A symmetric baseline restorer may be included to achieve baseline shift suppression. When a hit is detected, a 3-4 bit analog-to-digital conversion will be performed by a Flash ADC or by means of a Time-Over-Threshold (TOT) detection. The hit information will be buffered until a trigger is received; together with the hit time stamp, it will be then transferred to an output interface, where data will be serialized and transmitted off chip on output LVDS lines. An n-bit data output word will be generated for each hit on a strip. A programming interface accepts command and data from a serial input bus and programmable registers are used to hold input values for DACs that provide currents and voltages required by the analog section. These registers have other functions, such as controlling data output speed and selecting the pattern for charge injection tests.

Given the very different requirements of inner and outer layers, in terms both of detector parameters and hit frequency, two different chips will be designed; they will be based on a same data protocol, but will be optimized for operation at different clock frequencies. The block diagram of the analog channel is shown in Fig. 6.6.

The digital readout of the matrix will exploit the architecture that was originally devised for a high-rate, high-efficiency readout of a large CMOS pixel sensor matrix. Each strip has a dedicated array of pre-trigger buffers, which can be filled by hits with different time stamps. The size of this buffer array is determined by the maximum strip hit rate (inner layers) and by the trigger latency. After arrival of a trigger, only hits with the same time stamp as the one provided by the triggering system send their information to the back-end. The array of 128 strips is divided in four sections, each with a dedicated sparsifier encoding the hits in a single clock cycle. The storage element next to each sparsifier (barrel level-2) acts like a FIFO memory conveying data to a barrel-L1 by a concentrator which merges the flux of data and preserves the time order of the hits. This barrel-L1 will drive the output data bus which will use up to four output lines depending on the data throughput and will be synchronous to a 120 MHz clock.

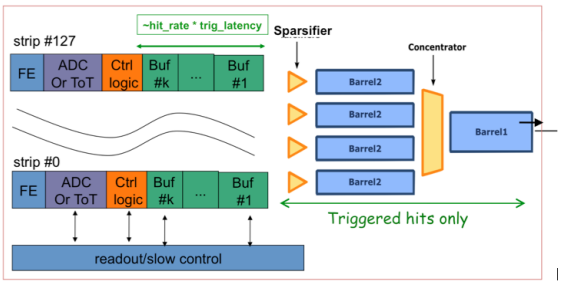

Figure 6.7: Readout architecture of the SVT strip readout chips.

6.6.1.4 R&D for strip readout chips

The R&D to support the development of the SuperB strip readout chips has begun in 2011. The chosen technology for integration is a 130 nm CMOS process: this has an intrinsically high degree of radiation resistance, which can be enhanced with some proper layout prescriptions such as enclosed NMOS transistors and guard rings. There is a large degree of experience with mixed-signal design in this CMOS node that was gained in the last few years inside the HEP community.

The readout architecture is being tested with realistic data created by Monte Carlo analysis of the interaction region. Verilog simulations demonstrate that the chip will be able to operate with a 99 % readout efficiency in the worst case condition, which includes the safety factor of 5 in the background levels.

The analog section of the chip is being optimized from the standpoint of noise, comparator threshold dispersion and sensitivity to variations of process parameters. It will be possible to select the peaking time of the signal at the shaper output (25-100 ns for inner layers, 400 ns-2 μs for outer layers) by changing the value of capacitors in the shaper. In this way the noise performances of the chip can be optimized according to the signal occupancy, preserving the required efficiency. Table 6.6 shows the main parameters of the analog section, according to simulation estimates for realistic values of detector parameters and strip hit rates. The loss in efficiency is determined by the limits in the double pulse resolution of the analog section, which depends on the signal peaking time. An acceptable compromise will be found here with the noise performance.

In 2012, the submission of two chip prototypes including 64 analog channels and a reduced-scale version of the readout architecture is foreseen.

The submission of the full-scale, 128-channels chip prototypes is then scheduled in late 2013. This version will have the full functionality of the final production chip.

6.6.2 Hybrid Design M.Citterio - 10

6.6.3 Data Transmission M.Citterio - 10

6.6.4 Power Supply - 2

6.7 Mechanical Support & Assembly S.Bettarini/F.Bosi - 14 pages

- Introduction

6.7.1 I.R. Constraint

- Description of the IR components: Be-pipe, L0, SVT, W shielding, QD0
- Active region definition and clearances
- Mechanical architecture (how each components is constrained to what)
- Staging area assembly
- Quick demounting motivations and removable support cage concept

6.7.2 Module Assembly

- L0 module baseline components and assembly procedure
- L 1-5 module components and assembly procedure

6.7.3 Detector Assembly and Installation

6.7.3.1 Half Detector Assembly

- L0 module assembly on the cold flanges
- Cold flanges descriptions, required features and jig

Table 6.6: Main parameters of the analog section of the SVT strip readout chips.

Layer	C_D [pF]	Available $t_p[ns]$	Selected $t_p[ns]$	ENC from R_S [e rms]	ENC [e rms]	Channel width [μm]	Hit rate/strip [kHz]	Efficiency 1-N
0	11.2		25	220	740		1370	0.948
1	26.7	25, 50	100	460	940	3000	429	0.959
2	31.2	100, 200	100	590	1100		268	0.976
3	34.4		200	410	940		105	0.982
4	52.6	400, 600,	500	490	1000		17.5	0.993
		800, 1000	600	440	940	9000		-
5	67.5	(or 500	800	560	1090			-
		and 1000)	1000	500	1030		11.3	0.990

- L 1-5 module assembly on the Support cones
- Support cones, buttons, cooling ring description, required features and jig
- Space frame features

6.7.3.2 Mount L0 on the Be-pipe and L 1-5 on the W Shielding

- HDMF assembly description for L0 on the be-pipe
- HDMF assembly for the L 1-5 on the W shielding
- Displacement w.r.t. the IR
- Gimbal ring and support cage description
- Optical modules survey
- Electrical testing and connection to the transition Card

6.7.3.3 Installation of Complete Assembly into the SuperB Detector

- Constrains and scenario of mounting, stiffness and clearance required

6.7.3.4 Quick Demounting

- Infrastructure required and SVT demounting/mounting procedure

6.7.4 Detector Placement and Survey

6.7.4.1 Placement accuracy

6.7.4.2 Survey with tracks

6.7.5 Detector Monitoring

6.7.5.1 Position Monitoring System

6.7.5.2 Radiation Monitoring

6.7.6 R&D Program

6.7.6.1 Cables

6.7.6.2 hybrid

6.7.6.3 Inner layer sextant

6.7.6.4 Arch modules

6.7.6.5 Cones and space frame

6.7.6.6 Full-scale model of IR

6.8 Layer0 Upgrade Options

G.Rizzo/L.Ratti - 10 pages

With the machine operated at full luminosity, the layer 0 of the silicon vertex tracker may ben-

efit from upgrading the layer0 to a pixellated detector. This solution can actually provide some significant advantages with respect to the baseline striplet option. In particular

- the occupancy per detector element from machine background is expected to fall to a few kHz, with a major impact on the speed specifications for the front-end electronics, mainly set by the background hit rate in the case of the striplet readout chip;
- better accuracy in vertex reconstruction can be achieved with a detector pitch of 50 μm or smaller; the shape of the pixel can be optimized in such a way to reduce the sensor pitch in the z direction while keeping the area in the range of 2500-3000 μm^2, which guarantees enough room for sparse readout functionalities.

A few technology alternatives for pixel detector fabrication are being investigated and R&D activity is in progress to understand advantages and potential issues of the different options.

6.8.1 Technology options

Following is a description of the technology options that are being considered for the upgrade of the SuperB SVT innermost layer.

6.8.1.1 Hybrid pixels

Hybrid pixel technology has reached quite a mature stage of development. Hybrid pixel detectors are currently used in the LHC experiments [9, 10, 11, 12], with pitch in the range from 100 μ to a few hundred μm, and miniaturization is being further pushed forward in view of the upgrade of the same experiments at the High Luminosity LHC (HL-LHC) [32, 14, 15]. Hybrid pixel systems are based on the interconnection between a sensor matrix fabricated in a high resistivity substrate and a readout chip. Bump-bonding with indium or indium-tin or tin-lead alloys is the mainstream technology for readout chip-to-sensor interconnection. The design of a hybrid pixel detector for the SVT innermost layer has to meet some challenging specifications in terms of material budget and spatial resolution. Since the readout chip and the sensor are laid one upon the other, hybrid pixels are intrinsically thicker detectors than microstrips. Interconnect material may further degrade the performance, significantly increasing the radiation length equivalent thickness of the detector. As far as the readout and sensor chips are concerned, substrate thinning to 100-150 μm and subsequent interconnection are within present technology reach. Further thinning may pose some issues in terms of mechanical stability and, as the detector thickness is reduced, of signal-to-noise ratio and/or front-end chip power dissipation. Concerning interconnection, the vertical integration processes currently under investigation in the high energy physics community might help reduce the amount of material. Among the commercially available technologies, the ones provided by the Japanese T-Micro (formerly known as ZyCube), based on so called micro-bumps, and by the US based company Ziptronix, denoted as direct bonding technique, seem the most promising [16]. The Fraunhofer EMFT has developed a bonding technique called SLID and based on a very thin eutectic Cu-Sn alloy to interconnect the chips [17]. The spatial resolution constraints set a limit to the area of the elementary readout cell and, as a consequence, to the amount of functionalities that can be included in the front-end electronics. A planar, 130 nm CMOS technology may guarantee the required density for data sparsification and in-pixel time stamping in a 50 μm$\times$50 μm pixel area (as already observed, a different aspect ratio might be preferred to improve the resolution performance in one particular direction). The above mentioned interconnection techniques can fully comply with the detector pitch requirements (in the case of the T-Micro technology, pitches as small as 8 μm can be achieved). A fine pitch (30 μm minimum), more standard bump-bonding technology is also provided by IZM. This technology has actually been successfully used to bond the SuperPIX0 front-end chip (to be described later on in this section) to a 200 μm thick pixel detector.

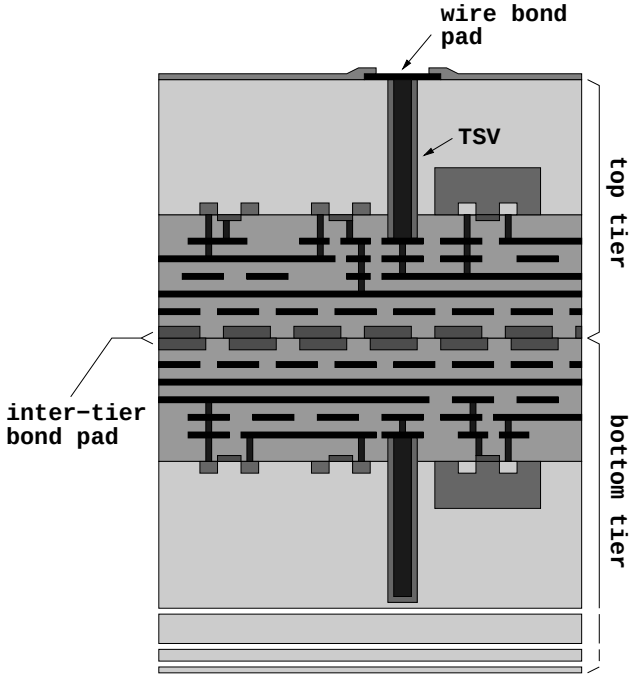

Figure 6.8: cross-sectional view of a double-layer 3D process.

Denser CMOS technologies (belonging to the 90 or 65 nm technology) can be used to increase the functional density in the readout electronics and include such functions as gain calibration, local threshold adjustment and amplitude measurement and storage. In this case, costs for R&D (and, eventually, production) would increase significantly. Vertical integration (or 3D) CMOS technologies may represent a lower cost alternative to sub-100 nm CMOS processes. The technology cross section shown in Fig. 6.8, in particular, points to the main features of the extremely cost-effective process provided by Tezzaron Semiconductor [18] which was used for the design of the SDR1 chip. The Tezzaron process can be used to vertically integrate two (or more) layers, specifically fabricated and processed for this purpose by Chartered Semiconductor (now Globalfoundry) in a 130 nm CMOS technology. In the Tezzaron/Chartered process, wafers are face-to-face bonded by means of thermo-compression techniques. Bond pads on each wafer are laid out on the copper top metal layer and provide the electrical contacts between devices integrated in the two layers. The top tier is thinned down to about 12 μm to expose the through silicon vias (TSV), therefore making connection to the buried circuits possible. Among the options available in the Chartered technology, the low power (1.5 V supply voltage) transistor option was chosen. The technology also provides 6 metal layers (including two top, thick metals), dual gate option (3.3 V I/O transistors) and N- and P-channel devices with multiple threshold voltages. The main advantages deriving from a vertical integration approach to the design of a hybrid pixel front-end chip can be summarized as follows:

- since the effective area is twice the area of a planar technology from the same CMOS node, a better trade-off can be found between the amount of integrated functionalities and detector pitch;
- separating the digital from the analog section of the front-end electronics can effectively prevent digital blocks from interfering with the analog section and from capacitively coupling to the sensor through the bond pad.

The design of a 3D front-end chip for pixel detectors is in progress in the framework of the VIPIX experiment funded by INFN.

6.8.1.2 Deep N-well CMOS monolithic sensors

Deep N-well (DNW) CMOS monolithic active pixel sensors (MAPS) are based on an original design approach proposed a few years ago and developed in the framework of the SLIM5 INFN experiment [4]. The DNW MAPS approach takes advantage of the properties of triple well structures to lay out a sensor with relatively large area (as compared to standard three transistor MAPS [19]) read out by a classical processing chain for capacitive detectors. As shown by the technology cross section in Fig. 6.9, the sensor, featuring a buried N-type layer with N-wells (NW) on its contour according to a typical deep N-well scheme, collects the charge released

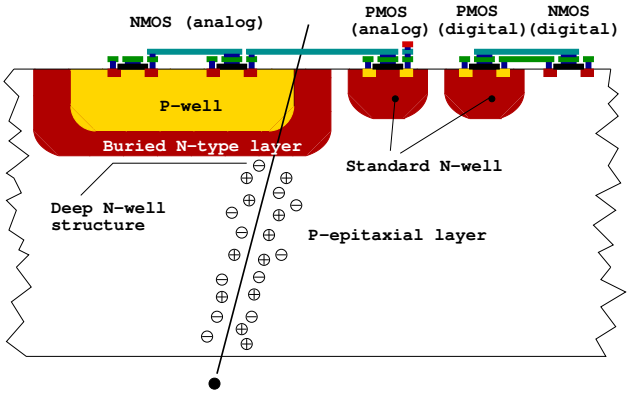

Figure 6.9: simplified cross-sectional view of a DNW MAPS. NMOS devices belonging to the analog section may be built inside the sensor, while the other transistors cover the remaining area of the elementary cell, with PMOSFETs integrated inside standard N-wells.

by the impinging particle and diffusing through the substrate, whose active volume is restricted to the uppermost 20-30 μm thick layer below the collecting electrode. Therefore, within this extent, substrate thinning is not expected to significantly affect charge collection efficiency, while improving momentum resolution performance in charged particle tracking applications. As mentioned above, DNW MAPS have been proposed chiefly to comply with the intense data rates foreseen for tracking applications at the future high energy physics (HEP) facilities. The area taken by the deep N-well collecting electrode can actually be exploited to integrate the NMOS parts of the analog front-end inside the internal P-well. A small amount of standard N-well area can be used for PMOS devices, instrumental to the design of high performance analog and digital blocks taking full advantage of CMOS technology properties. In this way, both analog functions, such as signal shaping, and digital functions, such as time stamping and data storing, buffering and sparsification, can be included in the pixel operation. Note that the presence of N-wells other than the sensor is instead strongly discouraged in standard MAPS design, where the operation of the tiny collecting electrode would be jeopardized by the presence of any N-type diffusion in the surrounding. Based on the concept of the DNW monolithic sensor, the MAPS detectors of the Apsel series (see Section 6.8.2.2), which are among the first monolithic sensors with pixel-level data sparsification [20, 21], have been developed in a planar, 130 nm CMOS technology. In 2008, the Apsel4D, a DNW MAPS with 128×32 elements has been successfully tested at the Proton Synchrotron facility at CERN [24]. More recently, vertical integration technologies, like the ones discussed in the previous section for hybrid pixels, have been considered for the design of 3D DNW monolithic sensors. Some specific advantages can derive from such an approach to DNW MAPS. In particular, all the PMOS devices used in digital blocks can be integrated in a different substrate from the sensor, therefore significantly reducing the amount of N-well area (with its parasitic charge collection effects) in the surroundings of the collecting electrode and improving the detector charge collection efficiency (CCE). The first prototypes of 3D DNW MAPS [27, 28] have been submitted in the framework of the 3D-IC collaboration [26]. Characterization has started in the last quarter of 2011.

6.8.1.3 Monolithic pixels in CMOS quadruple well technology

In DNW MAPS, charge collection efficiency can be negatively affected, although to a limited extent, by the presence of competitive N-wells including PMOS transistors of the pixel readout chain, which may subtract charge from the collecting electrode. Inefficiency is related to the relative weight of N-well area with respect to the DNW collecting electrode area. A novel approach for isolating PMOS N-wells has been made available with a planar 180 nm CMOS process called INMAPS, featuring a quadruple well structure [21]. Fig. 6.10 shows a simplified cross section of a pixel fabricated with the INMAPS process. By means of an additional processing step, an high energy deep P-well im-

plant is deposited beneath the PMOS N-well (and not under the N-well diode acting as collecting electrode). This implant creates a barrier to charge diffusing in the epitaxial layer, preventing it from being collected by the positively biased N-wells of in-pixel circuits and enabling a theoretical charge collection efficiency of 100%. The NMOS transistors are designed in heavily doped P-wells located in a P-doped epitaxial layer which has been grown upon the low resistivity substrate. Epitaxial layers with different thickness (12 or 18 μm) and resistivity (standard about 50 Ω·cm, and high resistivity, 1 kΩ·cm) are available. The epitaxial layer may obviously play an important role in improving charge collection performance. Actually, carriers released in the epitaxial layer are kept there by the potential barriers at the P-well/epi-layer and epi-layer/substrate junctions. A test chip, including several different test structures to characterize both the readout electronics and the collecting electrode performance has been submitted in the third quarter of 2011.

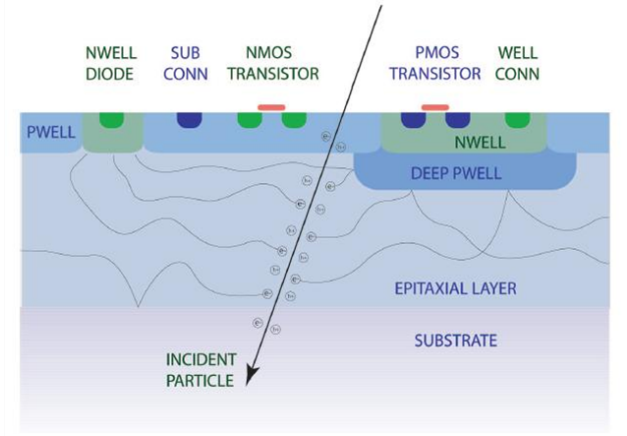

Figure 6.10: cross-sectional view of the INMAPS CMOS technology; emphasis is put on the deep P-well layer.

6.8.2 R&D activity

6.8.2.1 Front-end electronics for hybrid pixels in planar and 3D CMOS technology

A prototype hybrid pixel detector named SuperPIX0 has been designed as a first iteration step aimed at the development of a device to be used for the layer0 upgrade. The main novelties of this approach are the sensor pitch size (50×50μm) and thickness (200μm) as well as the custom front-end chip architecture providing a sparsified and data-driven readout. The SuperPIX0 pixel sensor is made of n-type, Float Zone, high-resistivity silicon wafers, with a nominal resistivity larger than 10 kΩ. The SuperPIX0 chip, fabricated in the STMicroelectronics 130nm CMOS technology, is composed of 4096 channels (50x50 μm^2) arranged into 128 columns by 32 rows. Each cell contains an analog charge processor (shown in Fig. 6.11) where the sensor charge signal is amplified and compared to a chip-wide preset threshold by a discriminator. The in-pixel digital logic, which follows the comparator, stores the hit in an edge-triggered set reset flip-flop and notifies the periphery of the hit. The charge sensitive amplifier uses a single-ended folded cascode topology, which is a common choice for low-voltage, high gain amplifier. The 20 fF MOS feedback capacitor is discharged by a constant current which can be externally adjusted, giving an output pulse shape that is dependent upon the input charge. The peaking time increases with the collected charge and is in the order of 100 ns for 16000 electrons injected. The charge collected in the detector pixel reaches the preamplifier input via the bump bond connection. Alternatively, a calibration charge can be injected at the preamplifier input through a 10 fF internal injection capacitance so that threshold, noise and crosstalk measurements can be performed. The calibration voltage step is provided externally by a dedicated line. Channel selection is performed by means of a control section implemented in each pixel. This control block, which is a cell of a shift register, enables the injection of the charge though the calibration capacitance. Each pixel features a digital mask used to isolate single noisy channel. This mask is implemented in the readout logic. The input device (whose dimensions were chosen based on [22]) featuring an aspect ratio W/L=18/0.3 and a

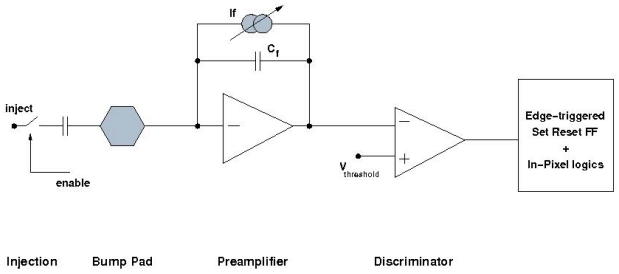

Figure 6.11: block diagram of the analog front-end electronics for the elementary cell of the SuperPIX0 readout chip.

drain current of about 0.5 μA, is biased in the weak inversion region. A non-minimum length has been chosen to avoid short channel effects. The PMOS current source in the input branch has been sized to have a smaller transconductance than the input transistor. For a detector capacitance of 100 fF, an equivalent noise charge of 150 e- rms was obtain from circuit simulations. The noise contribution arising from the leakage current can be neglected for the leakage current range considered in the simulations (0-2 pA). 2 pA corresponds to ten times the anticipated leakage current for the pixel sensor. An overall input referred threshold dispersion of 350 e- rms was computed from Monte-Carlo simulations. Since SuperPIX0 is the first iteration step aimed to the development of a readout chip for small pitch hybrid pixel sensors, in this design only the main functionalities have been integrated in the pixel cell. Threshold dispersion is a crucial characteristic to be considered in order to meet the required specifications in terms of noise occupancy and efficiency. Therefore, circuits for threshold fine-adjusting have to be implemented in the next version of the chip. The analog front-end cell uses two power supplies. The analog supply (AVDD) is referenced to AGND, while the digital supply is referenced to DGND. Both supplies have a nominal operating value of 1.2 V. Since single-ended amplifiers are sensitive to voltage fluctuations on the supply lines, the charge preamplifier is connected to the AVDD. The threshold discriminator and voltage references are connected to the AVDD and AGND as well. The in-pixel digital logic is connected to the digital supply. The substrate of the transistors is connected to a separate net and merged to the analog ground at the border of the matrix. The SuperPIX0 chip has been fabricated in a six metal level technology. Special attention has been paid to layout the channel with a proper shielding scheme. Two levels of metal have been used to route the analog signals, two for the digital ones and two for distributing the analog and digital supplies. The supply lines, at the same time, shield the analog signals from the digital activity. For nominal bias conditions the power consumption is about 1.5 μW per channel. More details on the design of the analog front-end can be found in the literature [23].

6.8.2.2 The Apsel DNW MAPS series

DNW MAPS in planar CMOS technology

Deep N-well MAPS were proposed a few years ago as possible candidates for charged particle tracking applications. The Apsel4D chip is a 4096 element prototype MAPS detector with data-driven readout architecture, implementing twofold sparsification at the pixel level and at the chip periphery. In each elementary cell of the MAPS matrix integrated in the Apsel4D chip, a mixed signal circuit is used to read out and process the charge coming from a deep N-well (DNW) detector. This design approach relies upon the properties of the triple well structures included in modern CMOS processes for NMOS transistor isolation and is intended to enable sparsified readout directly at the sensor level, as described in Section 6.8.1.2. In the so called DNW MAPS, we integrate a relatively large (as compared to standard three transistor MAPS) collecting electrode, featuring a buried N-type layer, with a classical readout chain for time invariant charge amplification and shaping. In the Apsel4D prototype, the elementary MAPS cells feature a 50 μm pitch and a power dissipation of about 30 μW/channel. The block diagram of the pixel analog front-end electronics is shown in Fig. 6.12. The first block of the processing chain, a charge preamplifier, uses a

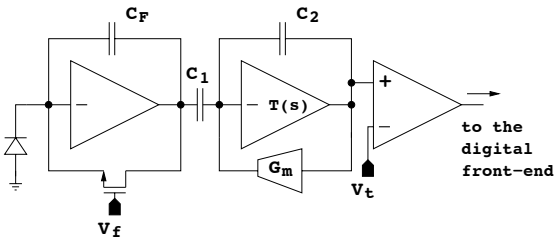

Figure 6.12: block diagram of the analog front-end electronics for the elementary cell of the Apsel4D prototype.

complementary cascode scheme as its forward gain stage, and is responsible for most of the power consumption in the analog section. The feedback capacitor C_F is continuously reset by an NMOS transistor, biased in the deep subthreshold region through the gate voltage V_f. The preamplifier input device, featuring an aspect ratio $W/L = 14/0.25$ and a drain current of 20 μA, was optimized for a DNW detector about 900 μm^2 in area and with a capacitance C_D of about 300 fF. The charge preamplifier is followed by a CR-RC, bandpass filtering stage, with open loop gain $T(s)$, featuring a programmable peaking time which can be set to 200 or 400 ns. C_1 is a differentiating capacitor at the CR-RC shaper input, while G_m and C_2 are the transconductance and the capacitance in its feedback network. A discriminator is used to compare the processed signal to a global voltage reference V_t, thereby providing hit/no-hit information to the cell digital section. More details on the design of the analog front-end can be found in the literature [25]. A dedicated readout architecture to perform on-chip data sparsification has been implemented in the Apsel4D prototype. The readout logic provides the timestamp information for the hits. The timestamp, which is necessary to identify the event to which the hit belongs, is generated by the bunch-crossing signal. The key requirements in this development are 1) to minimize logical blocks with PMOS inside the active area, thus preserving the collection efficiency, 2) to reduce to a minimum the number of digital lines crossing the sensor area, in particular its dependence on detector size to allow the readout scalability to larger matrices and to reduce the residual crosstalk effects, and 3) to minimize the pixel dead time by reading hit pixels out of the matrix as soon as possible. With these criteria a readout logic in the periphery of the matrix has been developed, as schematically shown in Fig 6.13. To minimize the number of digital lines crossing the active area the matrix is organized in MacroPixels (MP) with 4x4 pixels. Each MP has only two private lines for point-to-point connection to the peripheral logic: one line is used to comunicate that the MP has got hits, while the second private line is used to freeze the MP until it has been read out. When the matrix has some hits the columns containing fired MPs are enabled, one at the time, by vertical lines. Common horizontal lines are shared among pixels in the same row to bring data from the pixels to the periphery, where the association with the proper timestamp is performed before sending the formatted data word to the output bus. The chip has been designed with a mixed mode design approach. While the pixel matrix has a full custom design and layout, the periphery readout architecture has been synthetized in standard cell starting from a VHDL model; automatic place-and-route tools have been used for the layout of the readout logic [20]. The chip has been designed to run with a readout clock

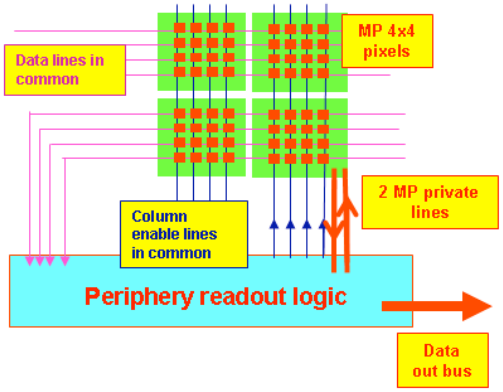

Figure 6.13: schematic concept of the architecture for MAPS matrix readout.

up to 100 MHz (20 MHz in test beam), a maximum matrix readout rate of 32 hit pixels/clock cycle and a local buffer of maximum 160 hits to minimize the matrix sweep time. Apsel4D has been successfully tested with 12 GeV/c protons at the PS-T9 beam line at CERN [24]. The efficiency of the DNS MAPS as a function of threshold for two devices with different silicon thickness (Chip 22 is 300 μm thick, while Chip 23 is 100 μm thick) has been measured. Figure 6.14 shows the measured hit efficiency, determined as described in [24]. At the low-

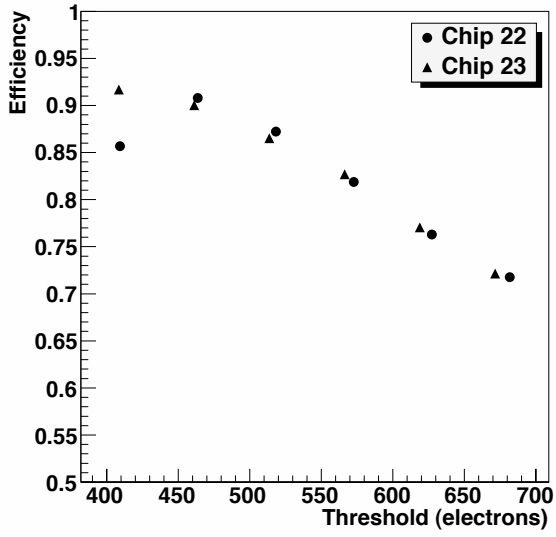

Figure 6.14: efficiency results for two MAPS detectors (the statistical uncertainty on each point is smaller than the size of the plotting symbol).

est thresholds we observe a maximum efficiency of approximately 92% and we see the expected general behavior of decreasing efficiency with increasing threshold. The noise occupancy for this range of thresholds varied from 2.5×10^{-3} to 1×10^{-6}. The low efficiency observed for Chip 22 at the lowest threshold appears to have been caused by a readout malfunction. Investigations have shown that a small localized area on the detector had very low efficiency, while the rest of the detector behaved normally with good efficiency. Additionally, we have studied the efficiency for detecting hits as a function of the track extrapolation point *within a pixel*. Since the pixel has internal structure, with some areas less sensitive than others, we expect the efficiency to vary as a function of position within the cell. The uncertainty on the track position, including multiple scattering effects is roughly 10 microns, to be compared to the 50 μm pixel dimension. We divide the pixel into nine square sub-cells of equal area and measure the hit efficiency within each sub-cell. The efficiencies thus obtained are "polluted" in some sense due to the migration of tracks among cells. We obtain the true sub-cell efficiencies by unfolding the raw results, taking into account this migration, which we characterize using a simple simulation. The result can be seen in Figure 6.15, where we show the efficiency measured in each sub-cell. One observes a significant variation of sensibility within the pixel area, as expected. In particular, the central region is seen to be virtually 100% efficient, while the upper part of the pixel, especially the upper right-hand subcell, shows lower efficiency due to the presence of competitive n-wells. We note that the position of this pixel map relative to the physical pixel is not fixed. This is a consequence of the alignment, which determines the absolute detector position by minimizing track-hit residuals, as described above. If the pixel area is not uniformly efficient, the pixel center as determined by the alignment will correspond to the barycenter of the pixel efficiency map. Thus, it is not possible to overlay Figure 6.15 on a drawing of the pixel layout, without adding additional information, for example a simulation of internal pixel efficiency. The efficiency as a function of position on the MAPS matrix has also been investigated, since disuniformity could indicate inefficiencies caused by the readout. We have generally observed uniform efficiency across the area of the MAPS matrix. We measure the intrinsic resolution σ_{hit} for the MAPS devices as described in [24]. The expected resolution for cases where the hit consists of a single pixel is given by $50/\sqrt{12} = 14.4$ μm, where 50 microns is the pixel dimension.

DNW MAPS in 3D CMOS technology

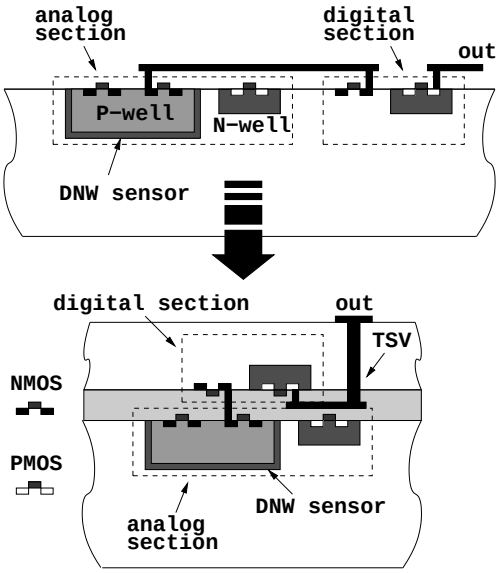

Figure 6.16: cross-sectional view of a DNW CMOS MAPS: from a planar CMOS technology to a 3D process

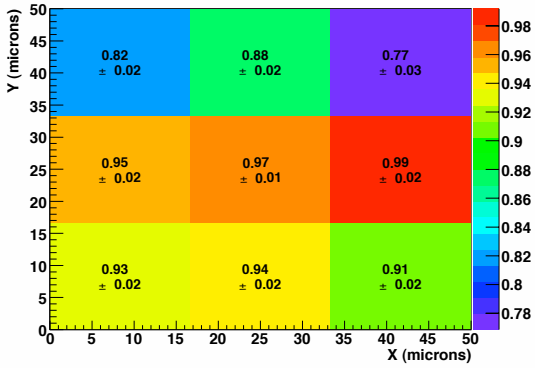

Figure 6.15: hit effiencies measured as a function of position within the pixel (the picture, which is not to scale, represents a single pixel divided into nine sub-cells).

6.8.2.3 The Apsel4well quadruple well monolithic sensor

6.8.3 Radiation tolerance

Hybrid pixels. The high degree of radiation tolerance of modern CMOS technologies, coming as a byproduct of the aggressive scaling down of device minimum feature size, is having a beneficial impact in high energy physics (HEP) applications. Beginning with the 130 nm CMOS processes, which entered the sub-3 nm gate oxide thickness regime, direct tunneling contribution to the gate current has assumed a significant role as compared to trap assisted mechanisms [29]. This may account for the very high degree of radiation hardness featured by devices belonging to the most recent technology nodes, which might benefit from relatively fast annealing of holes trapped in the ultrathin gate oxides. Tolerance to a few hundred of Mrad(SiO_2) has been recently proven in front-end circuits for hybrid pixel detectors [32]. Charge trapping in the thicker shallow trench isolation (STI) oxides is considered as the main residual damage mechanism in 130 nm N-channel MOSFETs exposed to ionizing radiation [30, 31], especially in narrow channel transistors [33]. Ionizing radiation was found to affect also the 90 nm and 65 nm CMOS nodes, although to an ever slighter extent, likely due to a decrease in the substrate doping concentration and/or in the STI thickness. As far a as analog front-end design is concerned, ionizing radiation damage mainly results in an increase in low frequency noise, which is more significant in multifinger devices operated at a small current density. This might be a concern in the case of the front-end electronics for hybrid pixel detectors, where the input device of the charge preamplifier is operated at drain currents in the few μA range owing to low power constraints. However, at short peaking times, typically below 100 ns, the effects of the increase in low frequency noise on the readout channel performance is negligible. Also, use of enclosed layout techniques for the design of the preamplifier input transistor (and of devices in other critical parts of the front-end) minimizes the device sensitivity to radiation [**?**]. For this purpose, Fig. 6.17 shows the noise voltage spectrum for a 130 nm NMOS transistor with enclosed layout, featuring no significant changes after irradiation with a 100 Mrad(SiO_2) total ionizing dose. On the other hand, CMOS technologies are virtually insensitive to bulk damage, since MOSFET

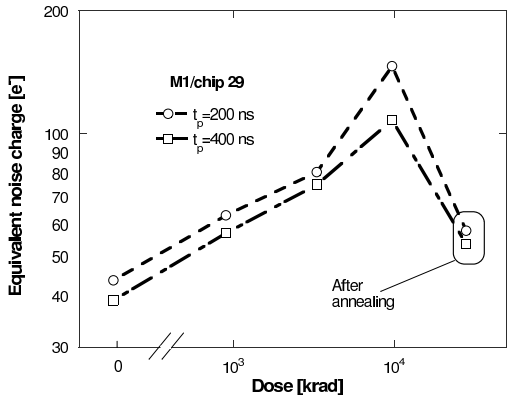

Figure 6.18: equivalent noise charge as a function of the absorbed dose and after the annealing cycle for DNW monolithic sensor. ENC is plotted for the two available peaking times.

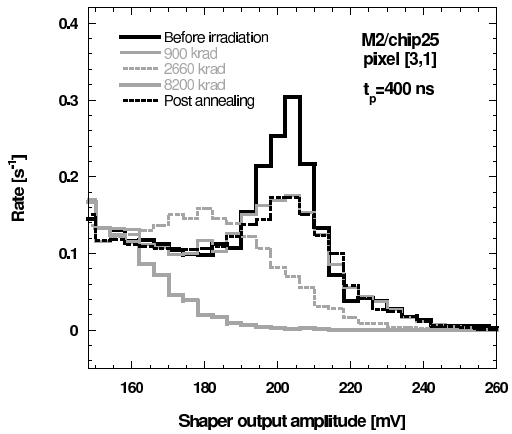

Figure 6.19: event count rate for a DNW monolithic sensor exposed to a ^{55}Fe source before irradiation, after exposure to γ-rays and after the annealing cycle.

transistor operation is based on the drift of majority carriers in a surface channel.

DNW CMOS MAPS DNW MAPS have been thoroughly characterized from the standpoint of radiation hardness to evaluate their limitations in harsh radiation environments. In particular, the effects of ionizing radiation, with total doses of about 10 Mrad(SiO_2), have been investigated by exposing DNW MAPS sensors to a ^{60}Co source [**?**]. In that case, some performance degradation was detected in the noise and gain of the front-end electronics and in the sensor leakage current, while no significant change was observed as far as the charge collection properties are concerned. Fig. 6.18 shows the equivalent noise charge as a function of the absorbed dose and after the annealing cycle for a DNW monolithic sensor. The significant change can be ascribed to the increase in the flicker noise of the preamplifier input device as a consequence of parasitic lateral transistors being turned on by positive charge buildup in the shallow trench isolation oxides and contributing to the overall noise. Use of an enclosed layout approach is expected to significantly reduce the effect of ionizing radiation. Fig. 6.19 shows event count rate for a DNW monolithic sensor exposed to a ^{55}Fe source before irradiation, after exposure to γ-rays and after the annealing cycle. As

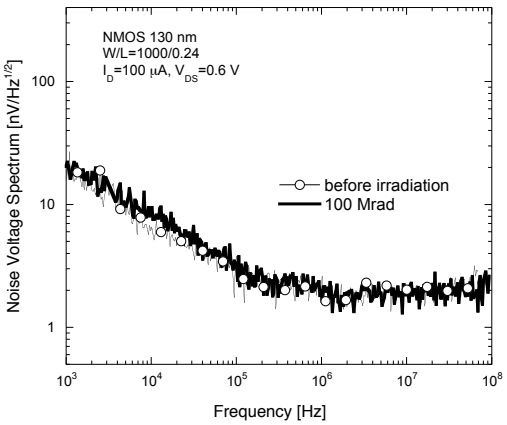

Figure 6.17: noise voltage spectrum for a 130 nm NMOS device with enclosed layout.

the absorbed dose increases, the 5.9 keV peak gets broader as a consequence of the noise increase (in fair agreement with data in Fig. 6.18. At the same time, the peak is shifted towards lower amplitude values, as a result of a decrease in the front-end charge sensitivity also due to charge build up in the STI of some critical devices. Recently [**?**], DNW MAPS of the same kind have been irradiated with neutrons from

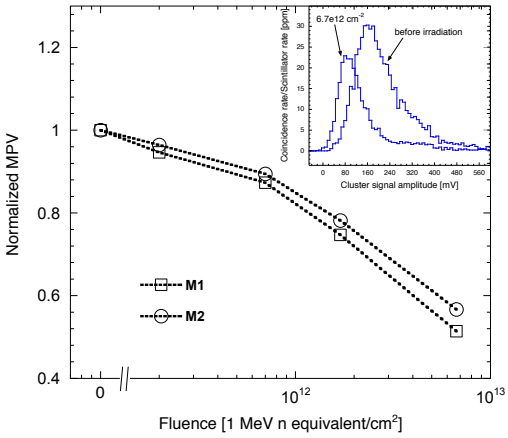

Figure 6.20: most probable value (MPV) of the ^{90}Sr spectra (shown in the inset for one of the tested chips before irradiation and after exposure to a 6.7×10^{12} cm^{-2} neutron fluence) normalized to the pre-irradiation value as a function of the fluence for DNW MAPS with different sensor layout.

a Triga MARK II nuclear reactor to test bulk damage effects. The final fluence, 6.7×10^{12} 1 MeV neutron equivalent/cm^2, was reached after a few, intermediate steps. The devices under test (DUT) were characterized by means of several different techniques, including charge injection at the front-end input through an external pulser, sensor stimulation with an infrared laser and spectral measurements with ^{55}Fe and ^{90}Sr radioactive sources. Neutron irradiation was found to have no sizable effects on the front-end electronics performance. This can be reasonably expected from CMOS devices, whose operation is based on the drift of majority carriers in a surface channel, resulting in a high degree of tolerance to bulk damage. Exposure to neutrons was instead found to affect mainly the charge collection properties of the sensors with a reduction in the order of 50% at an integrated fluence of about 6.7×10^{12} cm^{-2}. Fig. 6.20 shows the most probable value (MPV) of the ^{90}Sr spectra normalized to the pre-irradiation value as a function of the fluence for DNW MAPS with different sensor layout. A substantial decrease can be observed, to be ascribed to a degradation in the minority carrier lifetime. A higher degree of tolerance was instead demonstrated in monolithic sensors with high resisitivity (1 kcm) epitaxial layer [35]. Actually, doping concentration plays a role in determining the equilib- rium Fermi level, which in turn influences the effectiveness of neutron-induced defects as recombination centers [**?**].

6.9 Services, Utilities and E.S. & H issues - 8 pages

6.9.1 Service and Utilities

- Data and control lines
- Power
- Cooling water
- Dry air or nitrogen

6.9.2 ES&H Issue

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