RDO update

P. Antonioli – INFN Bologna

→ no time to check with RDO team, let's discuss!

December 16, 2025

Links & topics

Status of dRICH DAQ thinking @ SRO XIII → Pietro 9/12/2025
RDO status @ test beam → Sandro 11/12/2025
test beam overview @ TIC → Marco 15/12/2025

Topics

- Hardware status
- Lessons learned from first production / test beam
- Lessons to be learned yet from first production
- TODO
- 2026 schedule + test beam

Hardware status

Sandro@ePICItaly

BEFORE
BEAM TEST

- **Only 9 out of 10 RDOs** were validated before beam test.
- **One RDO was damaged** during beam test preparation.
- No additional RDOs and few FAKE-FEB spares!

AFTER
BEAM TEST

- **One RDO stops communicating with host**, due to a faulty connection of the VTRx+ (seen only after the beam test).
- Power management of the board is stable, but **noise induced effect on the LTM** input has been highlighted.
- Despite IPbus limitation, tested data taking even with high DCR!

- 6 RDO up and working, with SI5326 mounted (SN: 2, 4, 5, 7, 8, 9)
- 2 RDO up and working, with a second Si5519 wrongly mounted (SN 0, 1)
- 1 RDO not working “wrong IDCODE” --> some hope to recover (SN 3)
- 1 RDO not working : Artix damaged following wrong LV during debug → dead (SN 6)

Hardware status (II)

Full hardware database available on INFN OneDrive

Board	Posizione	Guai hardware noti	Atmel PRG	Artix PRG	PolarFire PRG	Note	EXT CLK	Setting resistors for maximum LDO currents	Post test-beam interventions
#0(Lotto1)	BO	Si5319 instead of Si5326; wrong charge pump	OK	OK	OK		Jumper su ckext (R64,R65)	Cambiata R35 da 3.3K a 2.2K per portare Imax su 1.8V a 1363mA e R53 da 2K ad 1.5K per portare Imax su 0.85V a 2A	
#1(Lotto1) Office on the web Frame	BO	Si5319 instead of Si5326; wrong charge pump ;TMP119 TOP not working	OK	OK	OK		Jumper su ckext (R64,R65)	Cambiata R35 da 3.3K a 2.2K per portare Imax su 1.8V a 1363mA e R53 da 2K ad 1.5K per portare Imax su 0.85V a 2A	Reinserite: capacità C51 con patch (era stata rimossa per evitare corto sulla +1.0V causa footprint errato); C86 e C33 che erano state tolte per rimuovere C51. Modificate R95-R101 da 33 a 100 ohm per diminuire la luminosità dei led di monitoring delle alimentazioni. Rimosse le 2 rondelle sui dadi del morsettino che blocca la fibra (toccavano il case dei mosfet traslatori sugli enable delle tensioni)
#2	BO		OK	OK	OK		Jumper su ckext (R64,R65)	Cambiata R35 da 3.3K a 2.2K per portare Imax su 1.8V a 1363mA e R53 da 2K ad 1.5K per portare Imax su 0.85V a 2A	
#3	BO		OK	OK	OK		Jumper su ckext (R64,R65)	Cambiata R35 da 3.3K a 2.2K per portare Imax su 1.8V a 1363mA e R53 da 2K ad 1.5K per portare Imax su 0.85V a 2A; R36 a 15K per mancanza 21K	
#4	BO		OK	OK	OK		Jumper su ckext (R64,R65)	Cambiata R35 da 3.3K a 2.2K per portare Imax su 1.8V a 1363mA e R53 da 2K ad 1.5K per portare Imax su 0.85V a 2A	
#5	BO		OK	OK	OK	Non erano montat1 FL1 ed FL2 (portano 1.8V ad U7 ed U13), sostituiti con goccia di stagno	Jumper su ckext (R64,R65)	Cambiata R35 da 3.3K a 2.2K per portare Imax su 1.8V a 1363mA e R53 da 2K ad 1.5K per portare Imax su 0.85V a 2A	
#6	Giovanni		OK	NO	NO	Corto sulla 0.85V e sulla 1.8V	40MHz on board	Cambiata R35 da 3.3K a 2.2K per portare Imax su 1.8V a 1363mA e R53 da 2K ad 1.5K per portare Imax su 0.85V a 2A	
#7	BO		OK	OK	OK		Jumper su ckext (R64,R65)	Cambiata R35 da 3.3K a 2.2K per portare Imax su 1.8V a 1363mA e R53 da 2K ad 1.5K per portare Imax su 0.85V a 2A	
#8	BO		OK	OK	OK	Non era montato C51, ora montato. C41 e C57 montati male. Su C41 montata una capacità da 10nF al posto di 100nF per indisponibilità in package 0201	Jumper su ckext (R64,R65)	Cambiata R35 da 3.3K a 2.2K per portare Imax su 1.8V a 1363mA e R53 da 2K ad 1.5K per portare Imax su 0.85V a 2A	
#9	BO		OK	OK	OK		Jumper su ckext (R64,R65)	Cambiata R35 da 3.3K a 2.2K per portare Imax su 1.8V a 1363mA e R53 da 2K ad 1.5K per portare Imax su 0.85V a 2A	

Lessons learned from first production/test beam

- bringing RDO up took time, now it will be better → think hard about test points / additional I/O for debug
- SAMTEC connector (ALCOR bus) somehow fragile (→ procedures!) plus “how to lock?”
- ARTEL made some errors mounting, but for production we should safe

Lists of changes to be done

- fix resistors / foot print bug on capacitors etc.
- all ALCOR bus “LVDS”
- monitor output LV of LDO via microprocessor
- replacement of microprocessor
- reshuffle several Artix PIN due scrubbing requests (CSI/CSO)
- replace Tantalium capacitor
- VTRX+ “shield”
- ….

Lessons yet to be learned

- power control via I2C RDO of fake-FEB / FEB
- several pieces of hardware still completely "untested" (Si5326, I2C interface with VTRX+)
- several key functionalities still completely "untested" (scrubbing + remote programming + FULL/lpGBT protocol -> clock)
- are the ARTIX resources enough?
- will the cooling requirements impact on RDO layout?
- should/can we reduce power consumptions? How?

TODO toward rev. 1

1. I2C interface with Attiny + VTRX+
2. FEB I2C power control
3. LV instabilities/noise/sense
4. Si5326 programming
5. all scrubbing machinery
    a. PolarFire – Artix bus
    b. Flash programming
    c. scrubbing
    d. setup irradiation test to test scrubbing
6. remote programming
7. FULL/lpGBT implementation
    a. tests with ePIC FMC card
    b. clock reconstruction
    c. ALCOR readout via reconstructed clock
    d. sync test on (3)
8. RDO inside PDU
    a. ALCOR64 readout
    b. noise tests (including charge pump and EMI)
    c. cooling
    d. check all ALCOR64 features (including shutter)
    e. VTRX+ shielding / cage
9. μC replacement
10. DAQ firmware requests and FPGA resources
    1. current fw optimization
    2. time ordering algorithm + data format
    3. data transmission to ePIC FMC card
    4. data transmission to VC709/VC707 ?
    5. data transmission to FELIX (note collaboration with ALICE DAQ)
11. irradiation tests (see next)

+ “RDO test card”

Irradiation tests

tested SAMD21 microprocessor:

in short:
- RAM SEU lower than measured by CERN (O(10-14 cm2/bit) instead of O(10-12 cm2/bit)
- dead for TID > 8 krad (between 8 and 30 krad) → rethink test methodology at high doserate?

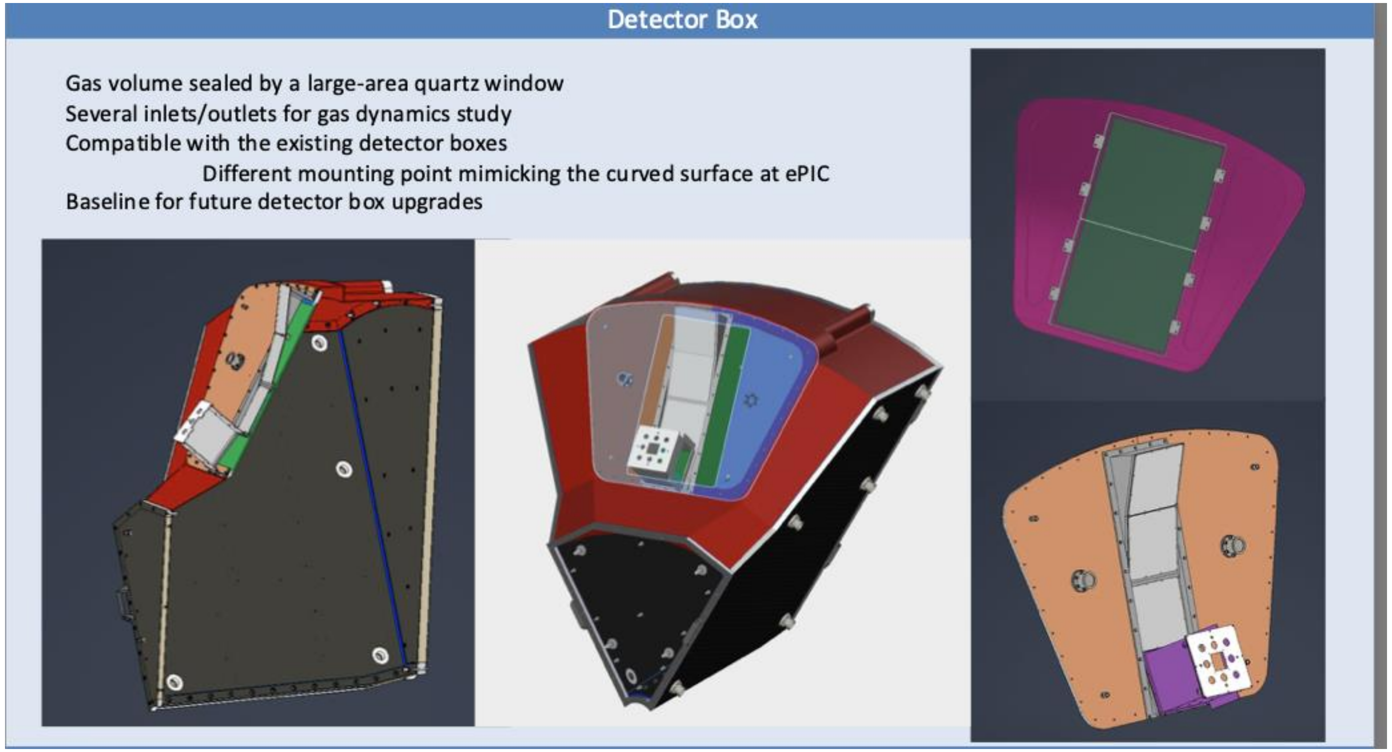
Needed tests:

1. scrubbing (Artix only)
2. full RDO with all radiation tolerance measures deployed: microprocessor + scrubbing + "Si5236/Si5319" watchdog
3. compare FULL and lpGBT FEC5 (this could be done irradiating just Artix+VTRX+ using a shield)
4. we might have separate tests for microprocessor (SAM21 again) and charge pump
5. full PDU test to CHARM ?

- March: 1, 4 and perhaps 3 (Trento)
- September: 2 (Trento)
- CHARM seems complicated especially considering (a) our assigned time for test beam (b) LHC schedule

We should agree on TID requirement: 2.3 krad has factor 5 safety
So 8 krad is a factor 20 safety. Isn't it enough?

Beam test(s) 2026 & RDO



test beam: 10 – 26 June
no RDO rev.1 will be available
how many RDOs we need?
should we produce additional RDOs rev. 0 for

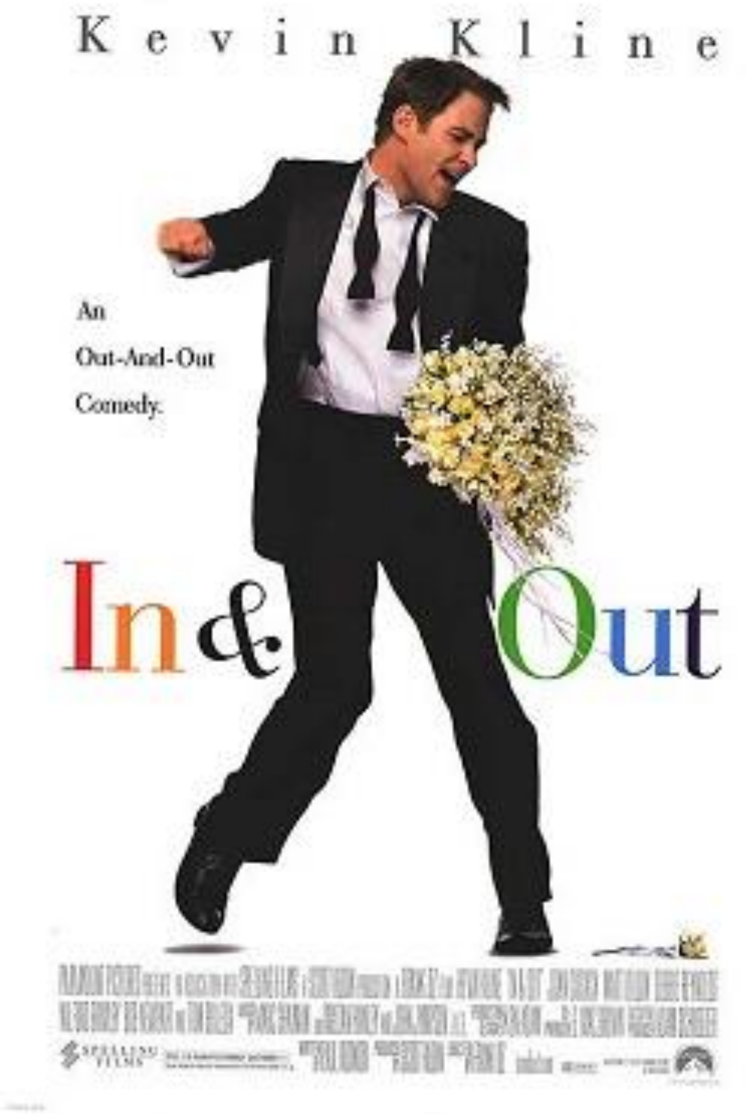
Miscellanea / Questions / open discussions

- somewhere in Spring “DAQ day” to bring all different stakeholders for discussions re: data reduction/data format (bring also electronics people)
- do we need additional Rev.0 RDO?
- impact of new EIC schedule (see Domenico @ ePIC Italy)?

What is “in” & what is “out” in this talk

dRICH design / dRICH recap
Data throughput modelling
ALCOR latest developments
RDO and FELIX roles
RDO latest developments
Data reduction latest developments

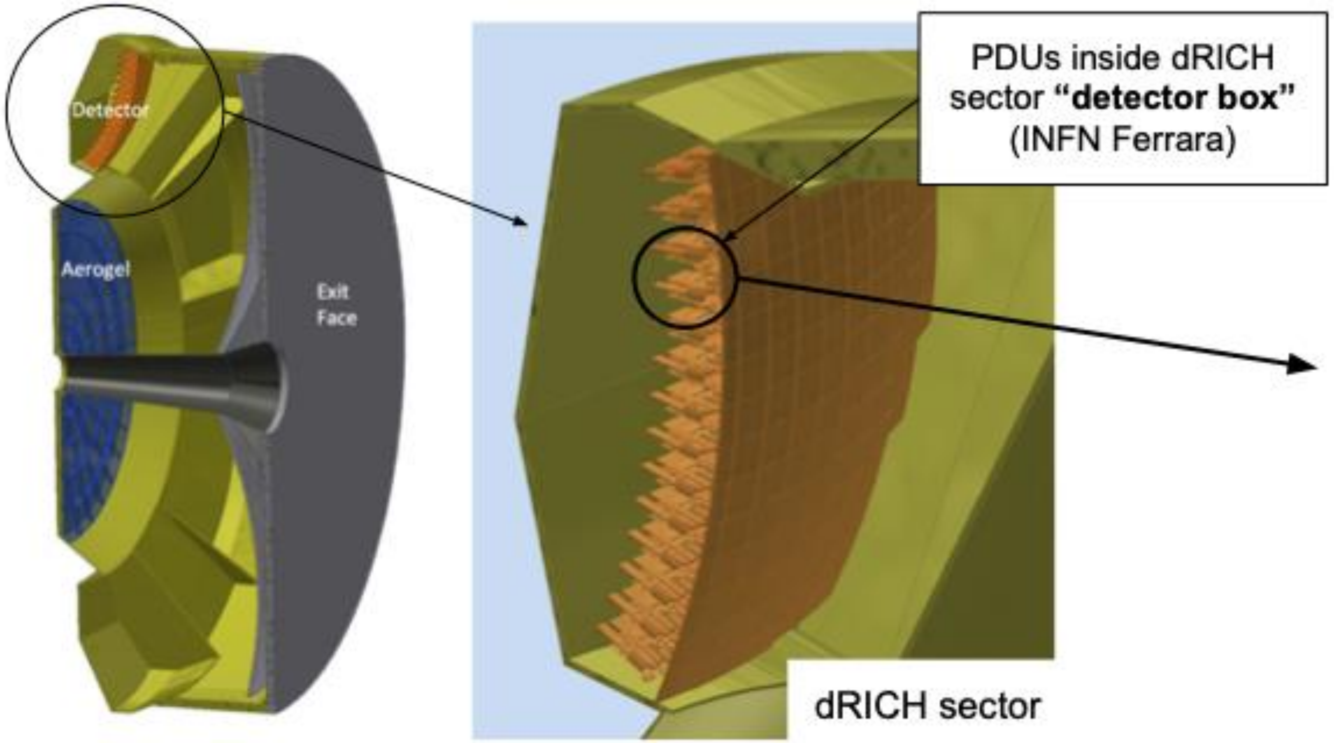
A path toward a full data-push architecture

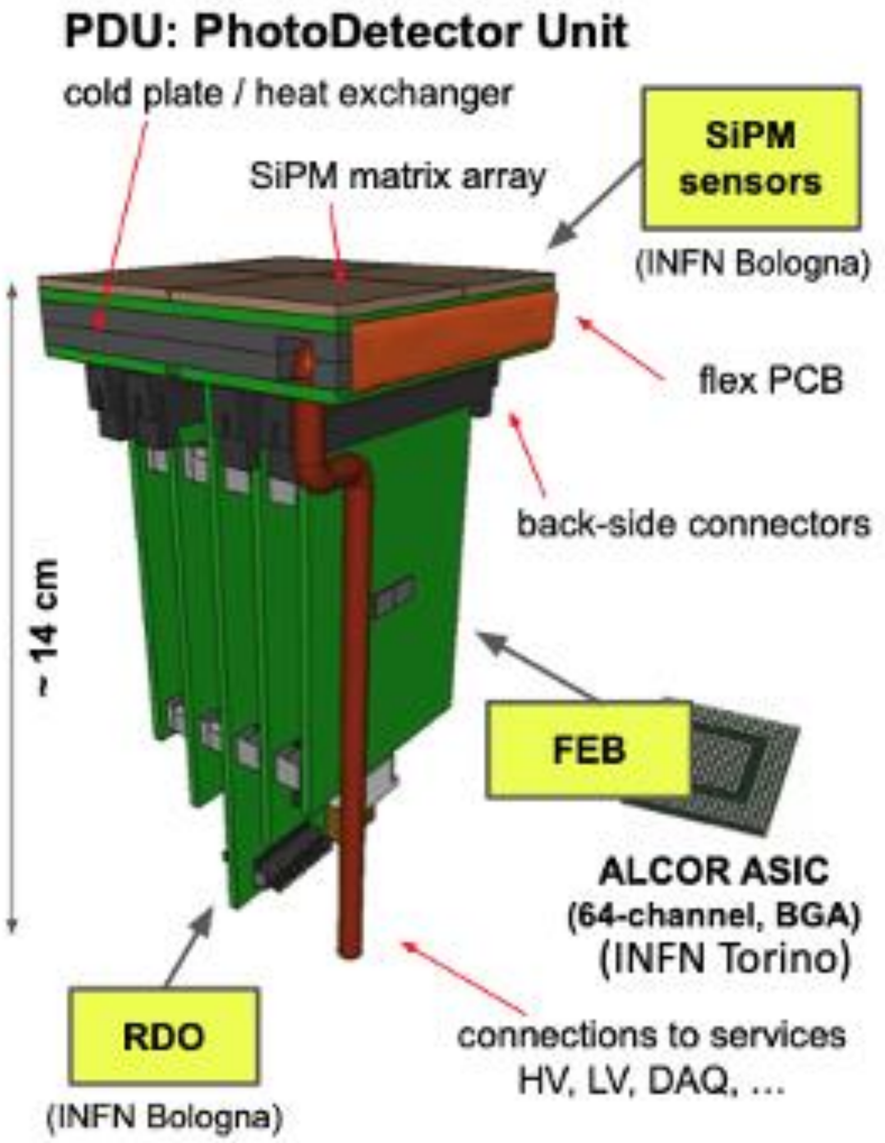


EIC physics and generalities
ePIC experiment
Why the dRICH
SiPM radiation damage
RDO design/hardware
ALCOR ASIC details
dRICH interaction tagger
Electronics radiation tests

(many links to topics "out")

dRICH recap in three slides (I): electronics



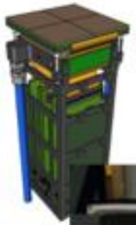


[dRICH status & intro]: M. Contalbrigo @RICH2025
[Photosensors (SiPM)]: N. Rubini et al., NIM A 1082 (2026) 170890 (Wien 2025)
[ALCOR (FEE ASIC)]: F. Cossio @PD2025
[PID performance]: T. Boasso @RICH2025
[dRICH Interaction tagger]: S. Vallarino @EICUG-ePIC 2025
[RDO]: P. Antonioli @EICUG-ePIC 2025
[RDO rad. tests]: S. Geminiani @TWEPP2025
[ML for data reduction in DAMs]: C. Rossi @RICH2025

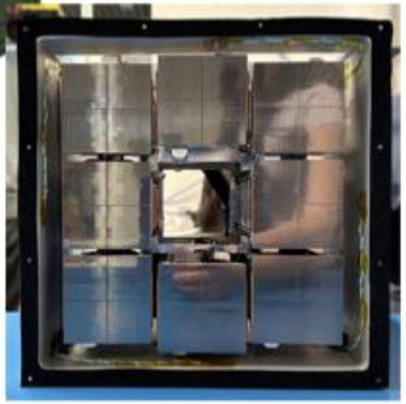
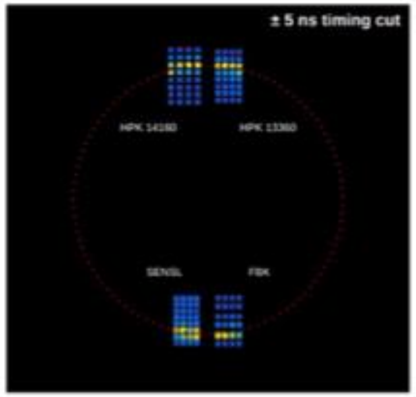
dRICH recap in three slides (II): test beams

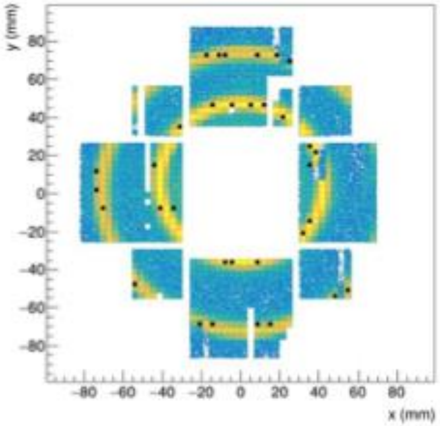
from the first prototype — towards detector construction

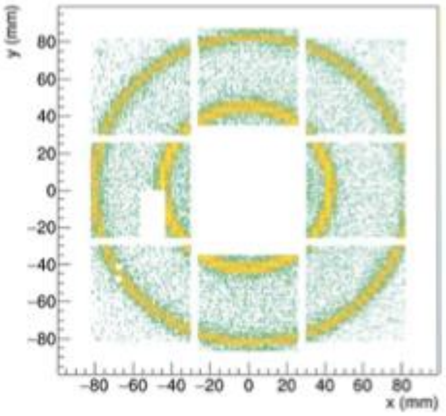
2022	2023	2024	2025
electronics v1	electronics v2	electronics v2.1	electronics v3

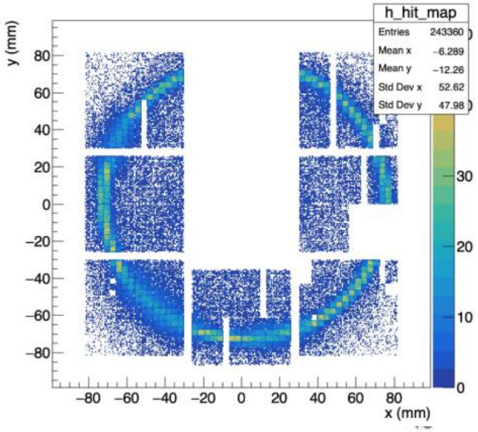






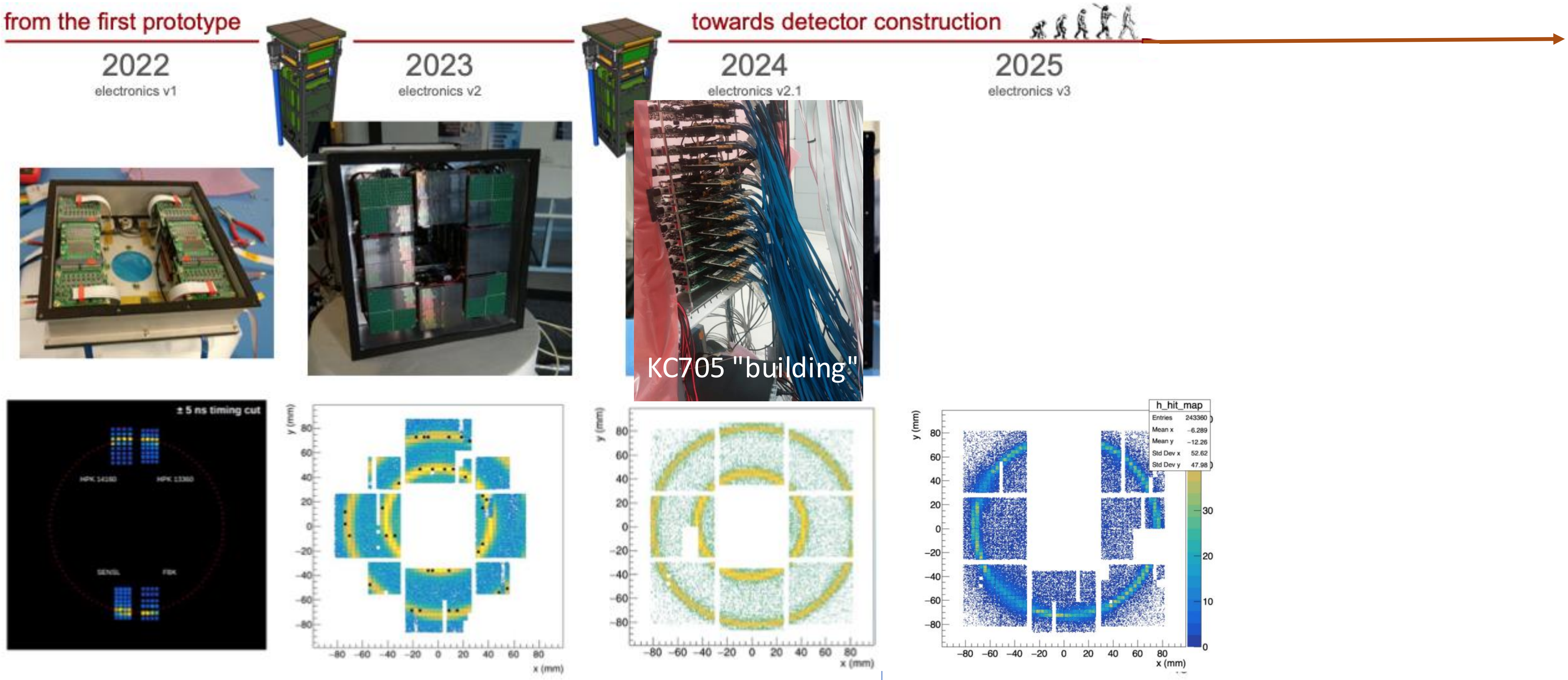




KC-705 readout + IPbus

RDO readout + IPbus

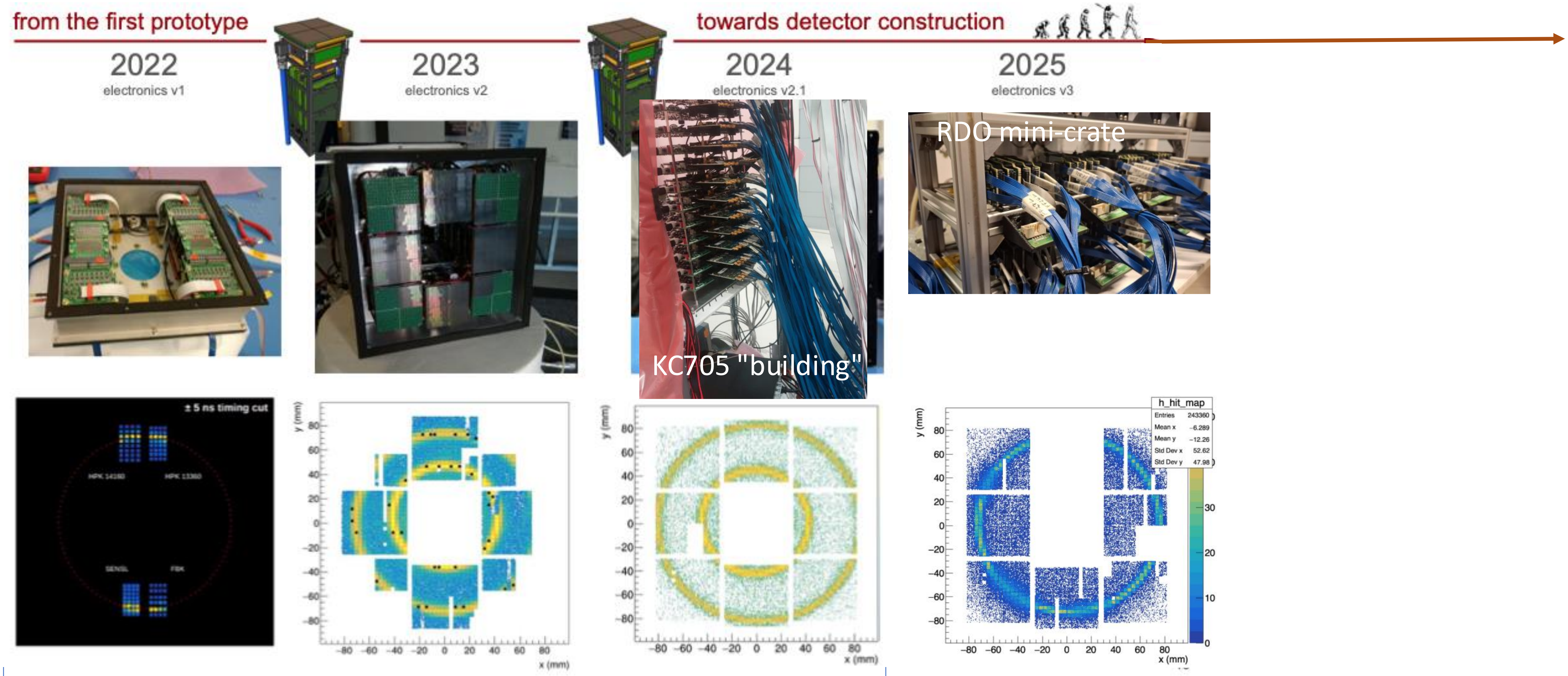
dRICH recap in three slides (II): test beams



KC-705 readout + IPbus

RDO readout + IPbus

dRICH recap in three slides (II): test beams



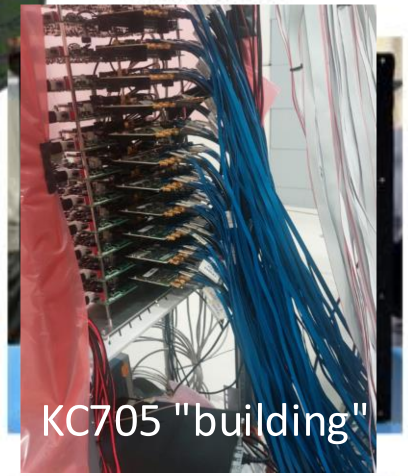
KC-705 readout + IPbus

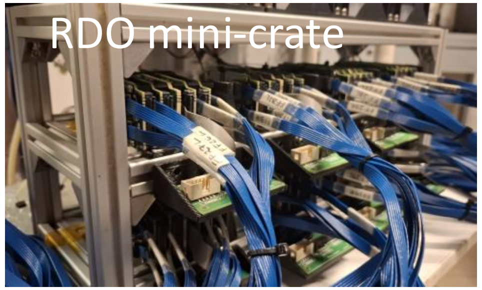
RDO readout + IPbus

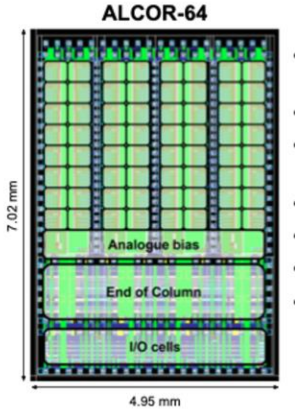
dRICH recap in three slides (II): test beams

from the first prototype — towards detector construction

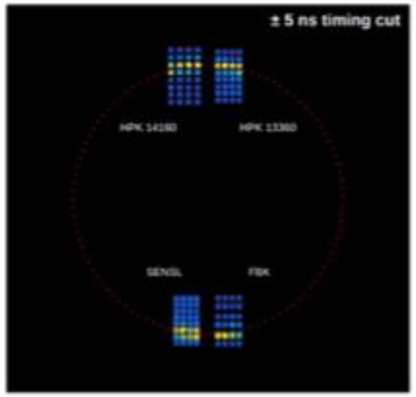
2022	2023	2024	2025	2026
electronics v1	electronics v2	electronics v2.1	electronics v3	electronics v3 + ALCOR64 + FELIX

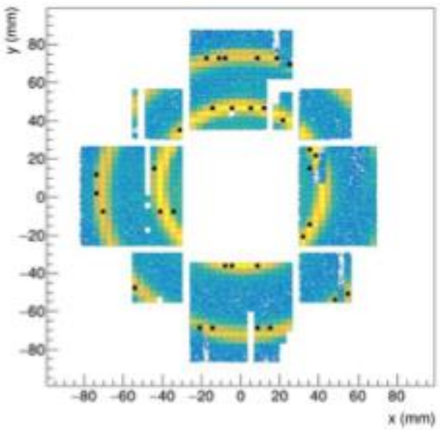


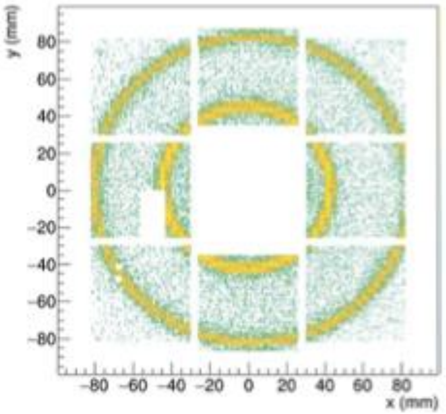


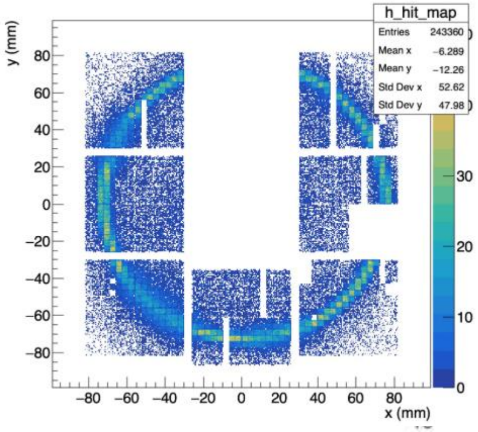


FLX-155









KC-705 readout + IPbus

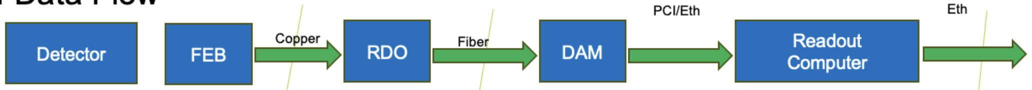
RDO readout + IPbus

RDO + "EIC link" + DAM

Summary of Channel Counts and Data Flow in ePIC

Detector Group	Channels					Det Fiber Down	Det Fiber Up	RDO	Fiber Pair (DAQ)	DAM	Data Volume (RDO) (Gb/s)	Data Volume (To Tape) (Gb/s)
	MAPS	AC-LGAD	SiPM/PMT	MPGD	HRPPD/ MCP-PMT							
Tracking (MAPS)	16B					187	4976	323	323	7	15	15
Tracking (MPGD)				164k		640	2560	160	160	5	27	5
Calorimeters	500M		100k					522	522	17	70	17
PID (TOF)		6.1M				500	1364		1364	30	50	12
PID Cherenkov			318k		143k	1334	1334	1242	1334	33	1275	32
Far Forward		1.5M	10k					80	80	6	36	12
Far Backward	66M		3.4k					25	289	11	37	8
Lumi		128k	5.1k					41	41	4	264	8
Polarimetry	Independent Electronics, DAQ, & Controls from central detector but expected to build on same technologies											
TOTAL	**16.6B**	**7.7M**	**432k**	**164k**	**143k**	**2,661**	**10,234**	**2,393**	**4,113**	**113**	**1,774**	**109**

Summary of Data Flow



Aggregate	2.0 Tb/sec
Noise	1.6 Tb /sec
Signal from Physics + Background	400 Gb / sec

Aggregate	2.0 Tb/sec
Per RDO (Avg)	0.7 Gb/sec

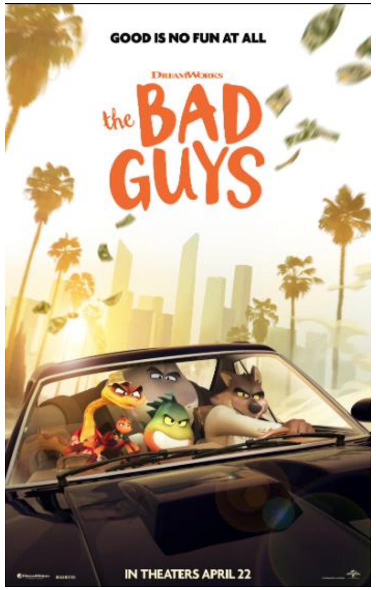
Aggregate	115 Gb/sec
Collision Signal	62 Gb/sec
Synchrotron Rad	6 Gb/sec*
Electron Beam	4.5 Gb/sec
Hadron Beam	1.0 Gb/sec
Noise	41 Gb/sec

Scale of the system:

- **Electronics**
  ~ 25 detector subsystems
  ~ 5 Readout Technologies
  ~ 2500 RDOs (on detector/in racks)
  ~ 110 DAM boards (DAQ room)
  GTU (with interface boards)
- **Maximum Data Volume**
  ~ 2 Tb/sec digitized
  ~ 115 Gb/sec recorded
- **Online Computing (Echelon 0)**
  ~200 nodes (DAQ Room/SDCC)

* Synchrotron radiation caveats:
1. Rates are based upon hit rate for all ePIC detectors. In fact, data volumes depend upon specific detector hit (64 bits/hit assumed)
2. Highest Synchrotron radiation / electron beam gas will correspond to lower values for collision signal
3. Plan to analyze by component soon

dRICH is one of the **bad guys** within a continuous readout approach for ePIC



Slide courtesy: D. Abbott and J. Landgraf

Note
at EIC zero-day (and during all commissioning) throughput will be 10^2 lower

how to approach dRICH throughput?

0 cool down the sensors → -40 C
heal the damage → annealing
optimize overvoltage and choice of the sensors

sensors
INFN-BO/INFN-FE/…

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1 electronics gated: ALCOR shutter

electronics, clock distribution, RDO
INFN-TO/INFN-BO

---

2 understand if the event is noise or signal → **deploy ML techniques on DAM**

DAM
INFN-RM

---

3 understand if the event is noise or signal with a **dRICH interaction tagger** → give a trigger to DAM

INFN-GE

---

4 get an external trigger from another sub-detector (Forw. HCAL?) → give a trigger to DAM

ePIC

ALCOR dRICH ASIC: born for streaming readout

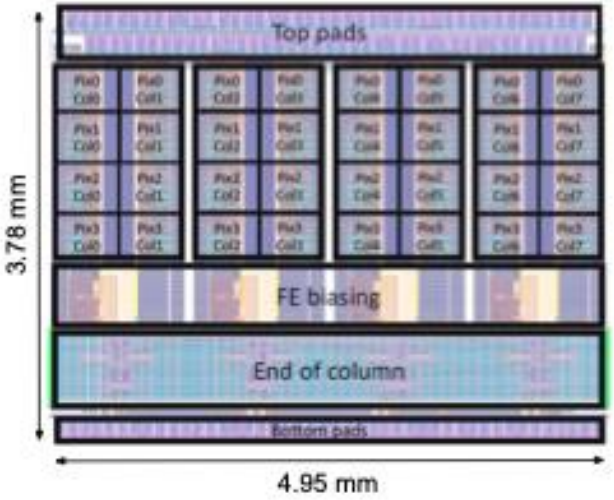
A Low Power **C**hip for **O**ptical **S**ensor **R**eadout

ALCOR (FEE ASIC): F. Cossio @PD2025

Data-push architecture: data are "immediately" out on LVDS Tx links

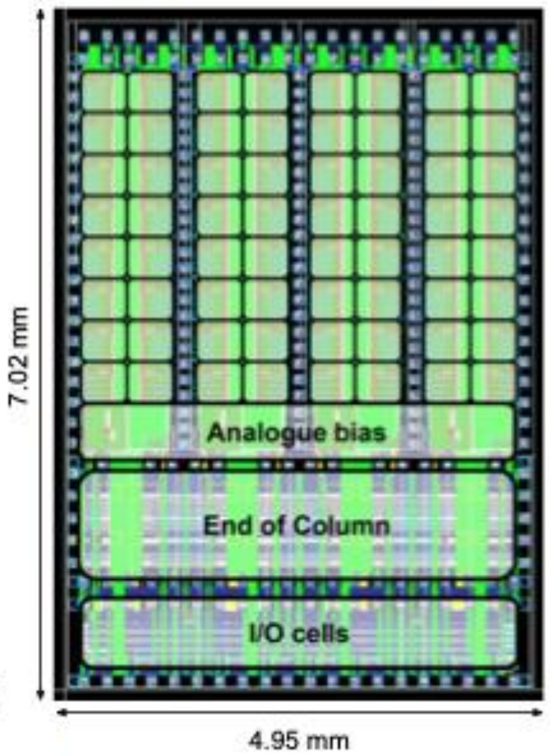
- **32** or **64-pixel matrix** mixed-signal ASIC with on-chip signal amplification, conditioning and digitization
- **ToA + ToT** or **Slew-Rate** measurements for **time walk compensation**
- **Triggerless readout**, fully digital output
- Power consumption **~12 mW/channel**
- **110 nm** CMOS technology

ALCOR-32



- ALCORv1: Developed for the DarkSide Experiment for SiPM readout at cryogenic temperature
- **32-channel**, **wire-bond**
- **320 MHz clock** frequency
- 4 LVDS 320 MHz DDR Tx links
- Extensively used within the ePIC-dRICH Collaboration **since 2021** and validated with multiple **successful beam tests** (ALCORv2)

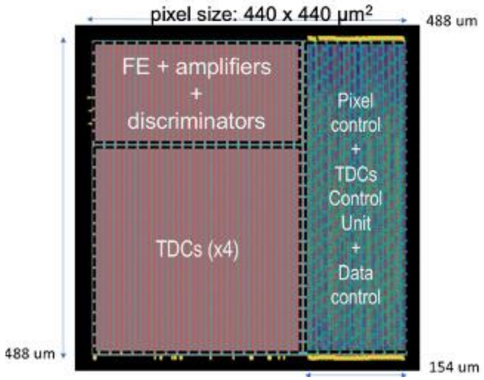
ALCOR-64



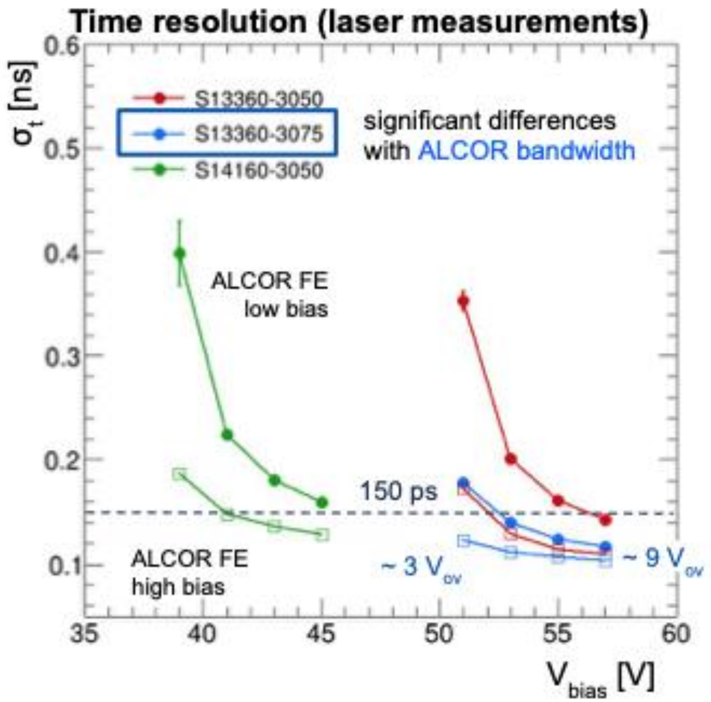
- New version (ALCORv3) with specific EIC-driven features
- **64-channel, FC-BGA** package
- Increased amplifier bandwidth to improve time resolution
- Hardware **shutter**
- **394 MHz clock** frequency
- 8 LVDS 394 MHz DDR Tx links
- **MPW tapeout** on **Apr 2025**, 60 singulated dies received on Aug 26th, packaging ongoing

7

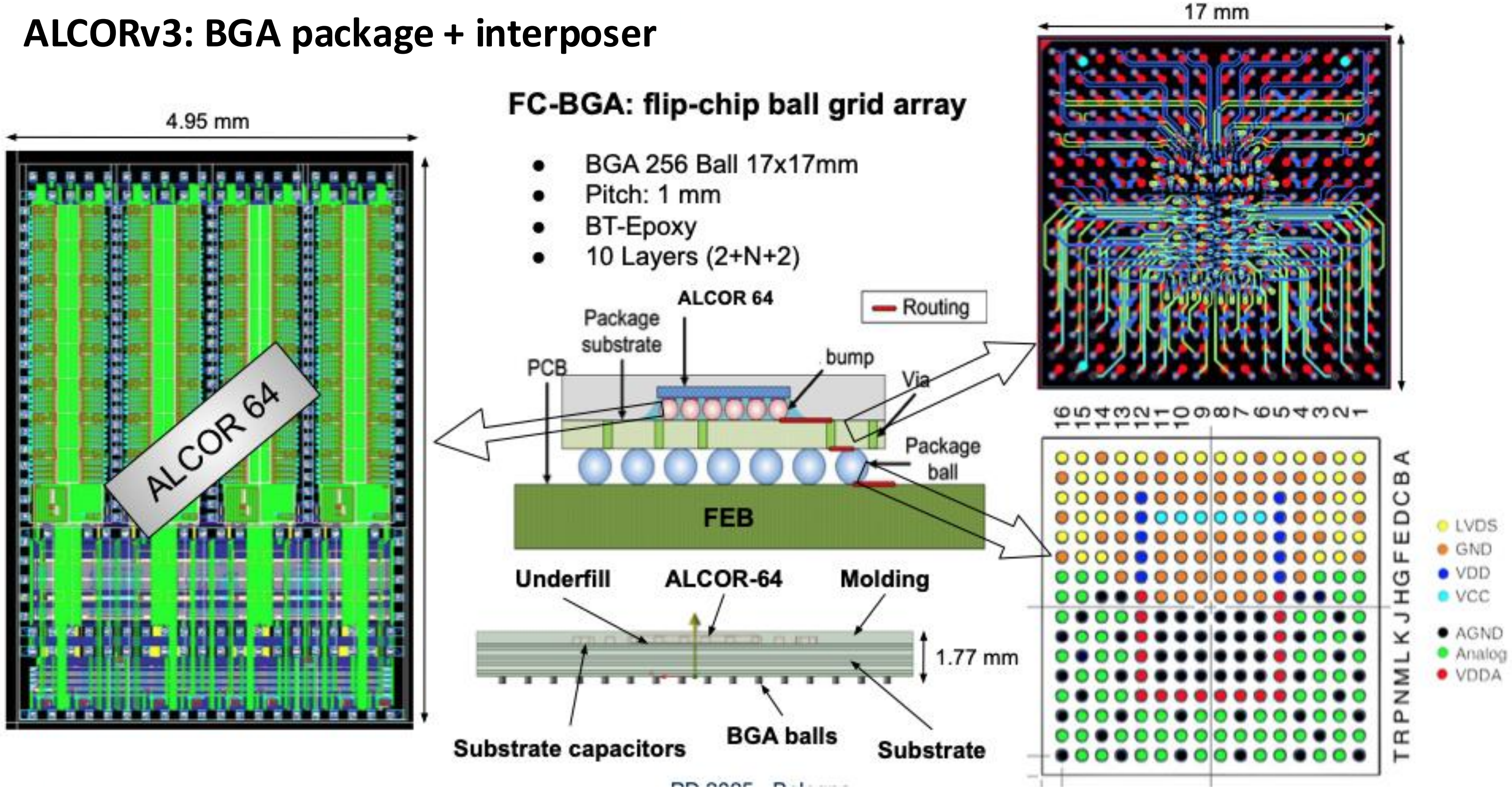
ALCOR: latest developments



- ALCOR pixel provides single-photon time tagging
- ALCOR pixel copes with maximum DCR rate (300 kHz/SiPM at maximum radiation damage)
- ALCORv3 → 64 channel → 8 LVDS Tx links
- A **shutter** can inhibit time digitization to suppress out-of-time SiPM DCR hits
- First samples soon (2026/Q1) in our hands

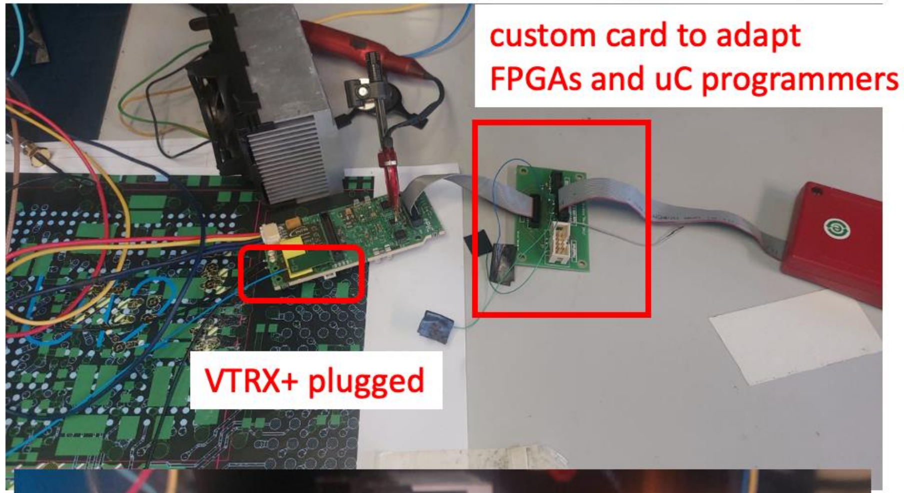


ALCORv3: BGA package + interposer

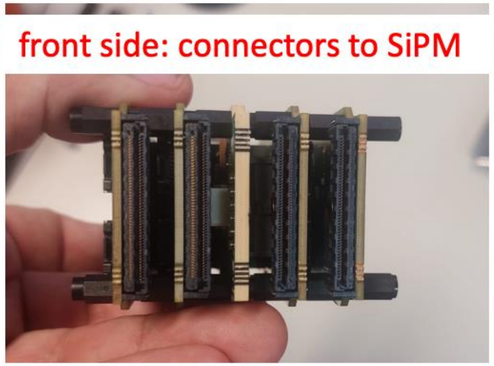


dRICH RDO: no longer drawings, just pics

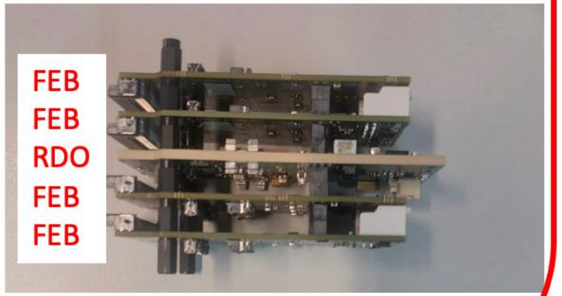
RDO: P.A. @EICUG-ePIC 2025

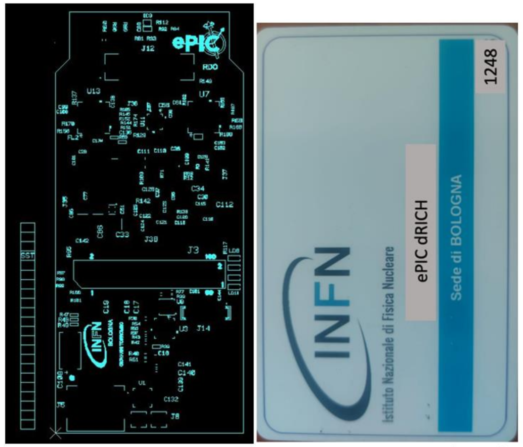


RDO+4 FEB dRICH



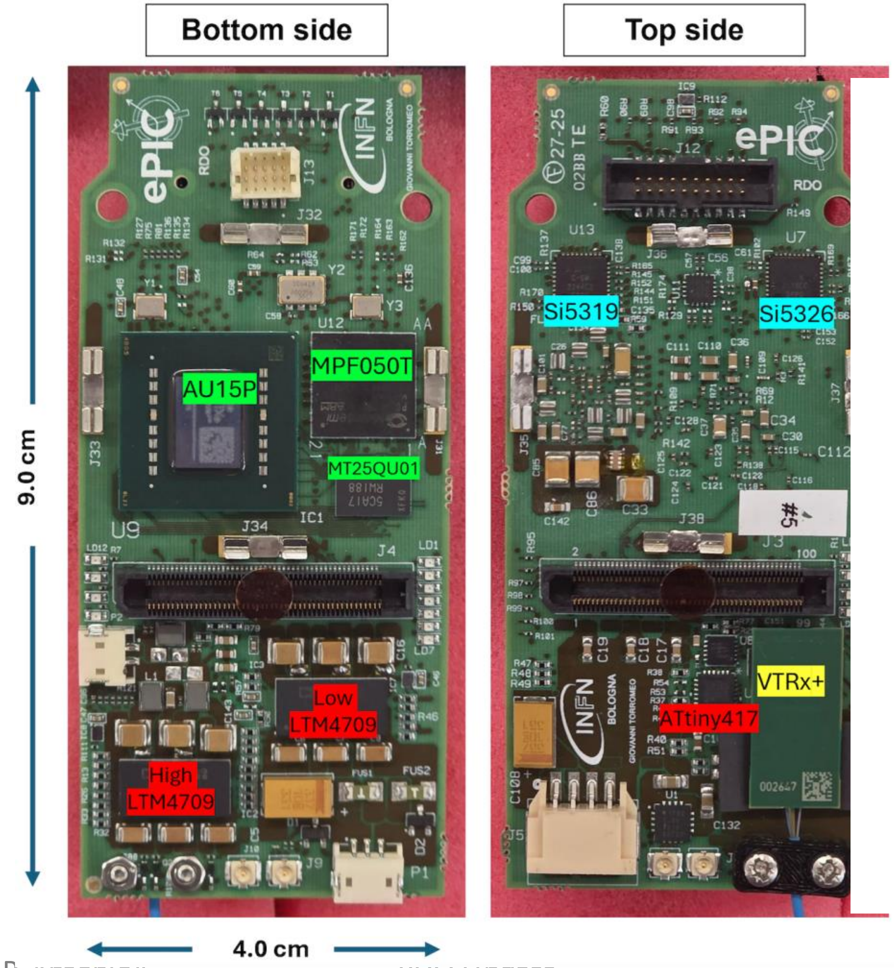
The dRICH electronic burger



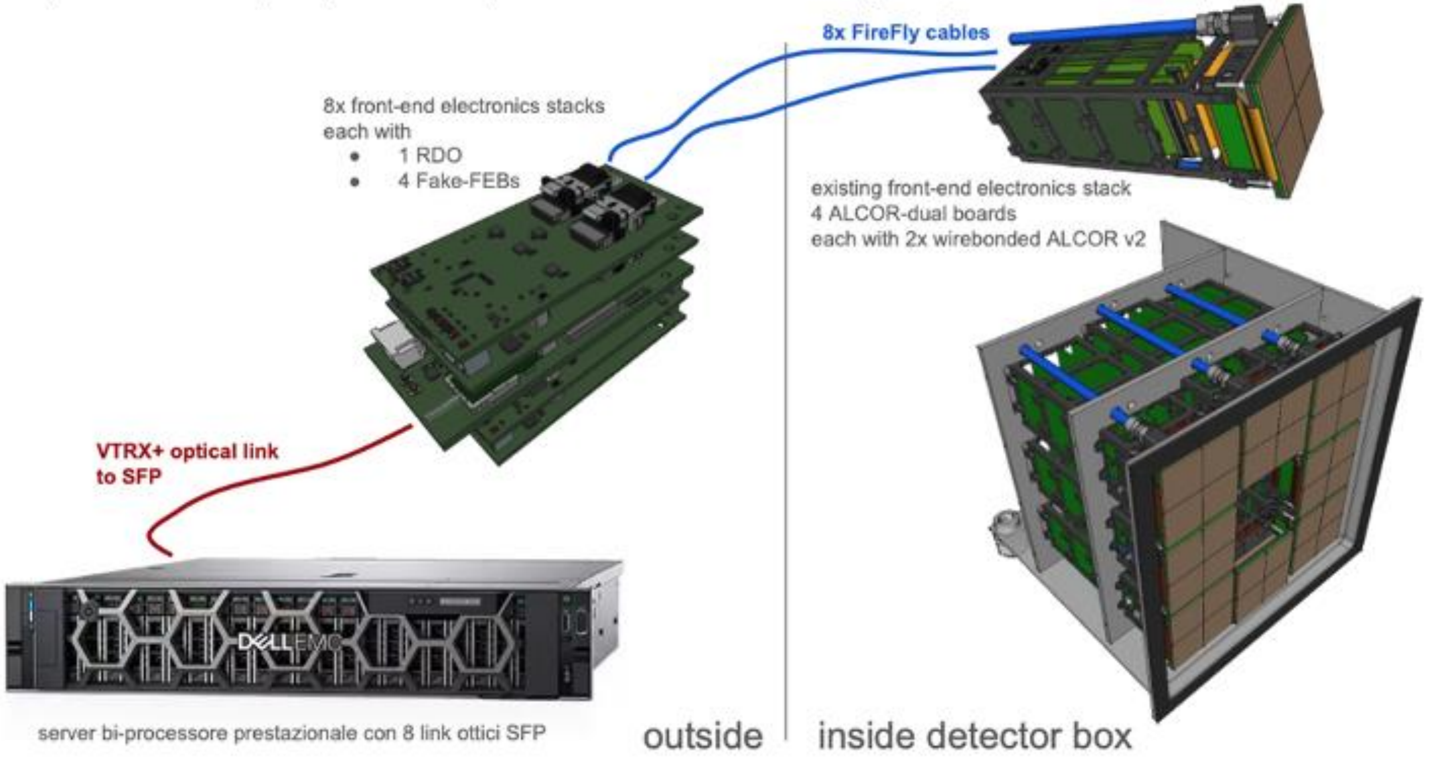


RDO latest developments

- RDO finally delivered to in Summer 2025
- Validated and used to test beam in November 2025
- "EIC-ready" but not yet validated with a full data-push data flow (i.e. streaming readout scheme down to DAM)
- IPbus adaptation as a DAQ bus so far

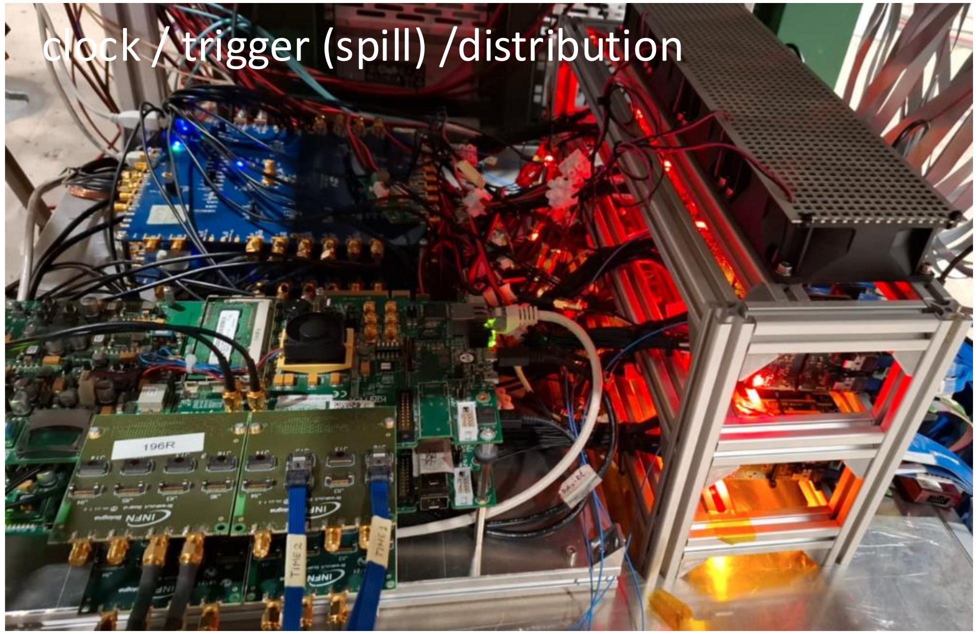


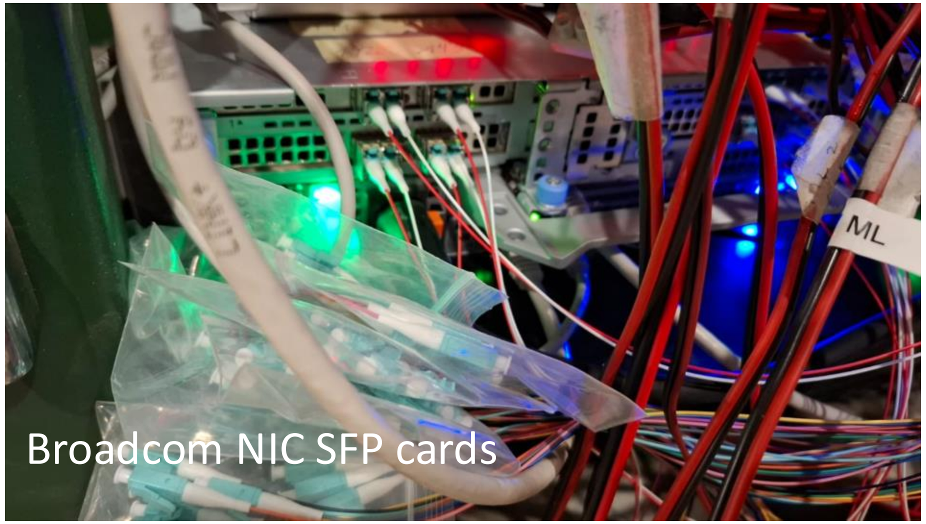
- we use IPBUS protocol over VTRX+ with SFP NIC cards on receiving end
- "fake-FEB" (ALCOR v2.1 adaptor) : two FireFly connectors to reach existing FEB (with 2 ALCOR v2.1)



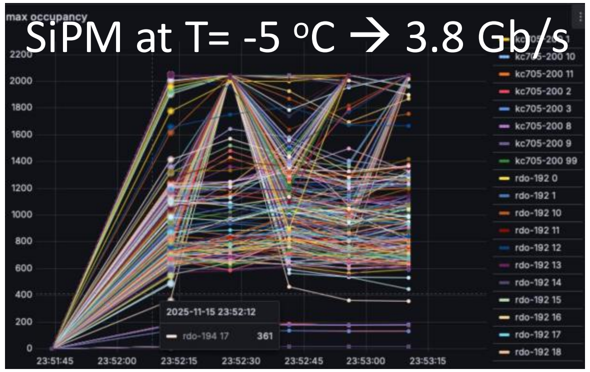
RDO latest developments: test beam setup

dRICH protoype in Bo-Lab
with RDO "crate"





streaming DAQ: data-push to RDO FIFO then IPbus



T=-35 ºC → T=-5 ºC
DCR increases
mimic radiation damage

full setup @ SPS

(for general dRICH test beam results see M. Giacalone @TB2024)

dRICH throughput modelling (I)

dRICH DAQ parameters	
RDO boards	1248
ALCOR64 x RDO	4
dRICH channels (total)	319488
Number of DAM	30
Input link in DAM	42
Output links from DAM to TP	1
Number of DAM Trigger Processor	1
Input link to DAM Trigger Processor	30
RDO-DAM Link Bandwidth (VTRX+) [Gb/s]	10
DAM to Echelon-0 Switch Bandwidth [Gb/s]	100
dRICH Interaction tagger reduction factor	1
Interaction tagger latency [s]	1,00E-04
EIC parameters	
EIC Clock [MHz]	98,522
Orbit efficiency (takes into account gap)	0,92

ALCOR parameters		Notes
Front end limit [kHz]	4000	
ALCOR Clock [MHz]	394,08	It will be 394.08 MHz or 295.55 MHz
Channels/serializer	8	
Bits per hit	64	2 32-bit words per hit (also TOT)
Bits per hit encoding 8/10	80	
Serializer band limit [Mb/s]	788,16	
Theoretical Serializer limit/ channel [kHz]	1231,5	this would be with 0 control words
Serializer limit single ch [kHz]	800	this is expected to improve with ALCOR v3
Number of serializer per chip	8	
Channel/chip	64	
Shutter width (ns)	2	(if you put 10 ns == no shutter)

Reduction factor via shutter
RF = 10 ns/(shutter width)

There are two reduction handles in this table:
- the shutter
- something external (can be NN on DAMs, dIT or ..?)

dRICH backend DAQ reorganized following studies from INFN Rome (see next slides) from 27+1 to 30+1 FLX-155: 30 DAMs + 1 Trigger Processor (TP)

Reduction factor provided by whatever external trigger (including NN on dRICH DAMs)

dRICH throughput modelling (II)

DAM to Echelon-0 Switch Bandwidth [Gb/s]	100				
dRICH Interaction tagger reduction factor	1		Channel/chip	64	
Interaction tagger latency [s]	1,00E-04		**Shutter width (ns)**	2	(if you put 10 ns == no shutter)
EIC parameters					
EIC Clock [MHz]	98,522				
Orbit efficiency (takes into account gap)	0,92				

dRICH data stream analysis		**Limit**	**Comments**
Sensor rate per channel [kHz]	300,00	4.000,00	
Rate post-shutter [kHz]	55,20	800,00	
Throughput to serializer [Mb/s]	34,50	788,16	
Throughput from ALCOR64 [Mb/s]	276,00		limit FPGA dependent: - check with RDO
Throughput from RDO [Gb/s]	1,08	10,00	based on VTRX+
Input at each DAM [Gbps]	45,28	420,00	
Buffering capacity at DAM [Mb]	4,64		to be checked but seems manageable
Output from each DAM [Gbps]	45,28	100,00	

Aggregated dRICH data throughput		**Comments**
Total input at DAM [Gb/s]	1.358,44	This is only "inside" DAM, not to be transferred on PCI
Total output from DAM [Gb/s] to Echelon	1.358,44	Reduction from interaction tagger (FPGA or det. based)

This is worst case!

*Take home message

Using only the shutter with a reduction factor 5 (2 ns over 10 ns BC) we keep 1.3 Tbps throughput and we stay within all limits (including transfer from DAM to Echelon-0)

dRICH throughput modelling (III)

DAM to Echelon-0 Switch Bandwidth [Gb/s]	100				
dRICH Interaction tagger reduction factor	5		Channel/chip	64	
Interaction tagger latency [s]	1,00E-04		**Shutter width (ns)**	10	(if you put 10 ns == no shutter)
EIC parameters					
EIC Clock [MHz]	98,522				
Orbit efficiency (takes into account gap)	0,92				

dRICH data stream analysis		**Limit**	**Comments**
Sensor rate per channel [kHz]	300,00	4.000,00	
Rate post-shutter [kHz]	276,00	800,00	
Throughput to serializer [Mb/s]	172,50	788,16	
Throughput from ALCOR64 [Mb/s]	1.380,00		limit FPGA dependent: - check with RDO
Throughput from RDO [Gb/s]	5,39	10,00	based on VTRX+
Input at each DAM [Gbps]	226,41	420,00	
Buffering capacity at DAM [Mb]	23,18		to be checked but seems manageable
Output from each DAM [Gbps]	45,28	100,00	

Aggregated dRICH data throughput		**Comments**
Total input at DAM [Gb/s]	6.792,19	This is only "inside" DAM, not to be transferred on PCI
Total output from DAM [Gb/s] to Echelon	1.358,44	Reduction from interaction tagger (FPGA or det. based)

10 ns means no shutter

data reduction via "another method"

further risk mitigation here might be applied using two TX links instead of one

If shutter is not effective we need a reduction factor 5 from a dRICH interaction tagger method and we stay within all limits (including transfer from DAM to Echelon-0)

Will the shutter be effective?

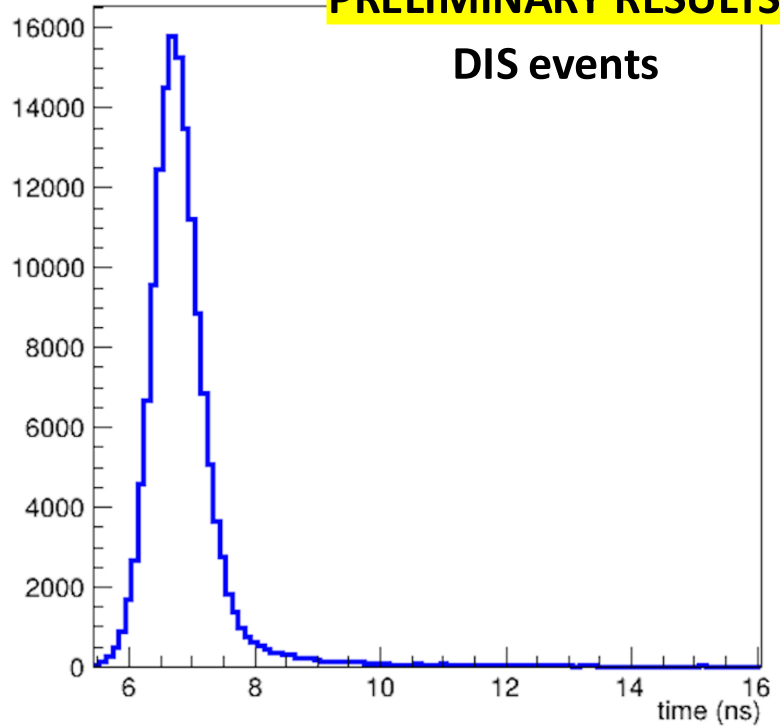
Simulations of hit time distribution at dRICH entrance window (before aerogel) within the context of dRICH Interaction tagger studies

- Hit time distribution (primaries) has Gaussian shape + a tail
- Bulk of primary hits lies **within 2 ns** ($\sigma_{pr} \cong$ 260 ps**)**
- added in quadrature time zero jitter (σ_{t0}= 250 ps) + front-end resolution (σ_{FE}= 150 ps)

$$\sigma = \sqrt{\sigma_{pr}^2 + \sigma_{t0}^2 + \sigma_{FE}^2} \approx 400 \text{ ps}$$

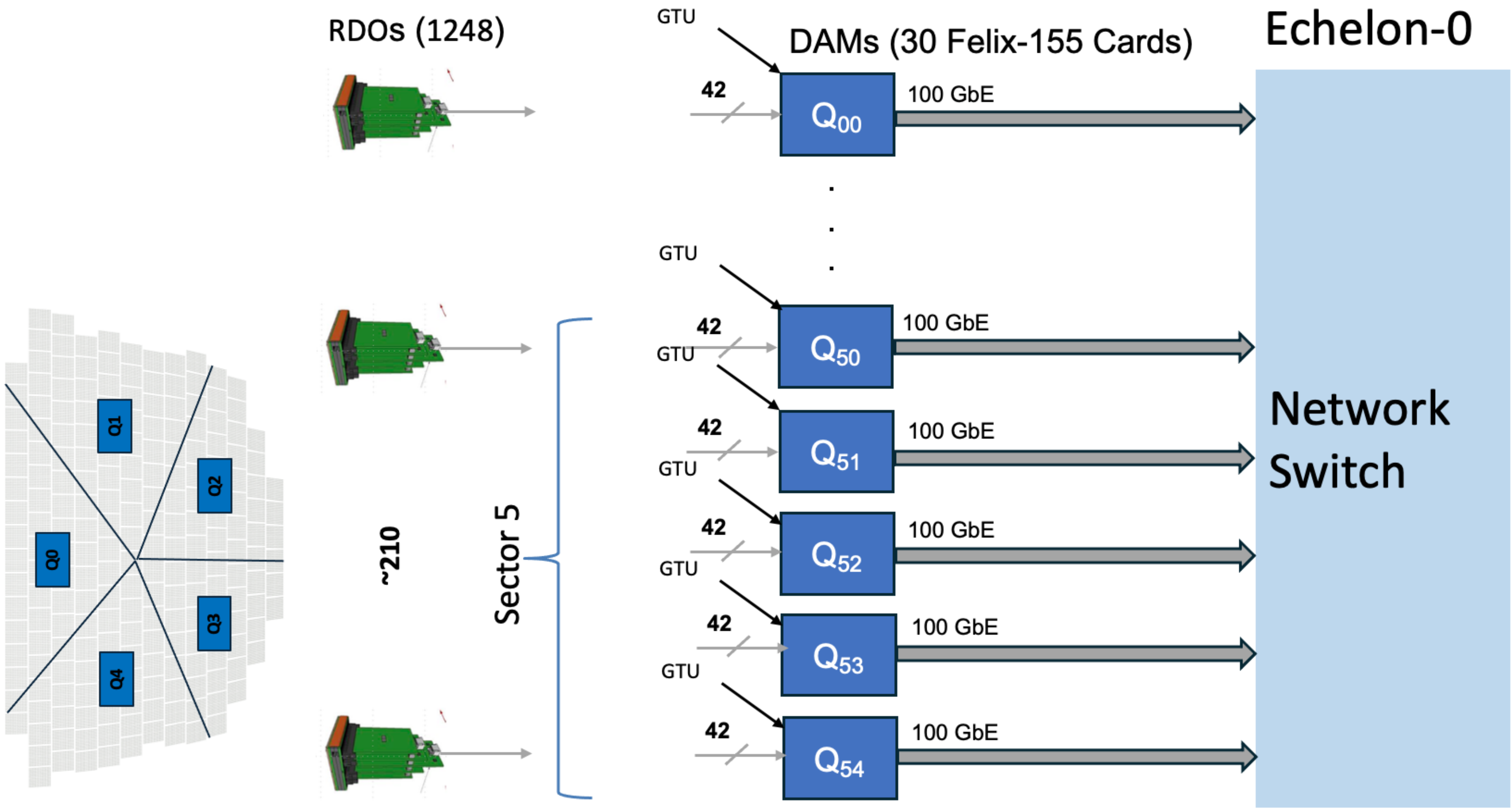
- from cumulative distribution 99% of particles included with a shutter window of 5 ns (from 5.5 ns to 10.5 ns → **50% DCR data reduction**)

PRELIMINARY RESULTS



Full simulation in progress:
→ we don't expect a large spread added by photon emission + propagation (confirmed already by simulation)
→ impact of time slewing effect to be assessed (could impact with the need of 2 ns additional window – see backup)

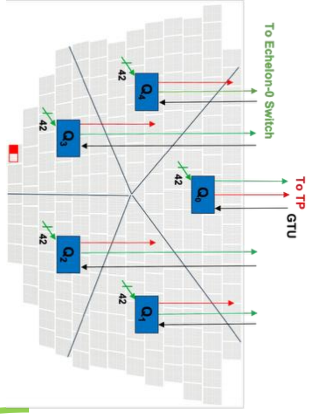
dRICH DAQ: the backend

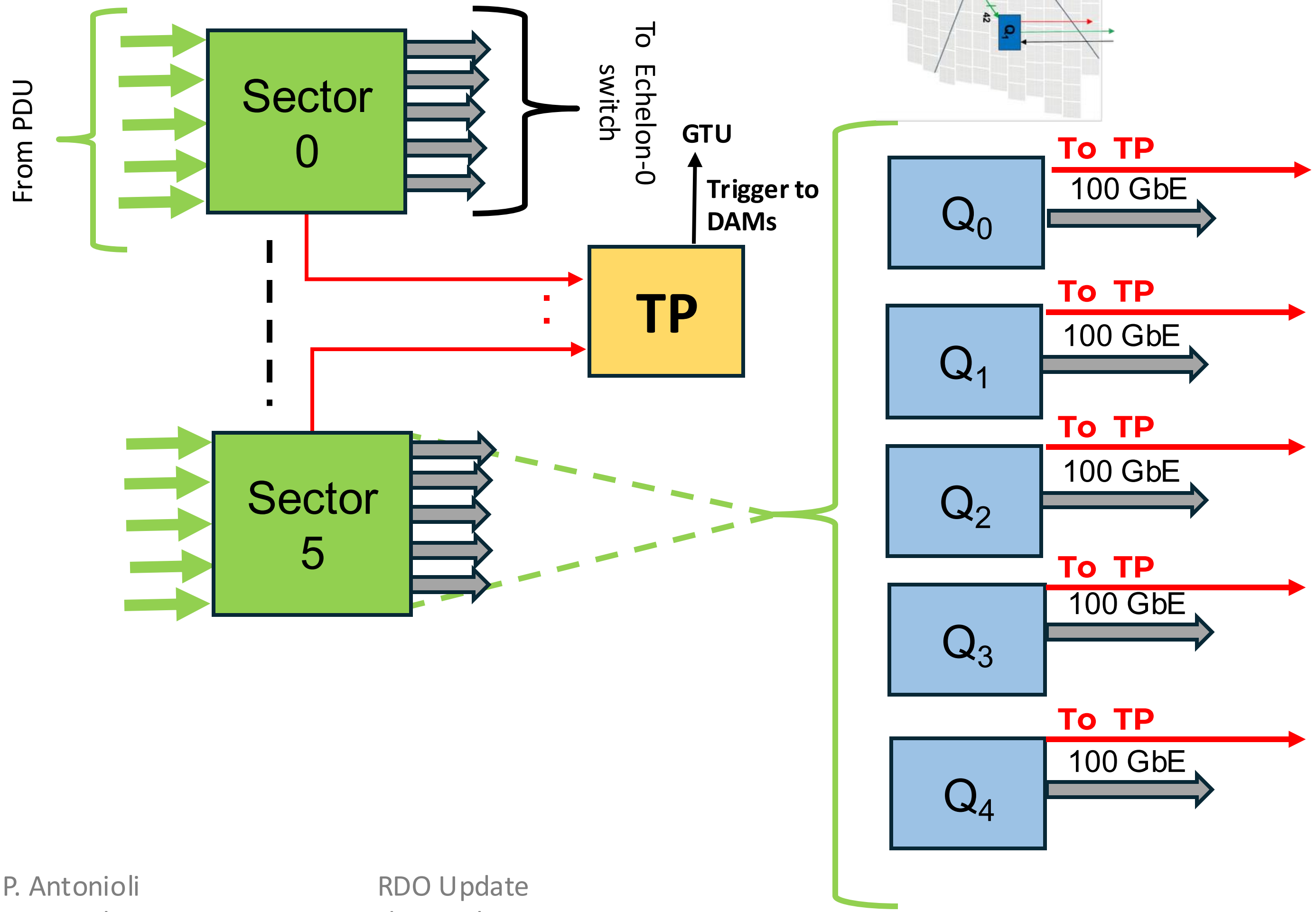


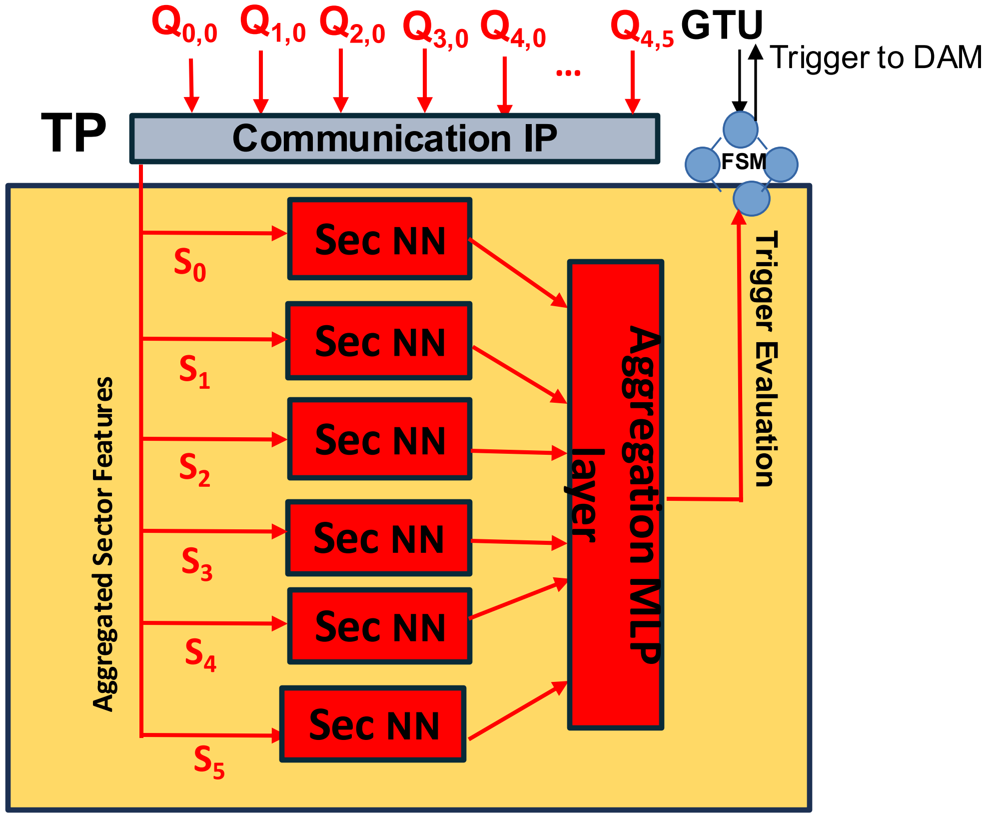
[ML for data reduction in DAMs](): C. Rossi @RICH2025

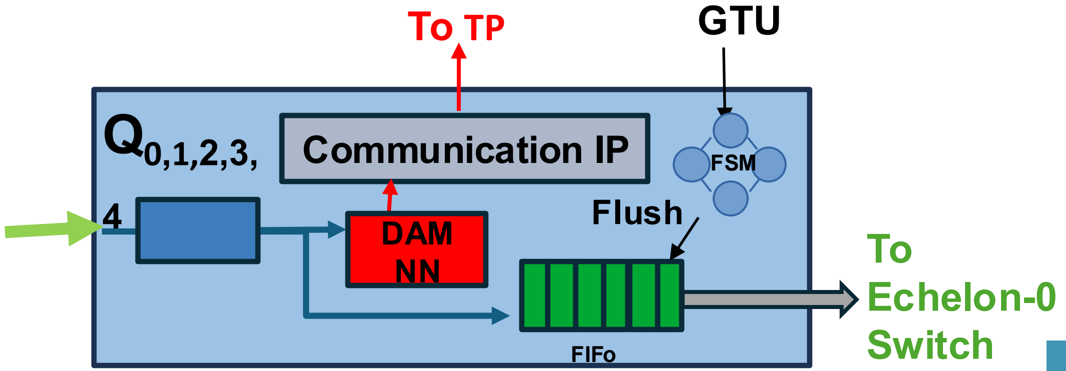
dRICH data reduction integrated in the DAQ Backend (I)

Neural network distributed over 31 Felix-155







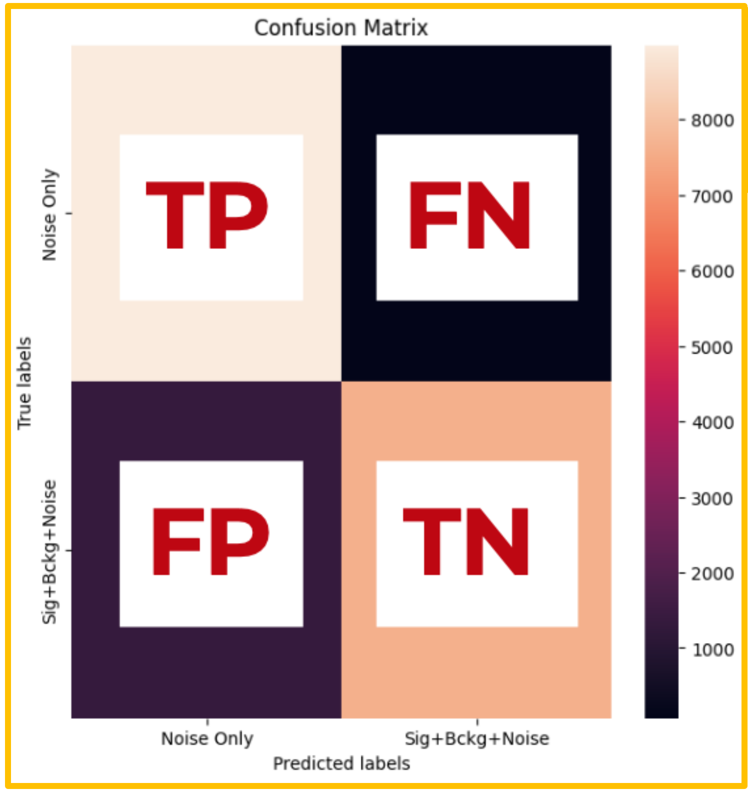


Data Reduction performance: 100 kHz DCR and time window = 10 ns

PRELIMINARY RESULTS

Test with 10000 signal+phys. background (P=Positive) + 10000 pure noise events (N=Negative)

KERAS MODEL



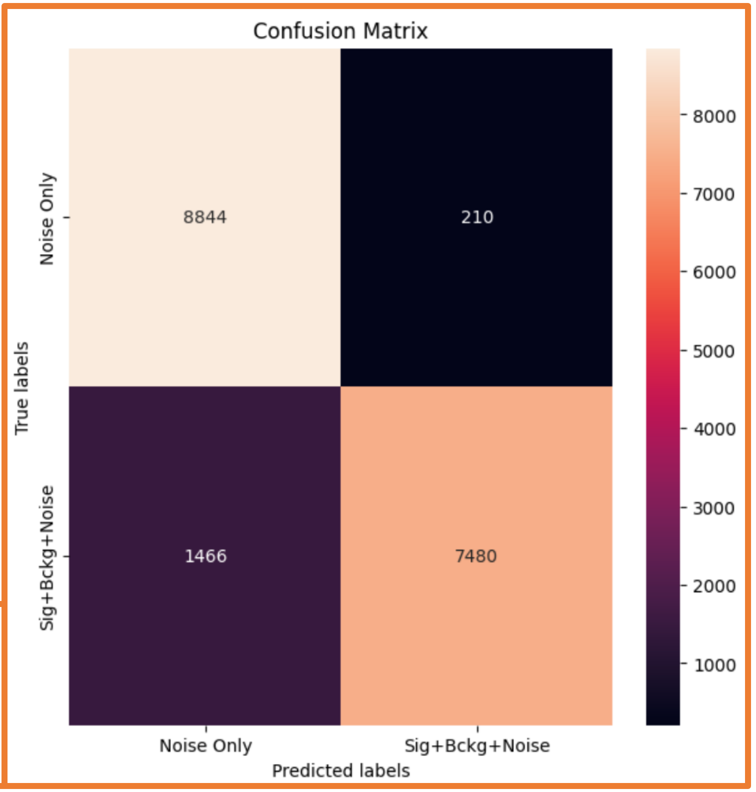
- Accuracy = (TP+TN)/(TP+TN+FP+FN) = 0.921
- Purity = TP/(TP+FP) = 0.870
- Efficiency = TP/(TP+FN) = 0.992

Preliminary result indicate DAM filter could comfortably provide ≫ 5 data reduction factor

Model Quantization

- Inputs, Activations: fixed point<16,6>
- Weights, Biases: fixed point<8,1>

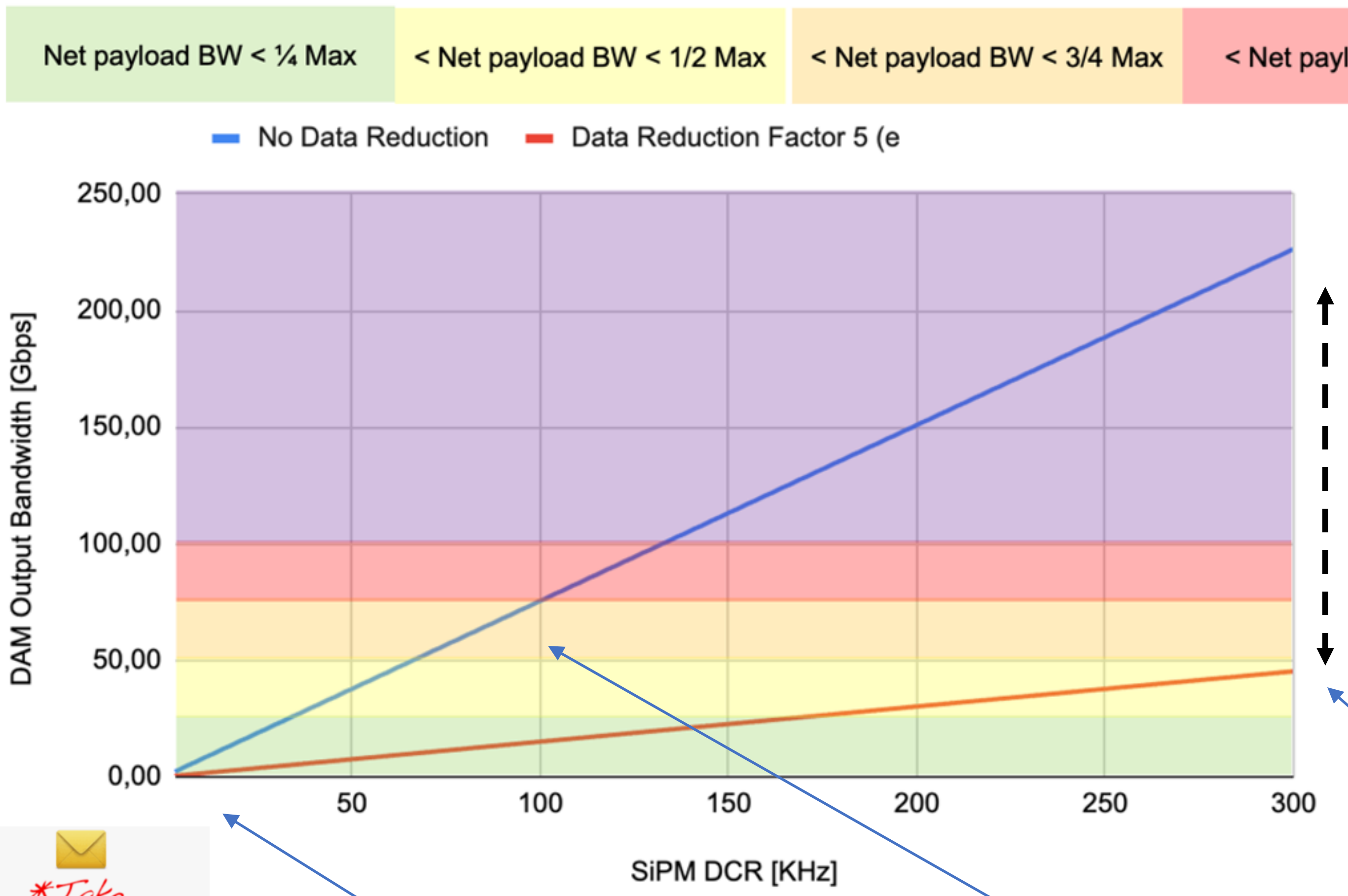
QUANTIZED MODEL

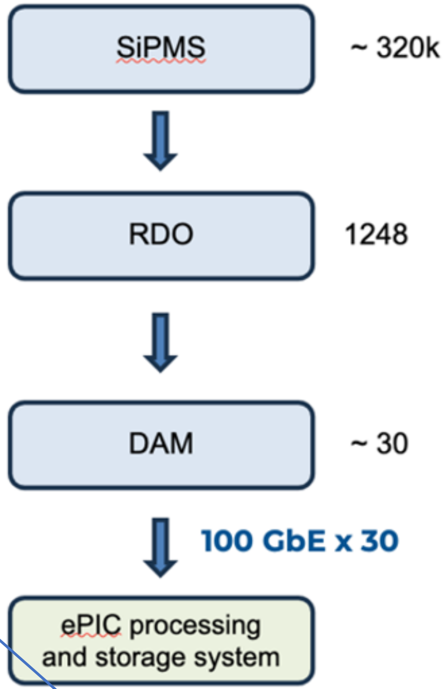


- Accuracy = (TP+TN)/(TP+TN+FP+FN) = 0.906
- Purity = TP/(TP+FP) = 0.858
- Efficiency = TP/(TP+FN) = 0.977

parameterization of DCR background included

Re-cap on dRICH output bandwidth





*Take home message

Data reduction factor (RF) five can be achieved via shutter or provided by NN or ext. trigger or a **combination** of them.

$$RF_{shutter} \times RF_{TP} = 5$$

Example:

- shutter window 5 ns → RF=2
- TP RF=2.5

*Take home message

Remember always at day zero dRICH starts with DCR = 3 kHz! Commissioning/first operations will allow tuning of shutter/TP etc.

without data reduction with a 100 kHz DCR we are close to DAM bandwidth limit

a data reduction factor 5 allows us to stay safe up to the 300 kHz limit

Towards full data-push architecture: time ordering

The problem: ALCOR timestamps are not *"immediately"* out

Pixel TDC conversion defines time required for digitization:

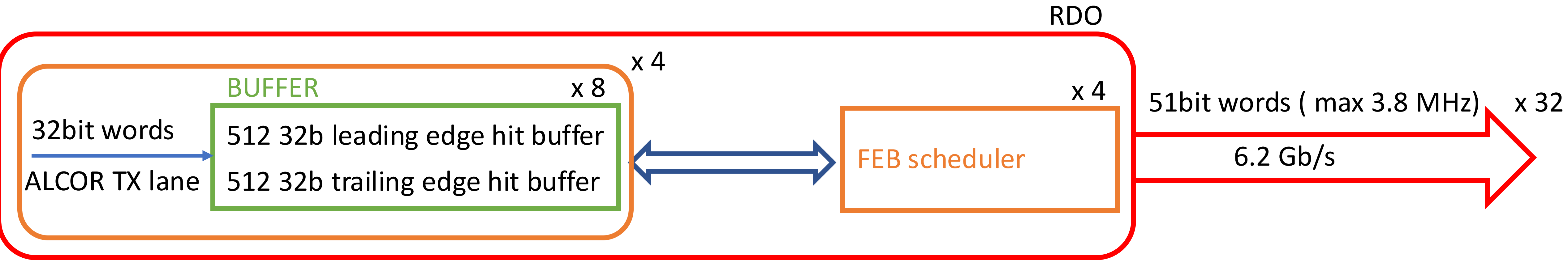
● TDC max conversion time = 1.5 x 128 = 192 clock cycles ≃ 500 ns
● TDC min conversion time = 0.5 x 128 = 64 clock cycles ≃ 170 ns
● Max ΔT = 500 ns - 170 ns = 330 ns (inside ALCOR channel) → down to the column and transmit off-chip

ALCOR data transmission:

● 1 word: 40 bits → 40 b / 788 Mb/s = 51 ns per event word (we have 8 channels for each Tx link)
● If no other hits in the column, 2 hits (separated by 128 clk cycles in the pixel) are only separated by idle words (K.28.5 "comma" are filtered by RDO) → [dependency on data rates
● Time reference given by ALCOR frame structure →
@DCR = 300 kHz/ch, Δt_{frame} = 12.7886 μs → $N_{events} = 8 \cdot DCR \cdot \Delta t_{frame}$ = 30.7
● 31 event words per frame (mean value, 2x in ToT mode, add physics)

→ can hits be sent time ordered (BC) by RDO to ease DAM work?

RDO "time ordering"?



BUFFER (1024 x 32 bit): → 1 Mbit full RDO:

- 512 leading words and 512 trailing words
- Leading/trailing edges waiting for matching
- 4.8 MHz : 300 kHz x 8 x 2 + ctrl words

Scheduler:

- Act on the occupancy and the timestamp to select the lane be read → push data to buffer
- Inspect BUF and build 51bit AWORDs(*)
- Completed 51b words are sent to the DAM via opt links ordered by BC

(*) AWORD = Alcor Word (see next slides)

we aim to send time ordered words (by BC) to the DAM

2026 Challenge: all this needs to be implemented (and validated!) in a "tiny" AU15P FPGA (5.1 Mbit BRAM)

ALCOR data (raw) and ePIC data (I)

ALCOR hits "event word" are timestamps

accelerator BC: bits 23 – 11

31 – 29	28 – 26	25 – 24	23 – 9	8 – 0
Col ID	Pix ID	TDC ID	Coarse Counter	Fine Counter

3 bits to identify the column (LVDS TX lane) [0 to 7]

3 bits to identify the pixel [0 to 7]

4 TAC TDC IDs: 2 bits
→ 2 TDCs for leading edge
→ 2 TDCs for trailing/slew rate

these nine bits are the measurement of the TAC you can reach 20-40 ps LSB at 394 MHz.
Calibration needed → can't be used at DAM level

394 MHz → coarse counter LSB 2.54 ns (currently 320 MHz → 3.125 ns)
15 bit coarse counter (0x7FFF = 32767)

Coarse counter expires every 83.228 μs > 12.78 μs (EIC orbit)
At each EIC orbit we get a RevTick signal from DAM (main EIC "synch")
→ this trigger a coarse counter reset and a frame structure injected in data flow

ALCOR data and ePIC data (II) + link protocol

DISCLAIMER NOTICE: all this is VERY PRELIMINARY

*Take home message

RDO "prepares" data reduction
DAM "does" data reduction

RDO

50	49 48	47 46	45 39	38 30	29 27	26 24	23 22	21 9	8 0
K CODE FLAG	FEB ID	TDC ID (trailing)	Coarse (trailing)	Fine (trailing)	Col. ID	Pixel ID	TDC ID (leading)	Coarse (leading)	Fine (leading)

- 51-bit AWORD: leading + trailing
- Bit optimization: EIC orbit / and max ToT

opt-link **protocol**

	DF3	DF2	DF1	DF0	DCS (free)	AWORD	AWORD	AWORD	AWORD
FULL	255	254	253	252	251 204	203 153	152 102	101 51	50 0
lpGBT	223	222	221	220	219 204	203 153	152 102	101 51	50 0

link protocol operated at **39.4 MHz** CLK (5/2 of EIC clock, close to LHC clock)

- Protocol over optical link: FULL (256 bits/CLK or lpGBT (224 bits/CLK with FEC5)
- if lpGBT, likely used without e-link: "hybrid" mode à la ALICE/GBT
- space for DCS bus (SWT à la ALICE-ITS2)

DAM

- extract BC from bits 21-11
- extract geographic position from RDOID (DAM is link-aware) + FEBID (49-48) + AlcorCh (29-24): geo info → data pattern
- NN decision is reached the DAM must add to the 51-bit word the 11 bits of the RDOID → 62-bit word
- 2 bits added → PCI 64-bit words → dRWORDS (dRICH words)
- dRWORDS out in timeframes to SRO computing

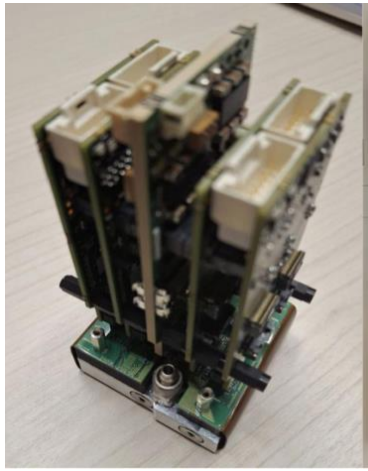
Collaboration with ALICE-DAQ for testing “simple” data transmission on FLX-182

Conclusions and outlook

- Keen to test soon ALCORv3: stay tuned
- RDO built and tested. On-going: scrubbing firmware / SRO firmware / radiation tests
- FELIX DAQ is coming: first data transfers over optical link
- Data format and division of “duties” between dRICH RDO and DAM under discussion

→ We plan to report full dRICH - SRO implementation @SRO-XIV!

PDU



RDO

DAM

(many credits to several INFN colleagues for various slides: F. Cossio, S. Geminiani, A. Lonardo, R. Preghenella, C. Rossi)

Conclusions and outlook

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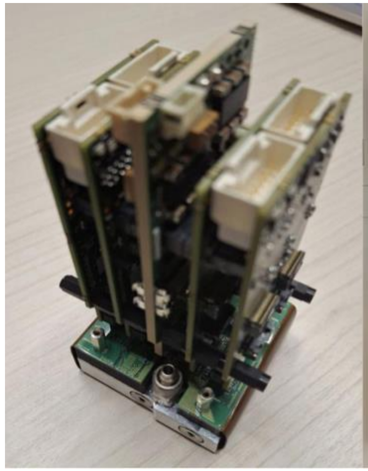


RDO

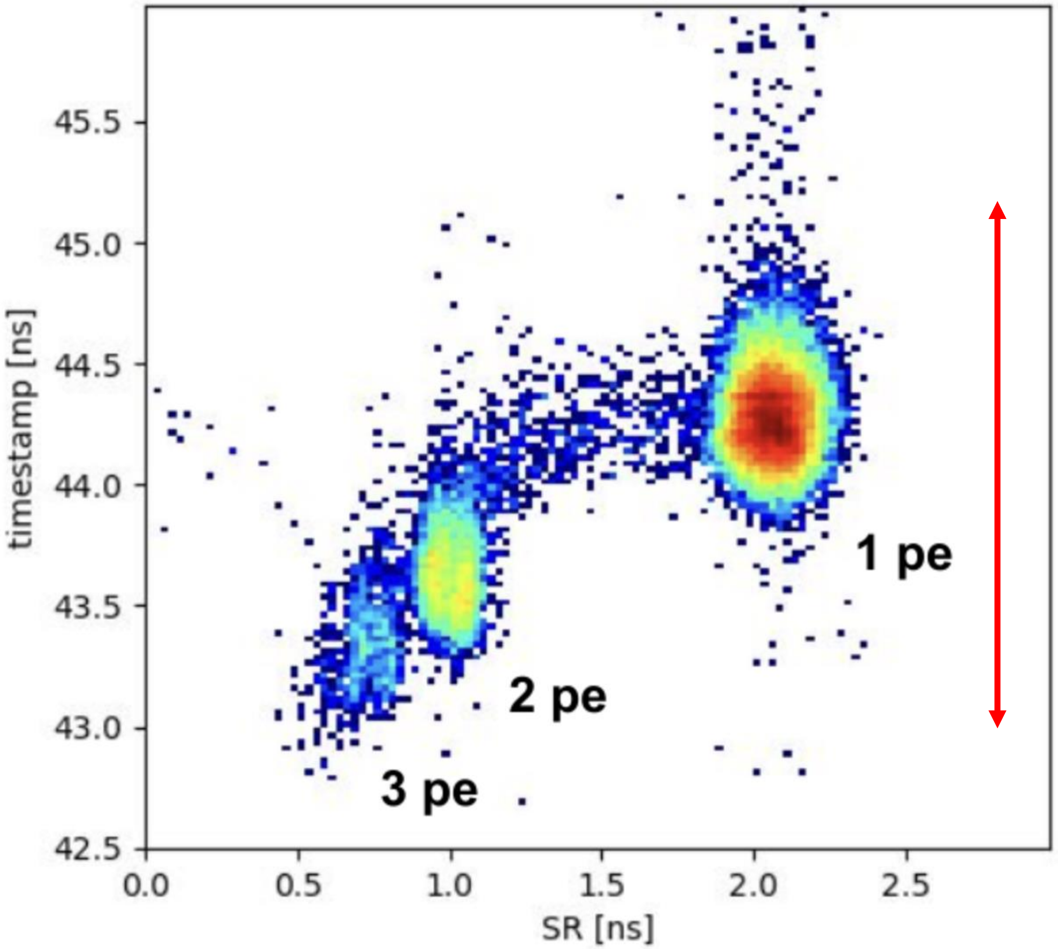
DAM

(many credits to several INFN colleagues for various slides: F. Cossio, S. Geminiani, A. Lonardo, R. Preghenella, C. Rossi)


BACKUP

Further analysis: time slewing warning

Time slewing effect due to multiple photons



For the fraction of events when we will have > 1 pe we can expect an additional shift of ~ **2 ns**!

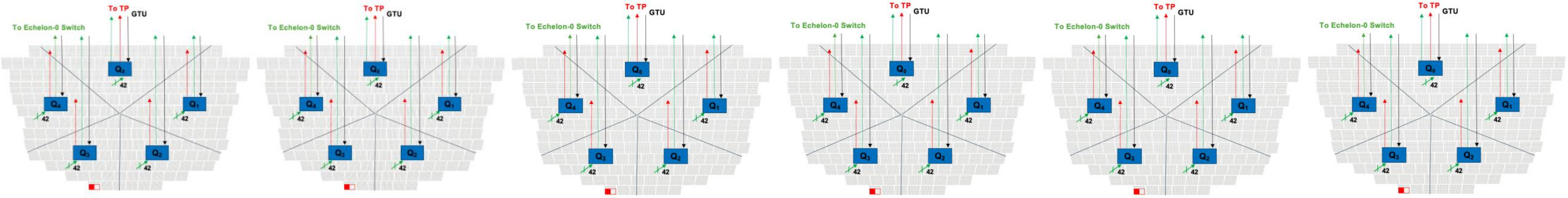
How many times we have more than 1 pe?
Note we have also SiPM-cross talk here.

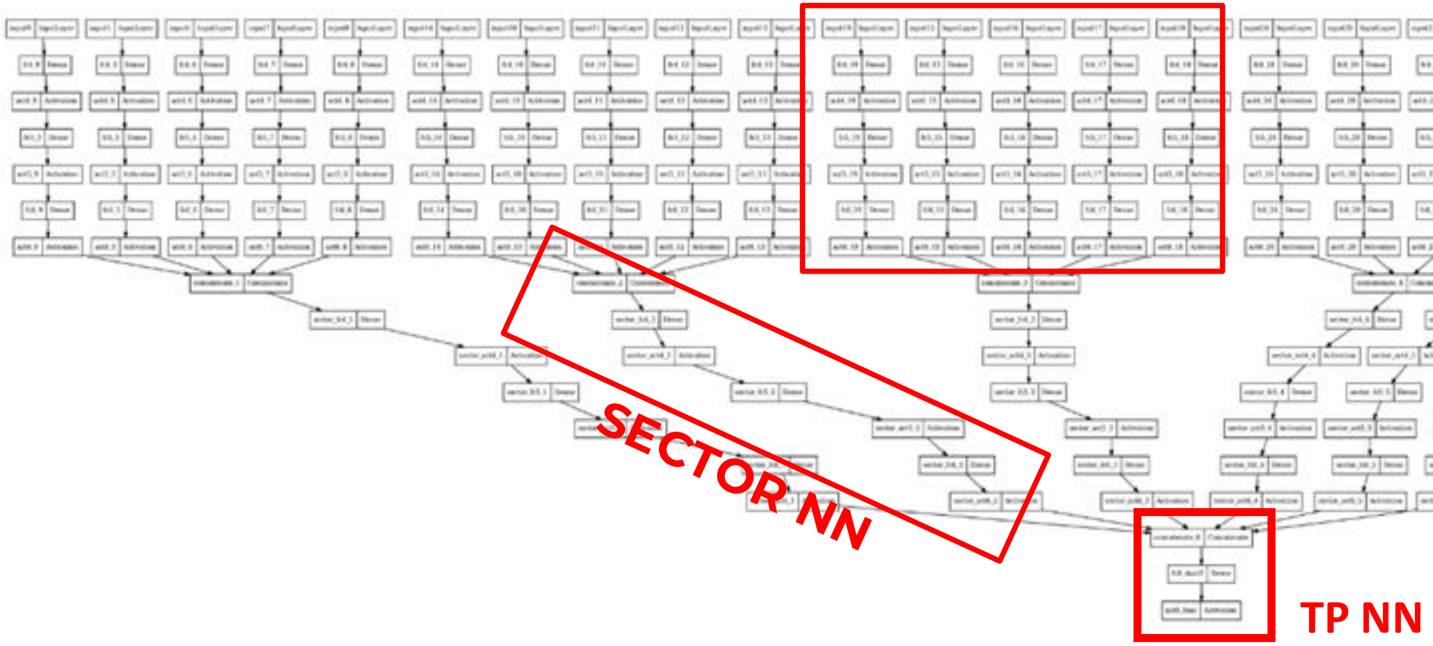
To be fully simulated.

Shutter could be "off" 5 – 3 ns
→ Shutter reduction factor 0.5 – 0.37

NN deployment model and DAMs

6 dRICH sectors – 5 DAMs/sectors





The 6 dRICH sector-NNs and final TP NN are deployed on 31st dRICH FLX-155

dRICH RDO requirements

- **space**: 40 x 90 mm area
- RDO not accessible: **remote firmware upgrade** must be possible

- RDO FPGA need **high speed** (“high performance”) 120 I/O pins to implement ALCOR bus towards FEBs
- RDO connector need high speed specs. and (minimum) 60 I/O pins each

- RDO must implement clean **clock** multiplication (ALCOR@394 MHz, EIC clock 98.5 MHz)
- RDO must reconstruct clock via optical link
- RDO must produce clean clock (minimize jitter)

- **opt. tranceiver** must minimize space/power consumption + “rad hard” and bandwitdh up to 10 Gbps