Karlsruhe Institute of Technology

BULLKID-DM Readout Electronics

Bimonthly digest, 12.11.2025

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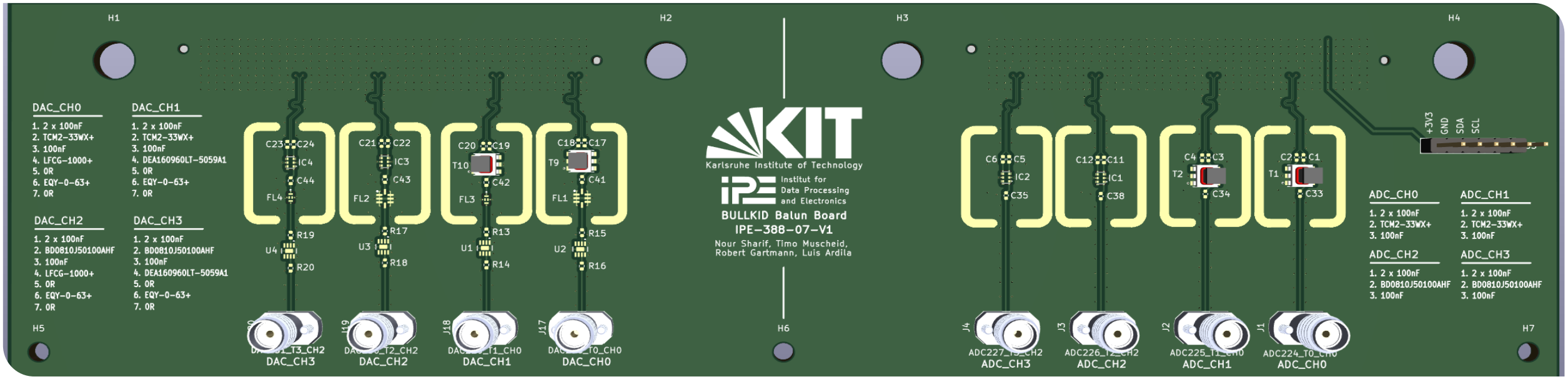
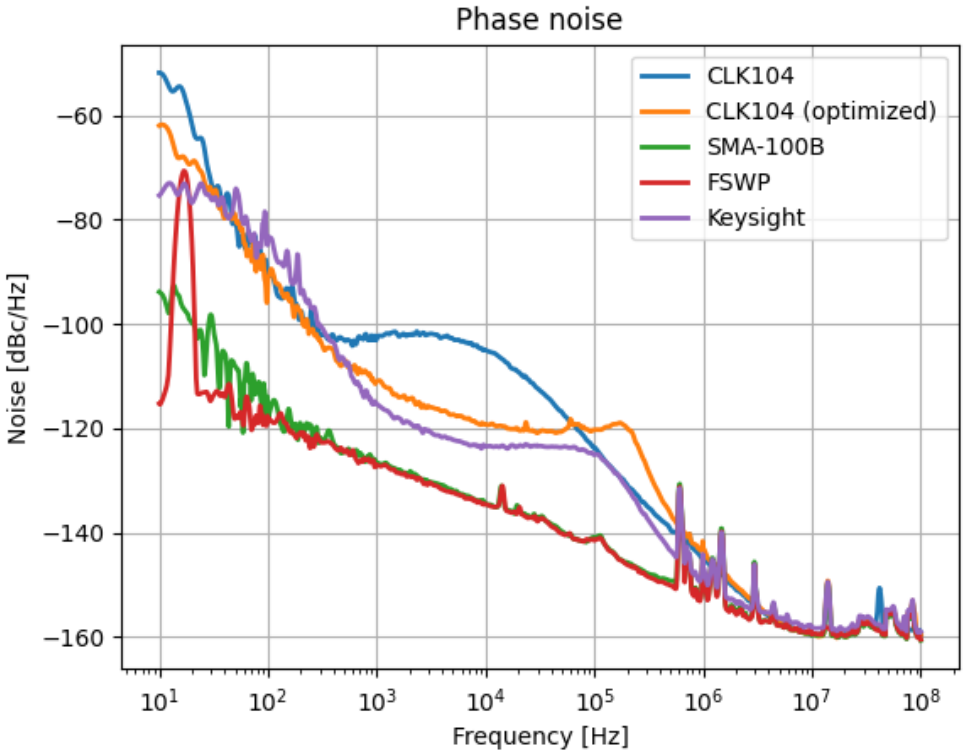


Recap

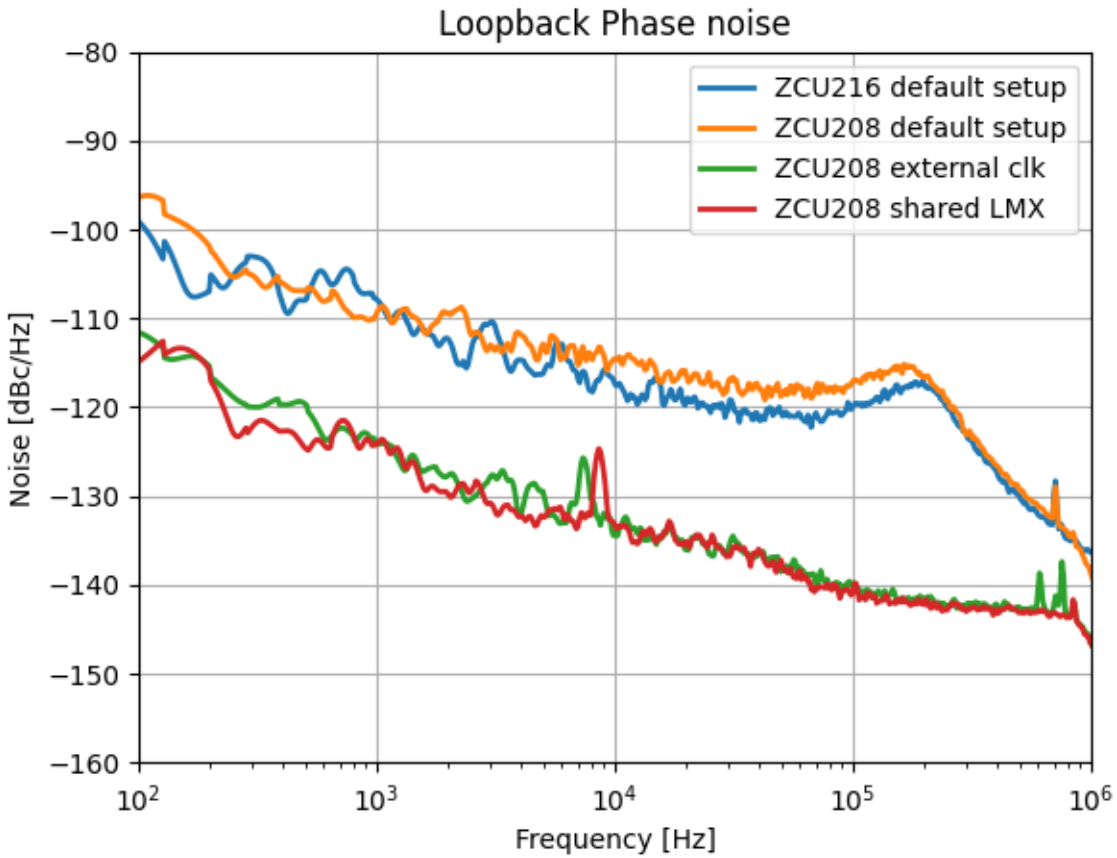
- Noise performance
  - Main contribution: Phase noise of clock
  - Improvement using external synthesizers
- Frequency resolution of carrier tones
  - Current approach not feasible for full-scale electronics
  - Limited resources in programmable logic



Single tone (831 MHz), full amplitude

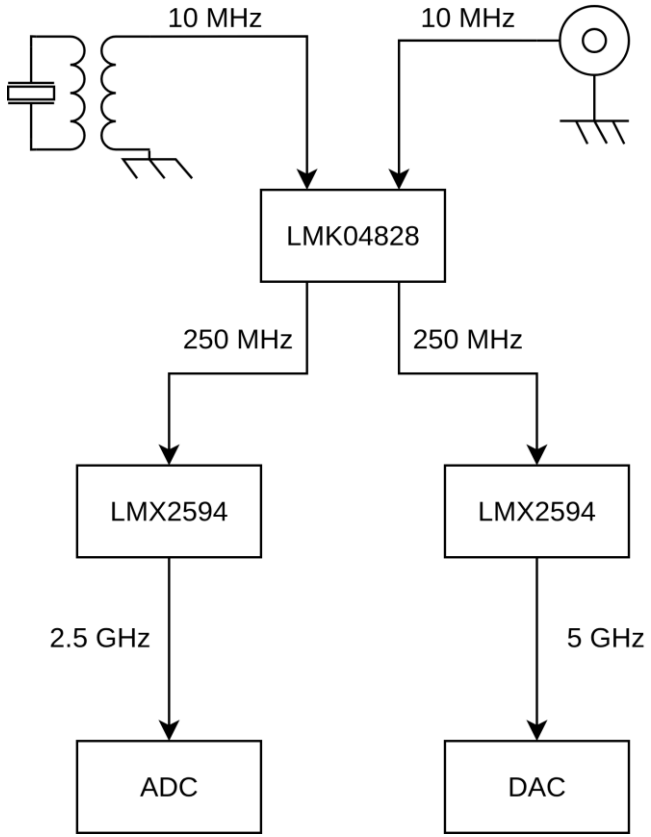
Evaluation of ZCU208

- DAC and ADC with 5 GHz
- Common external clock
  (R&S SMA100-B with PNO option)
- Alternative: Same clock chip for both converters
  -> Phase noise cancels out

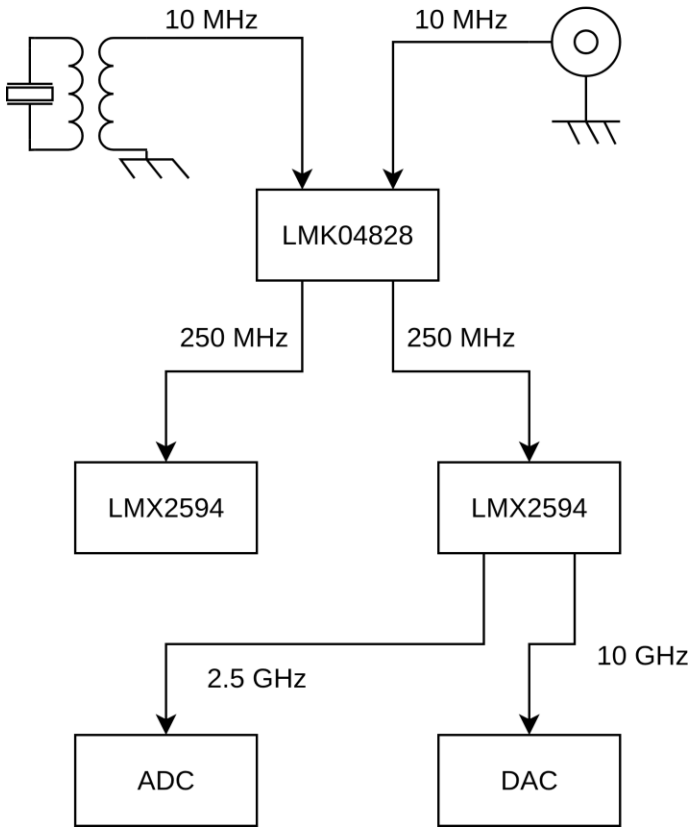


Optimization of ZCU216 Clock Tree

Old Setup

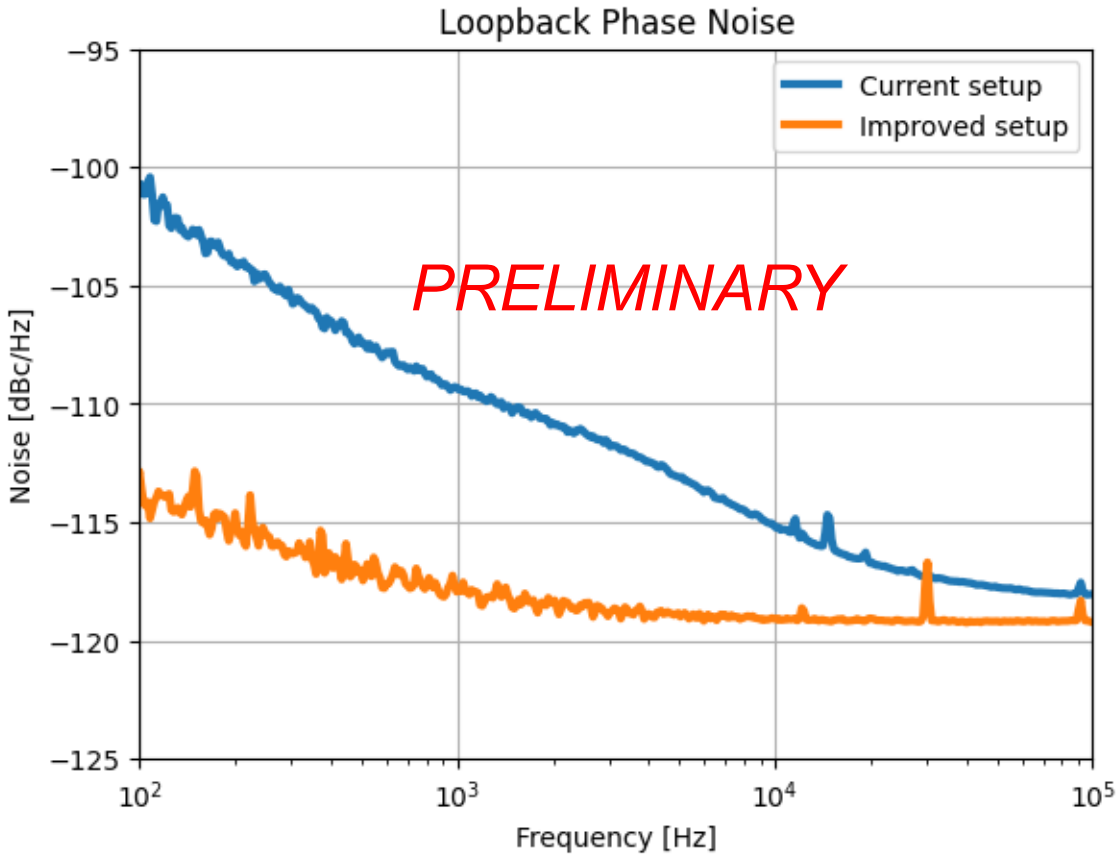


New Setup



Newest results (11.11.2025)

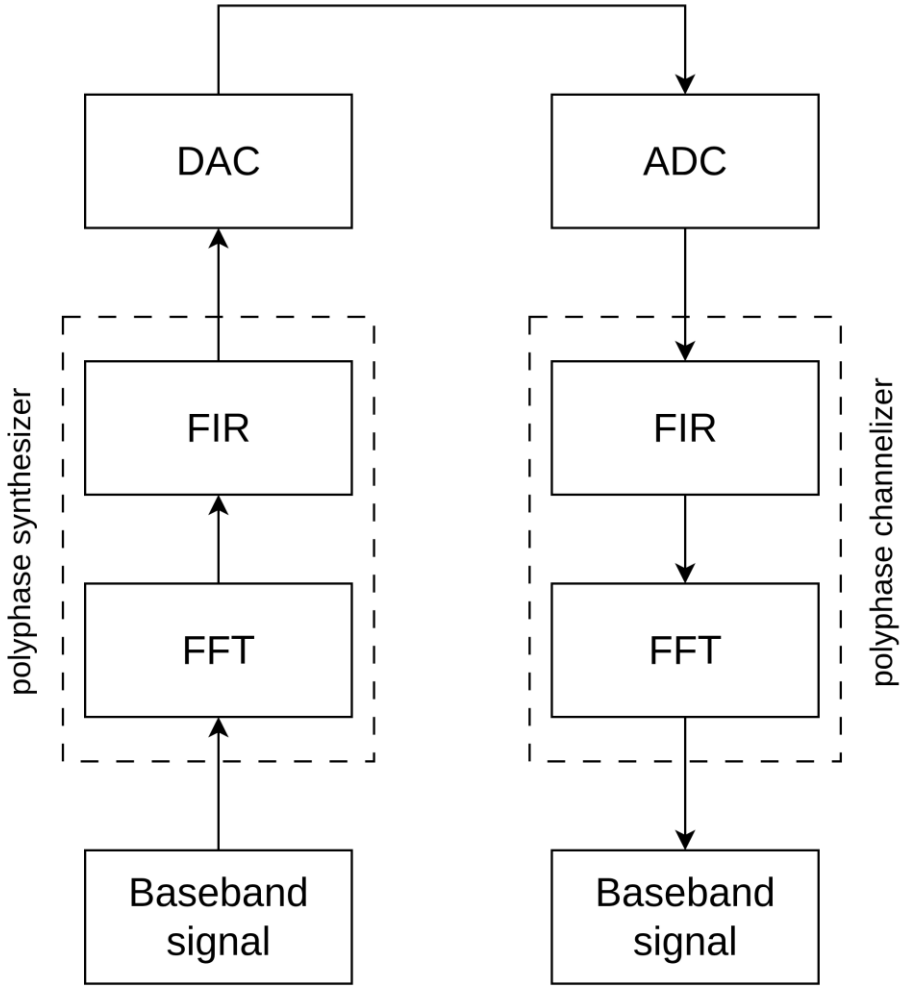
- New clocking scheme improves noise without new hardware
- 10 GHz clock of DAC additionally improves SFDR
- More measurements required for final statement



Phase noise of demodulated signal

Carrier Tone Generation

- Use inverted polyphase channelizer -> polyphase synthesizer
- Frequency resolution: < 1 Hz
- Based on DSP, less memory consumption
- Implementation almost ready, can be tested before the end of the year



Other news

- Fixed persistent error on system in Rome
  -> Many thanks to Davide for support
- Submitted paper about electronics
  -> Focus on demultiplexing and noise
- Add-on board for LANTERN integration
  -> Design 95% ready, order next week