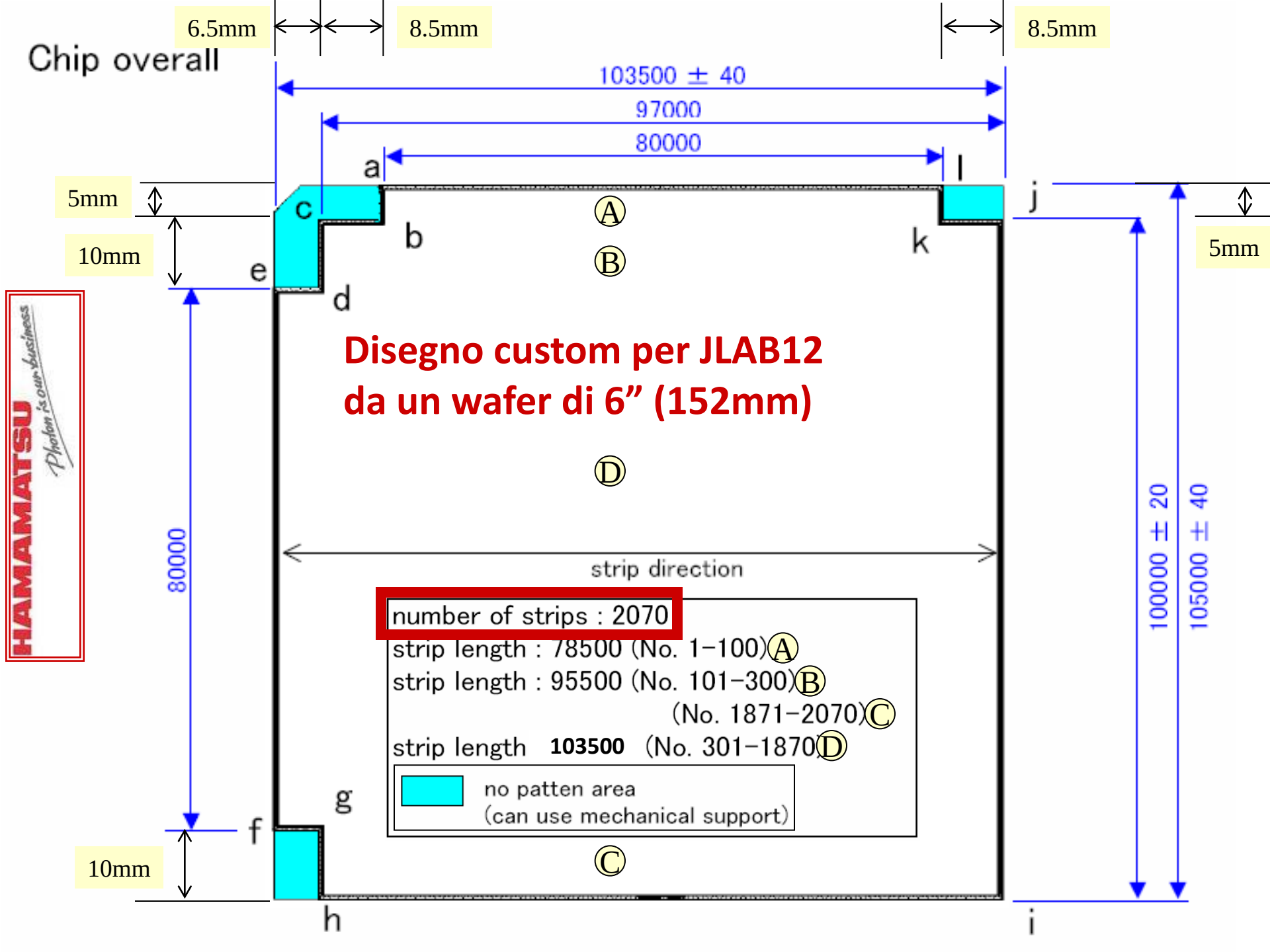
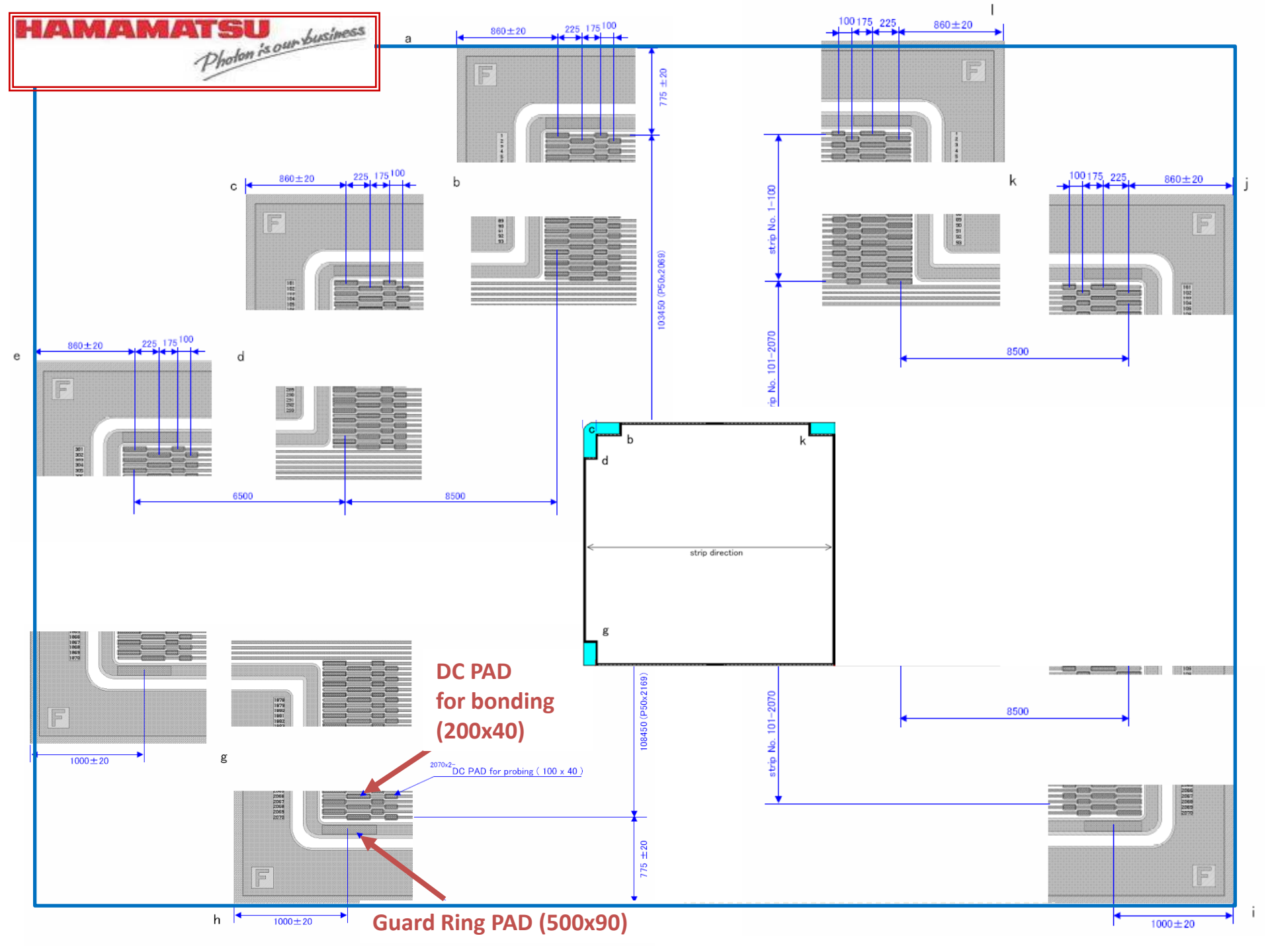
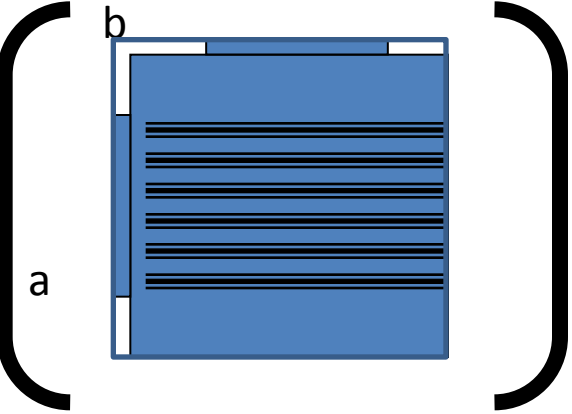
Status attivita' Roma1 2011/2012

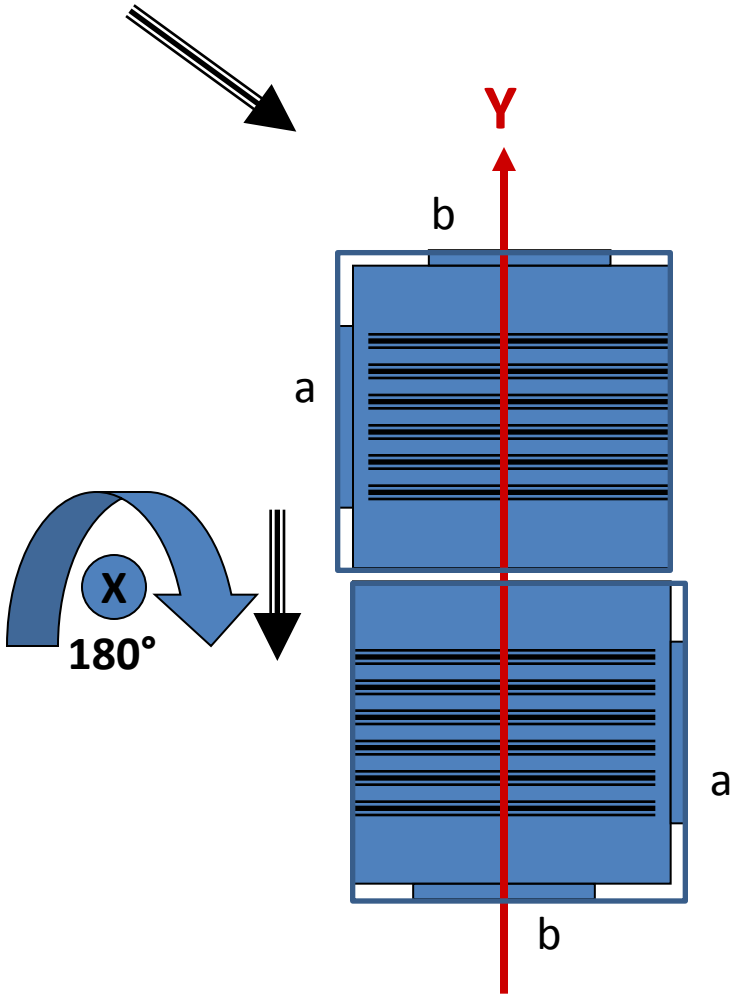
INDICE:

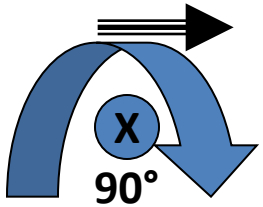

Chip overall
6.5mm
8.5mm
8.5mm
103500 ± 40
97000
80000
a
l
5mm
c
A
j
5mm
10mm
b
k
B
e
d
Disegno custom per JLAB12
da un wafer di 6” (152mm)
D
80000
strip direction
100000 ± 20
105000 ± 40
number of strips : 2070
strip length : 78500 (No. 1-100) A
strip length : 95500 (No. 101-300) B
(No. 1871-2070) C
strip length 103500 (No. 301-1870) D
no patten area
(can use mechanical support)
g
f
10mm
C
h
i
HAMAMATSU
Photon is our business

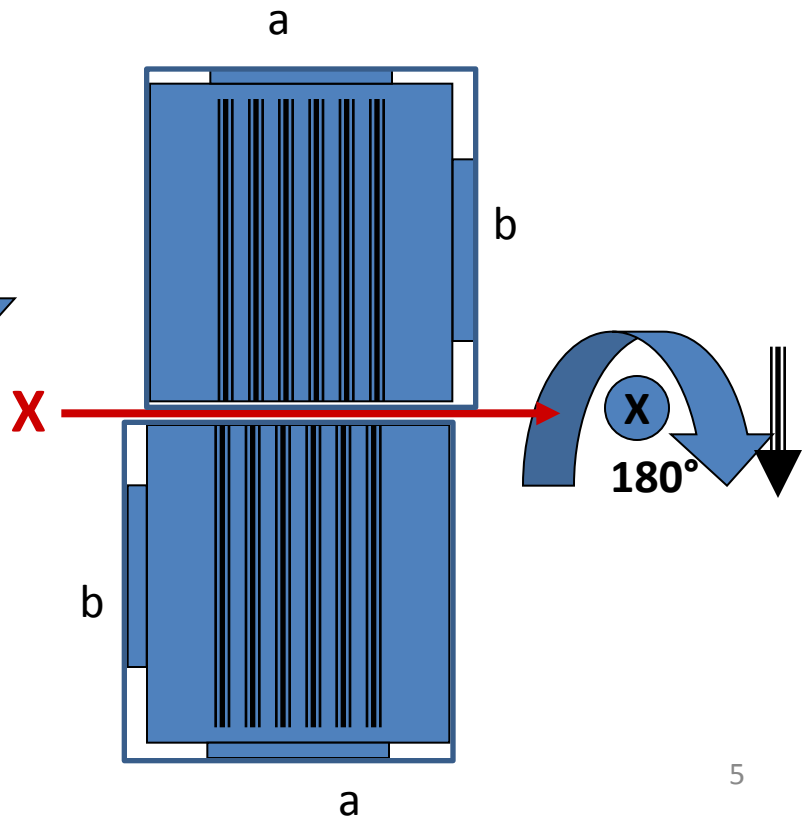

HAMAMATSU
Photon is our business
a
b
c
d
e
g
h
i
j
k
l
860±20
225
175
100
775±20
103450 (P50x2069)
strip No. 1–100
strip No. 101–2070
8500
6500
strip direction
108450 (P50x2169)
1000±20
2070×2
DC PAD for probing (100 x 40)
DC PAD
for bonding
(200x40)
Guard Ring PAD (500x90)

Dal rivelatore (Hamamatsu) ai Piani X e Y









PCB Rigido per SiD:

- **Necessità di ottimizzare gli ingombri, e la lunghezza delle piste.**

- **Necessità di ottimizzare il piano di massa.**

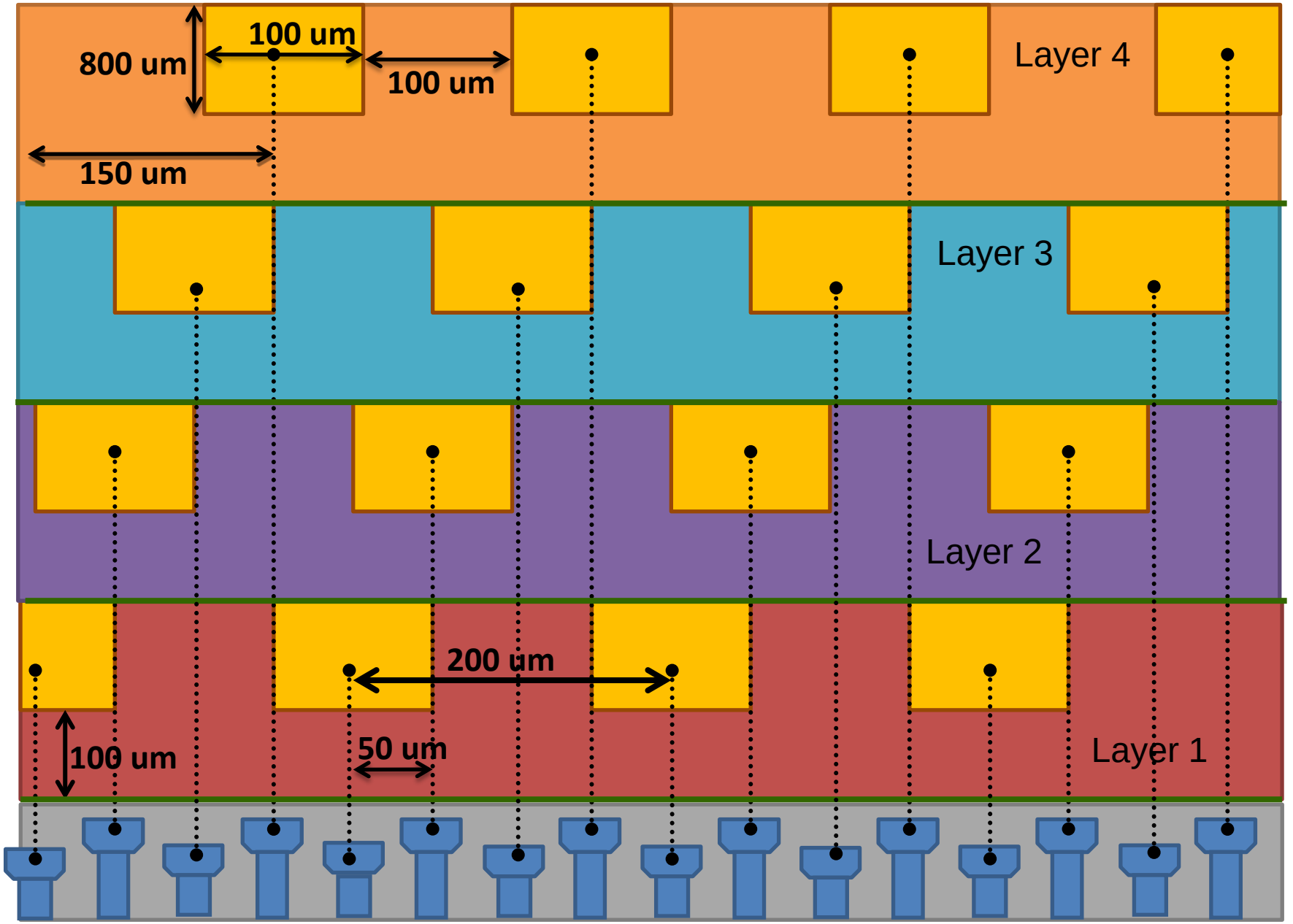
- **Necessità di progettare due PCB rigidi distinti, di uguali dimensioni, per i piani X e Y.**

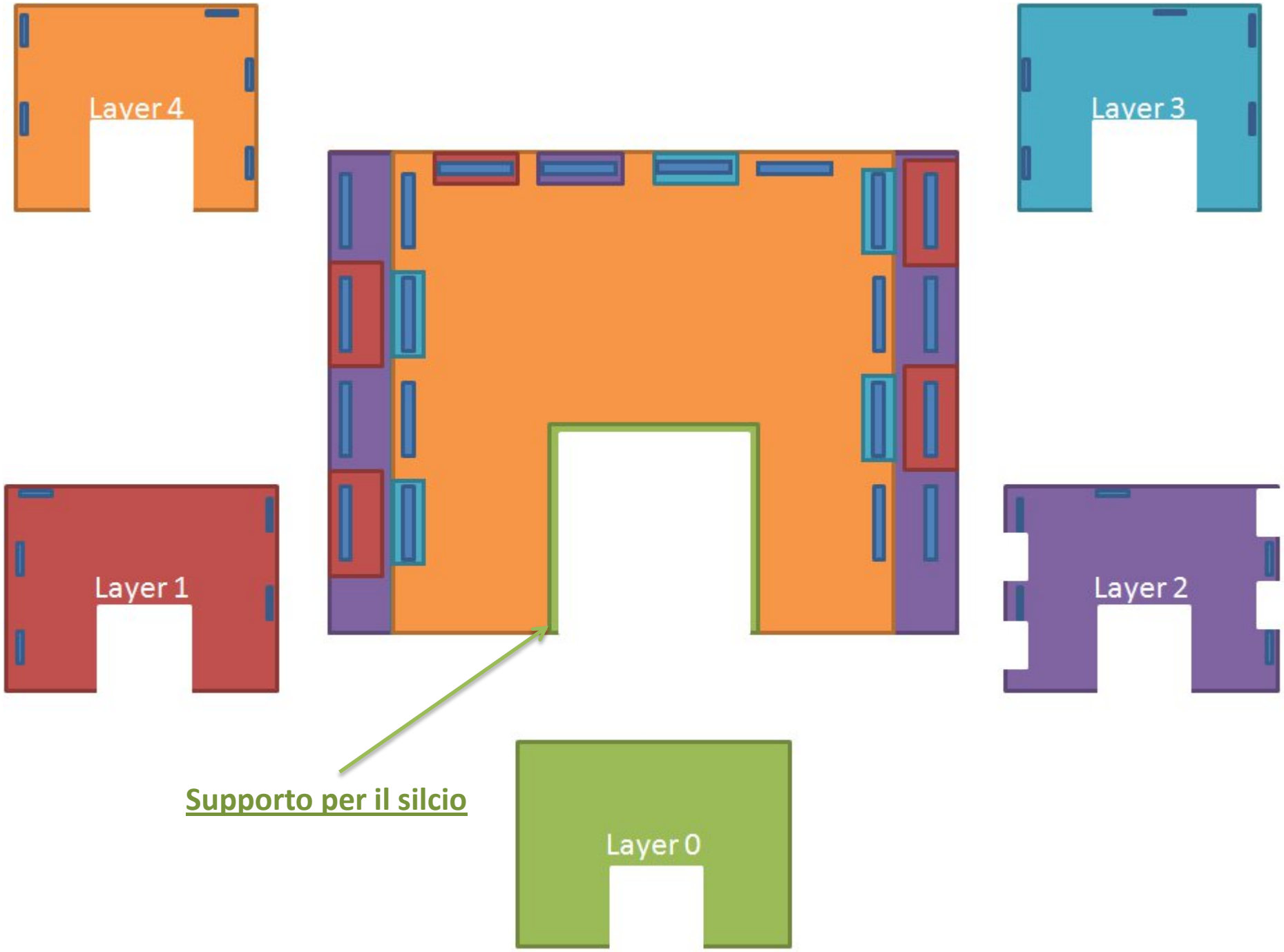
- **Necessità di prevedere una culla di alloggiamento del rivelatore al silicio (SiD) nel PCB rigido stesso.**

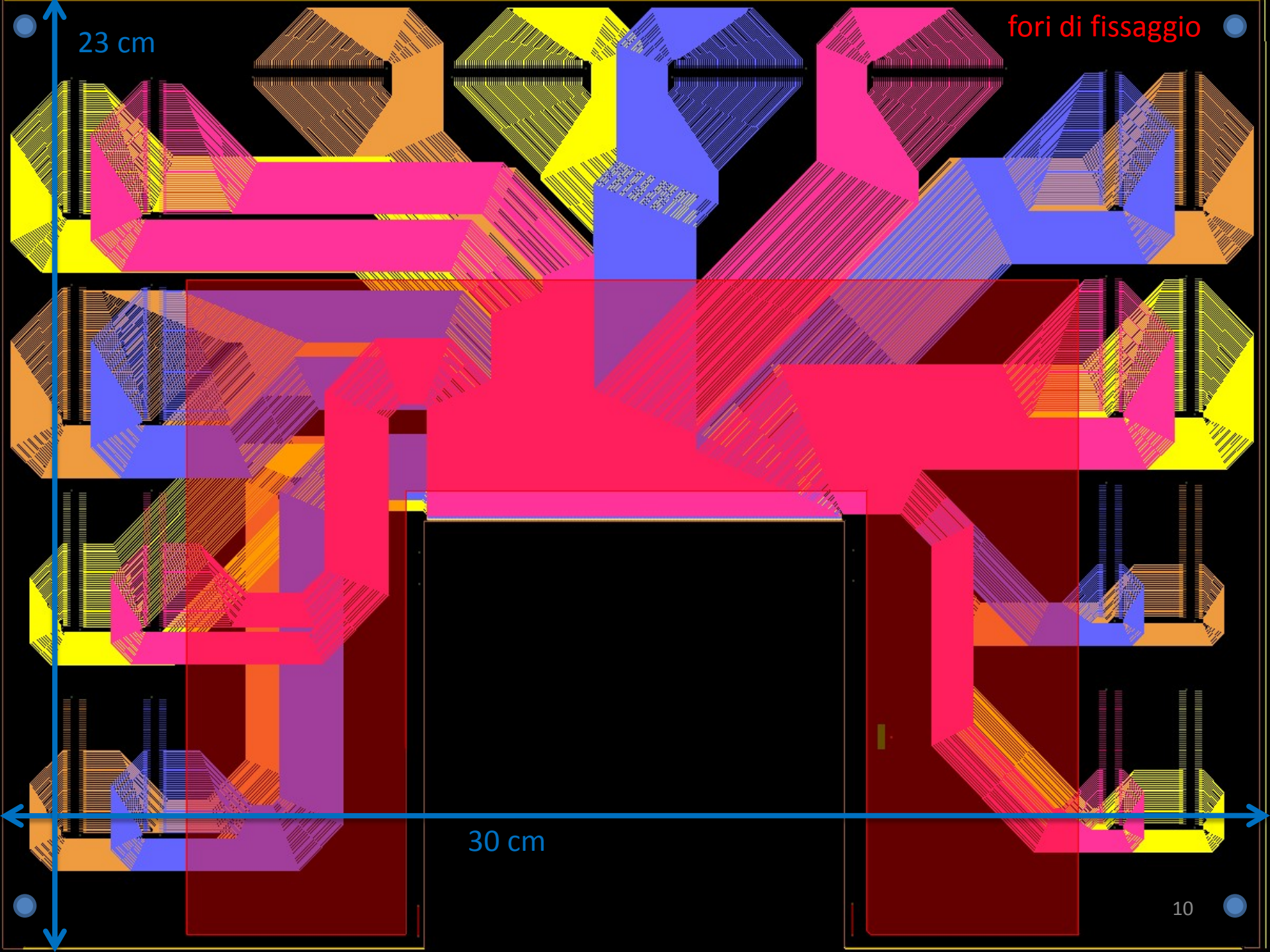
- **Necessità di poter essere realizzato con le attuali capacità tecnologiche ad un costo contenuto.**

PIANO X

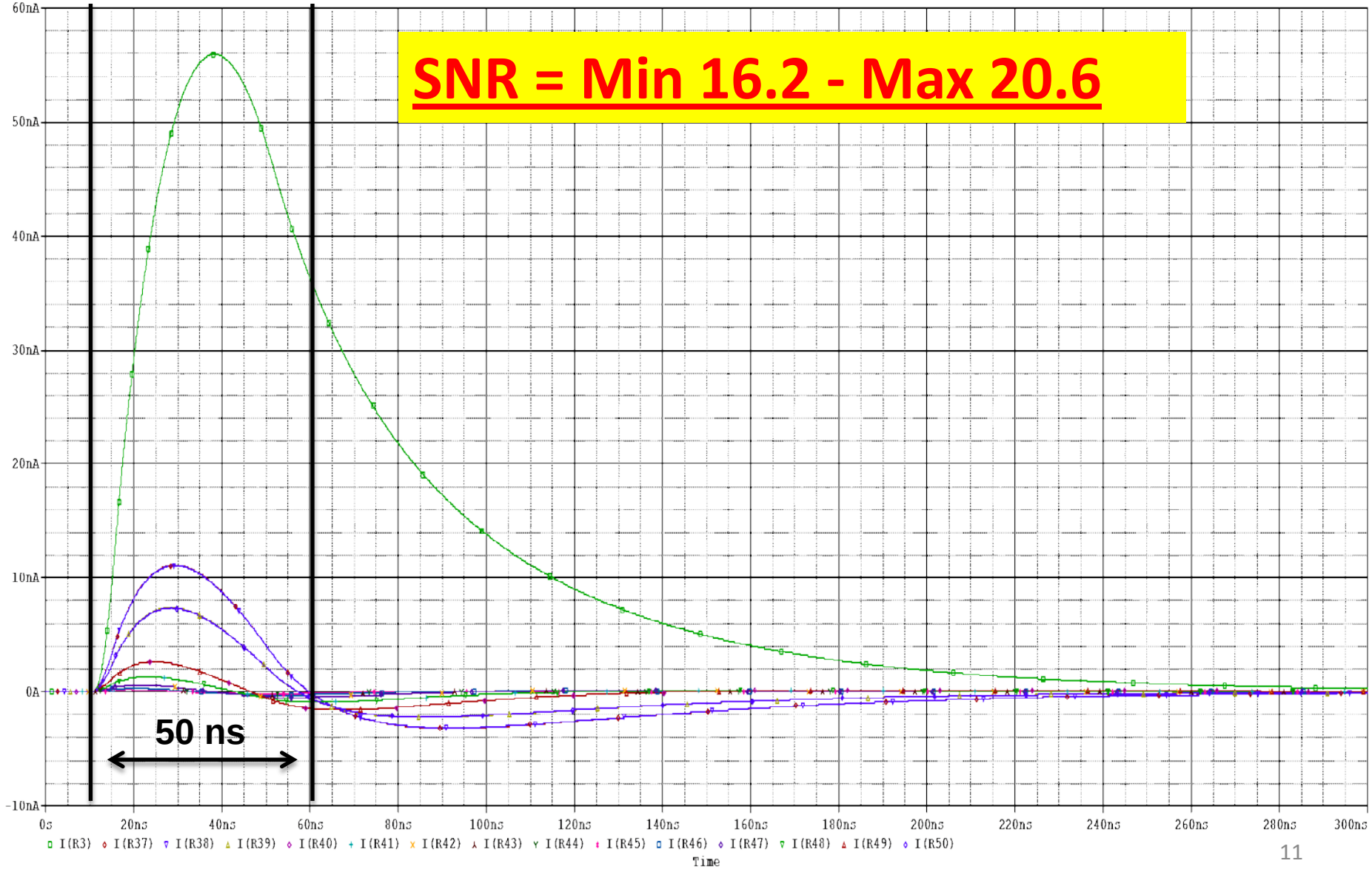
PCB X formato da 4 strati o Layer



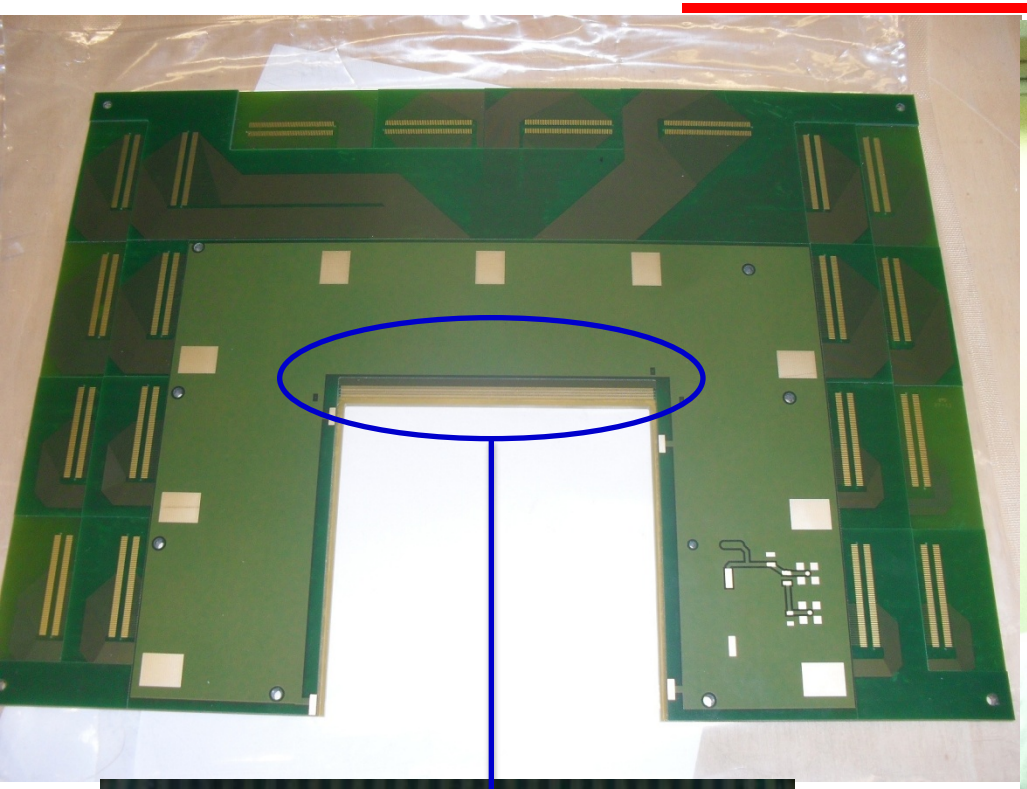

Layer 4
Layer 3
Layer 1
Layer 2
Supporto per il silcio
Layer 0

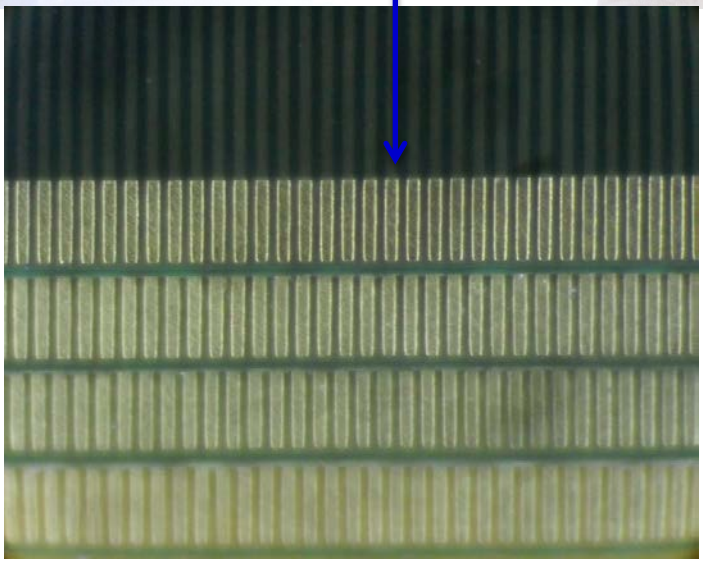

23 cm
fori di fissaggio
30 cm

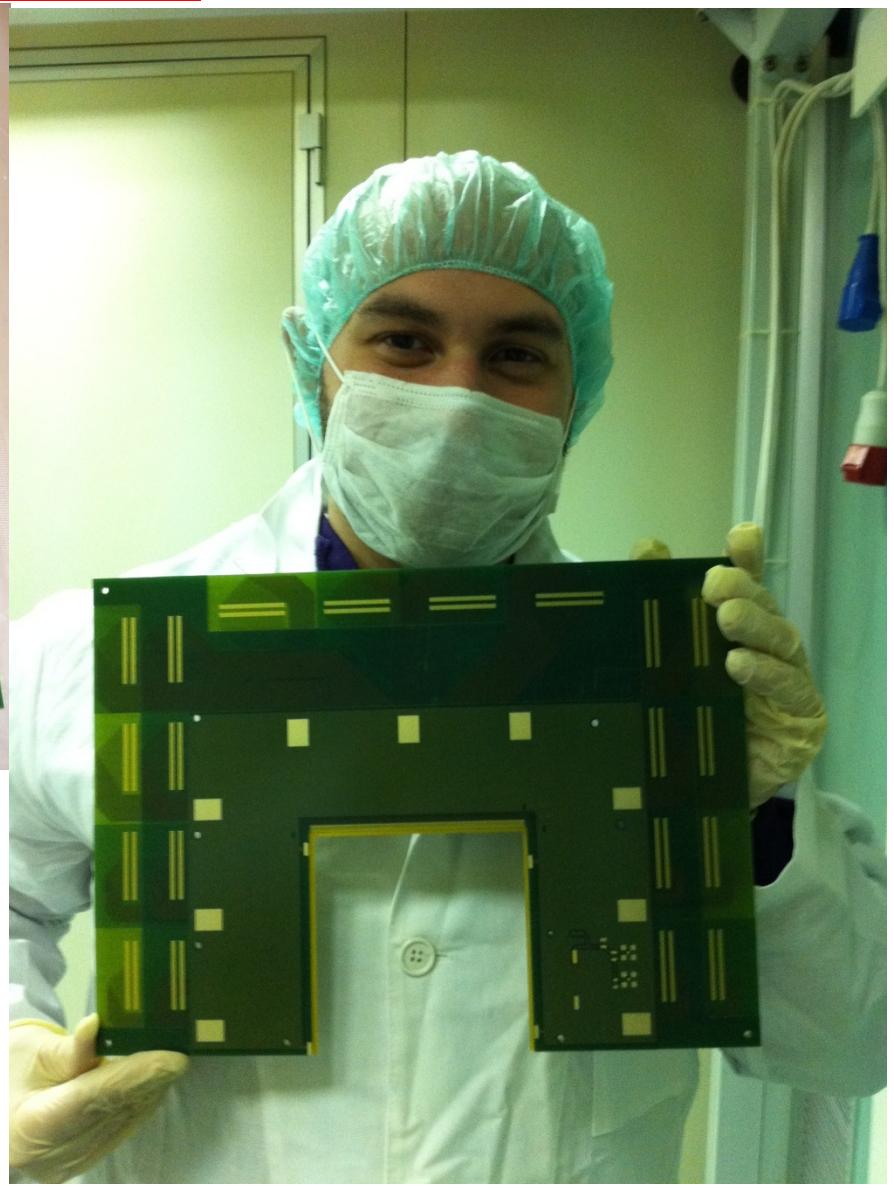
Risultati delle simulazioni delle piste del PCB X

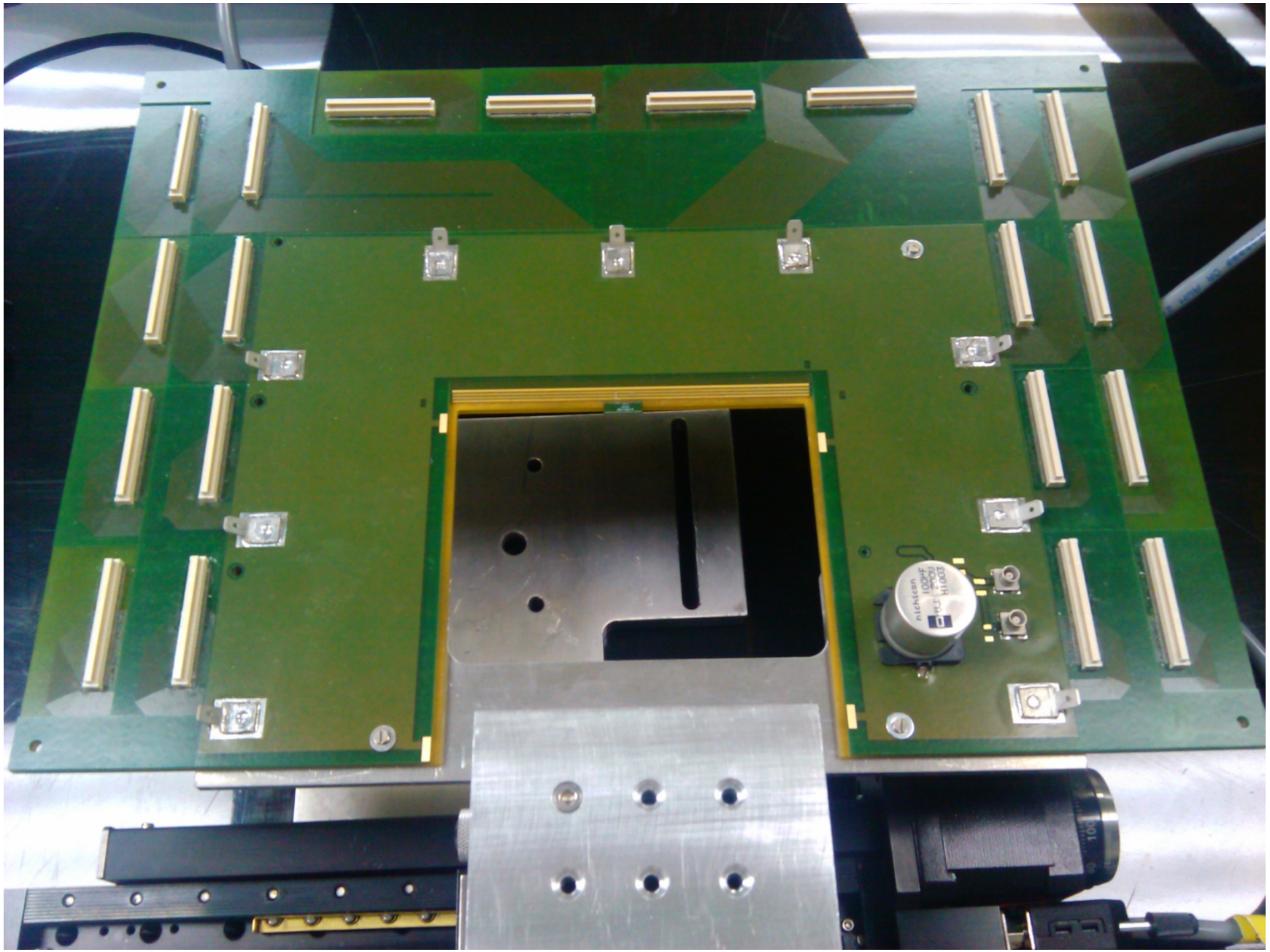


PCB Piano X.

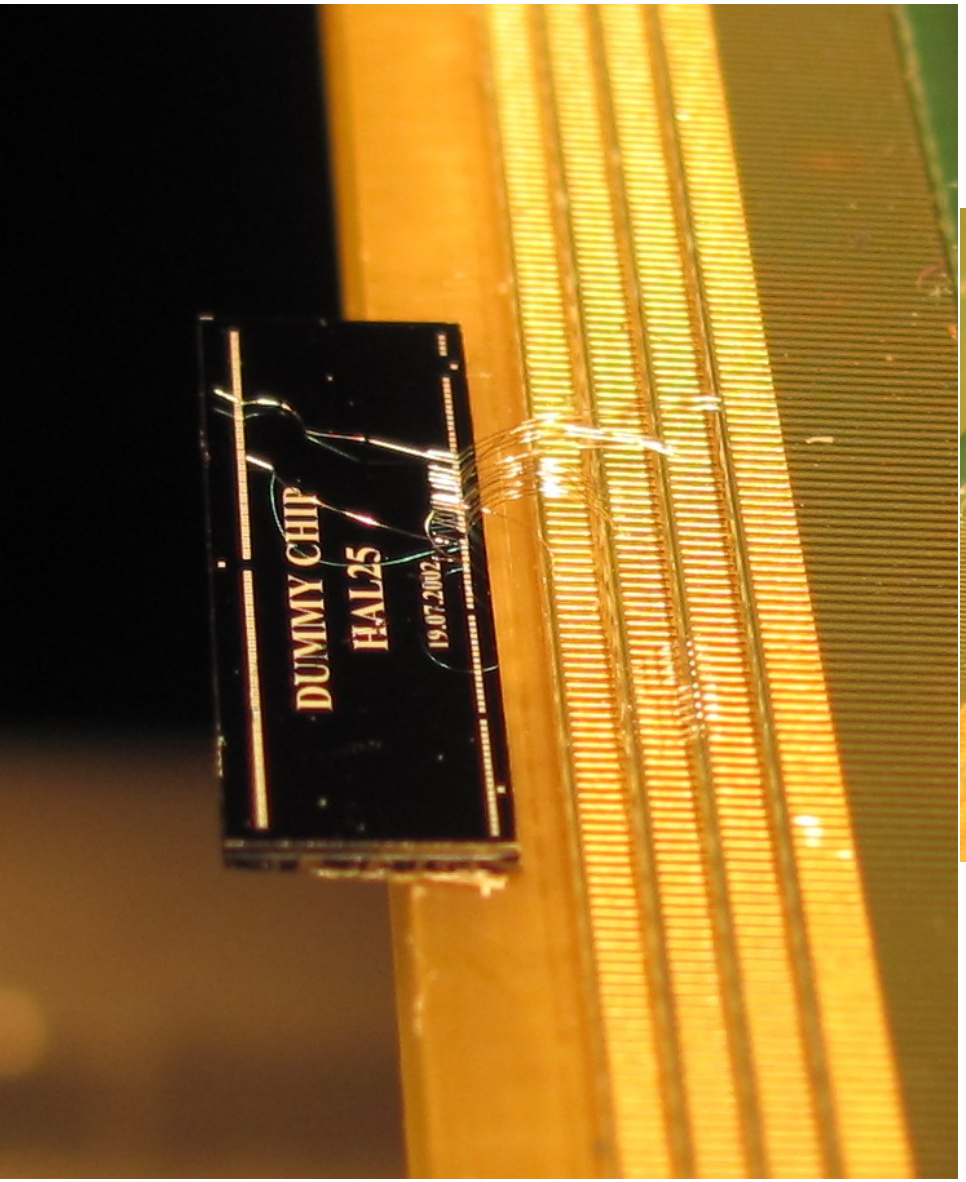


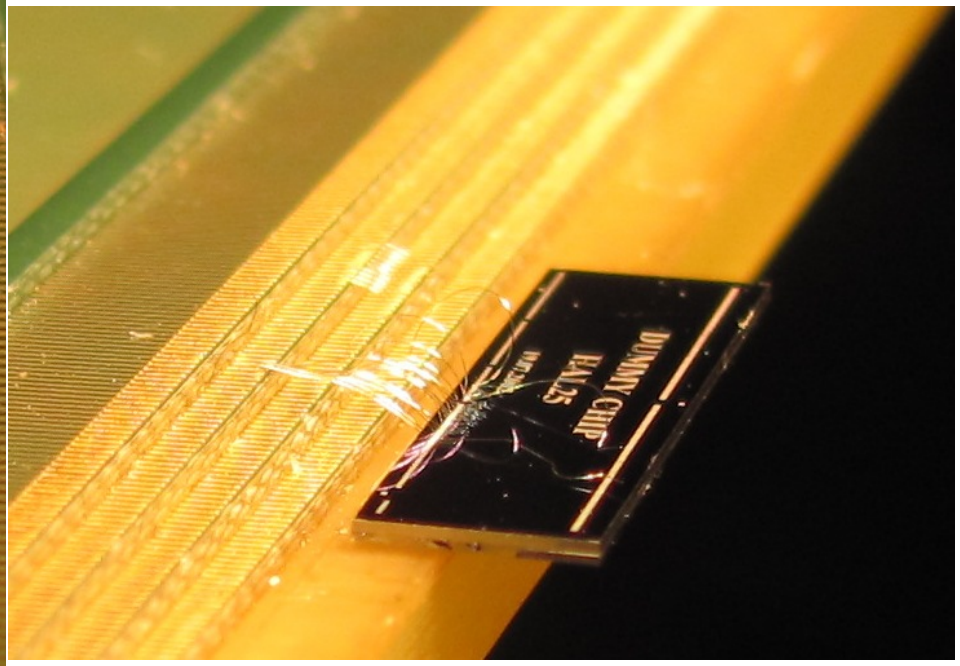




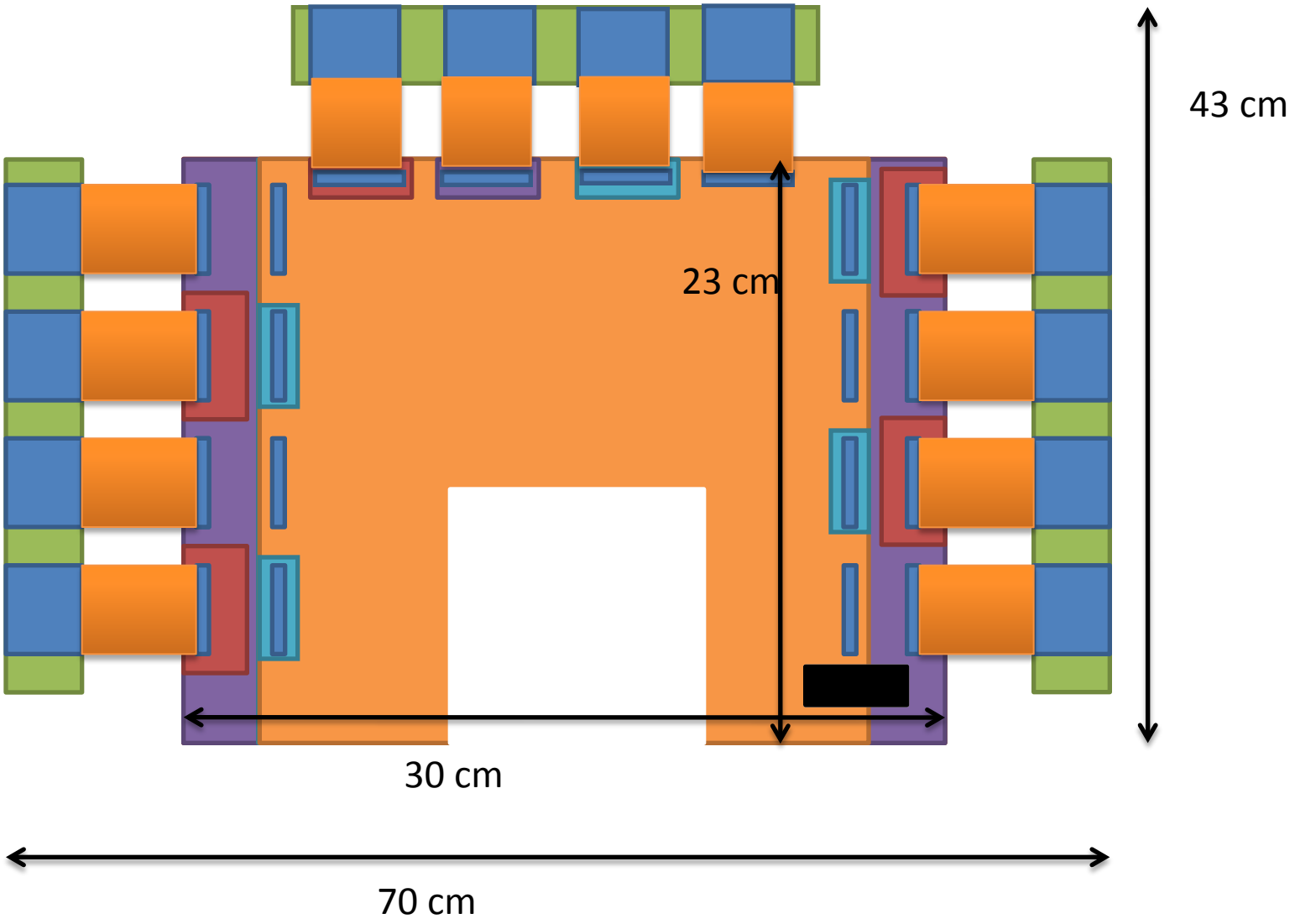


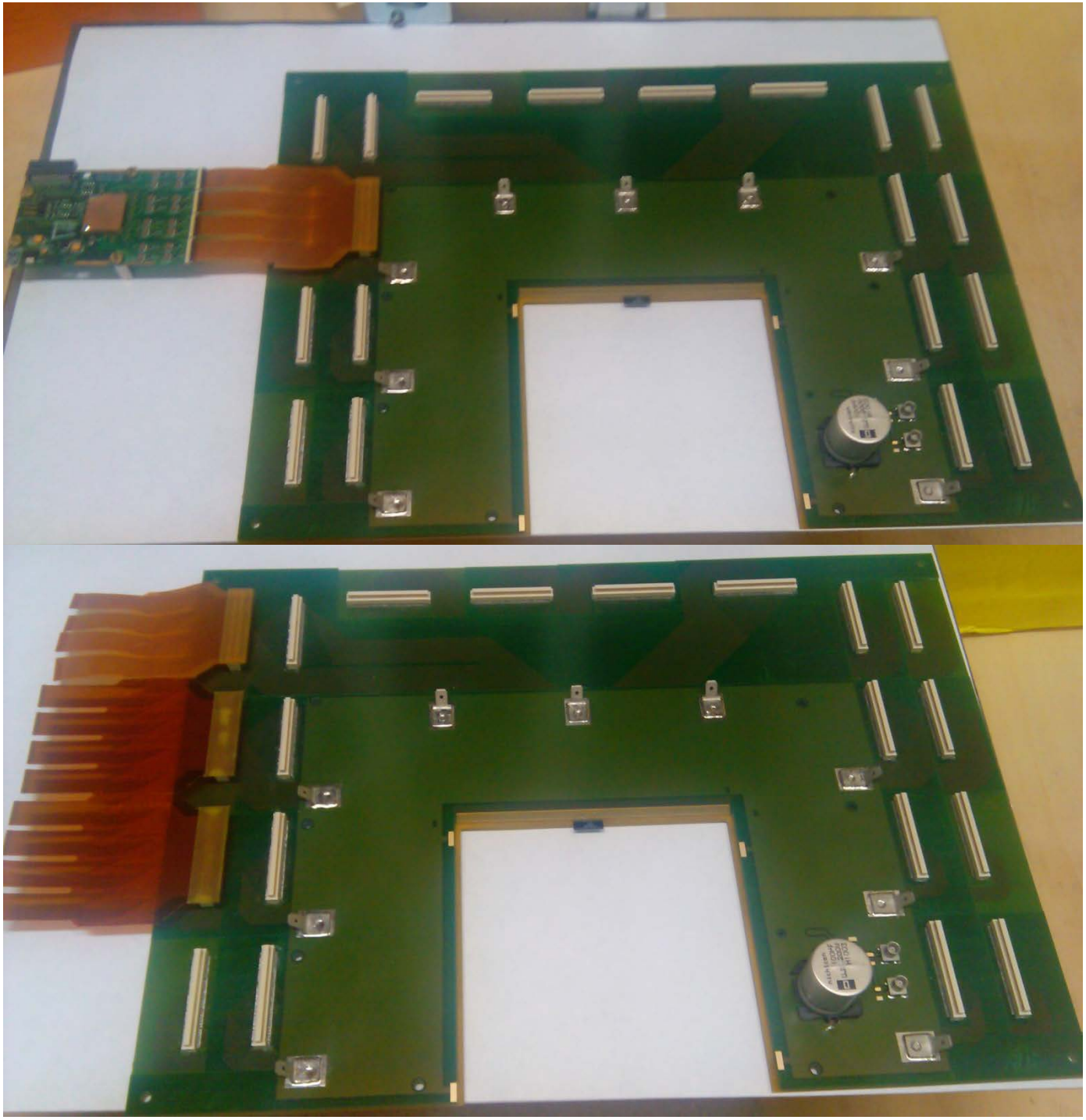
Prove di Saldatura ad Ultrasuoni sul terrazzamento





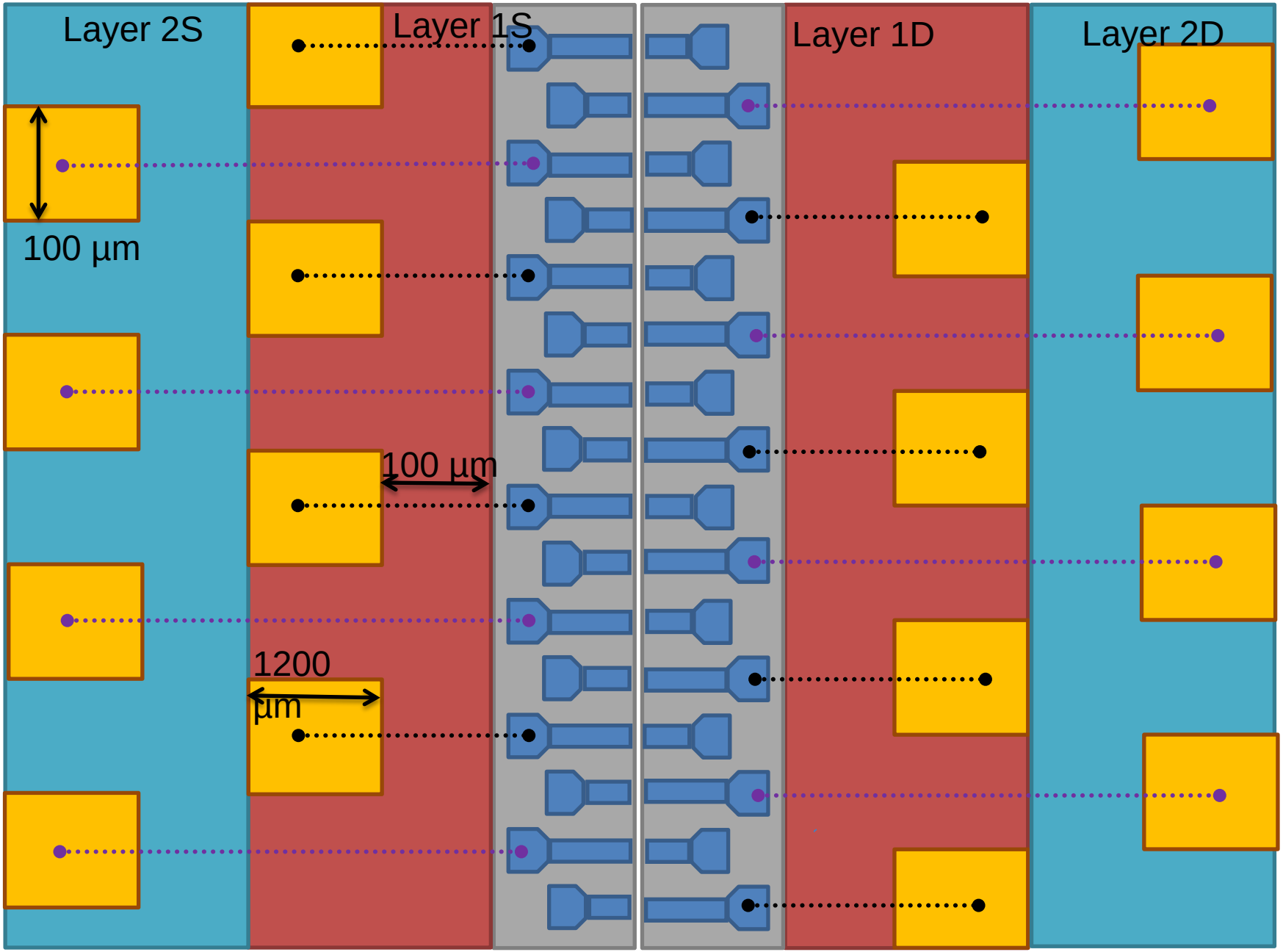
Vista Frontale del semi piano X



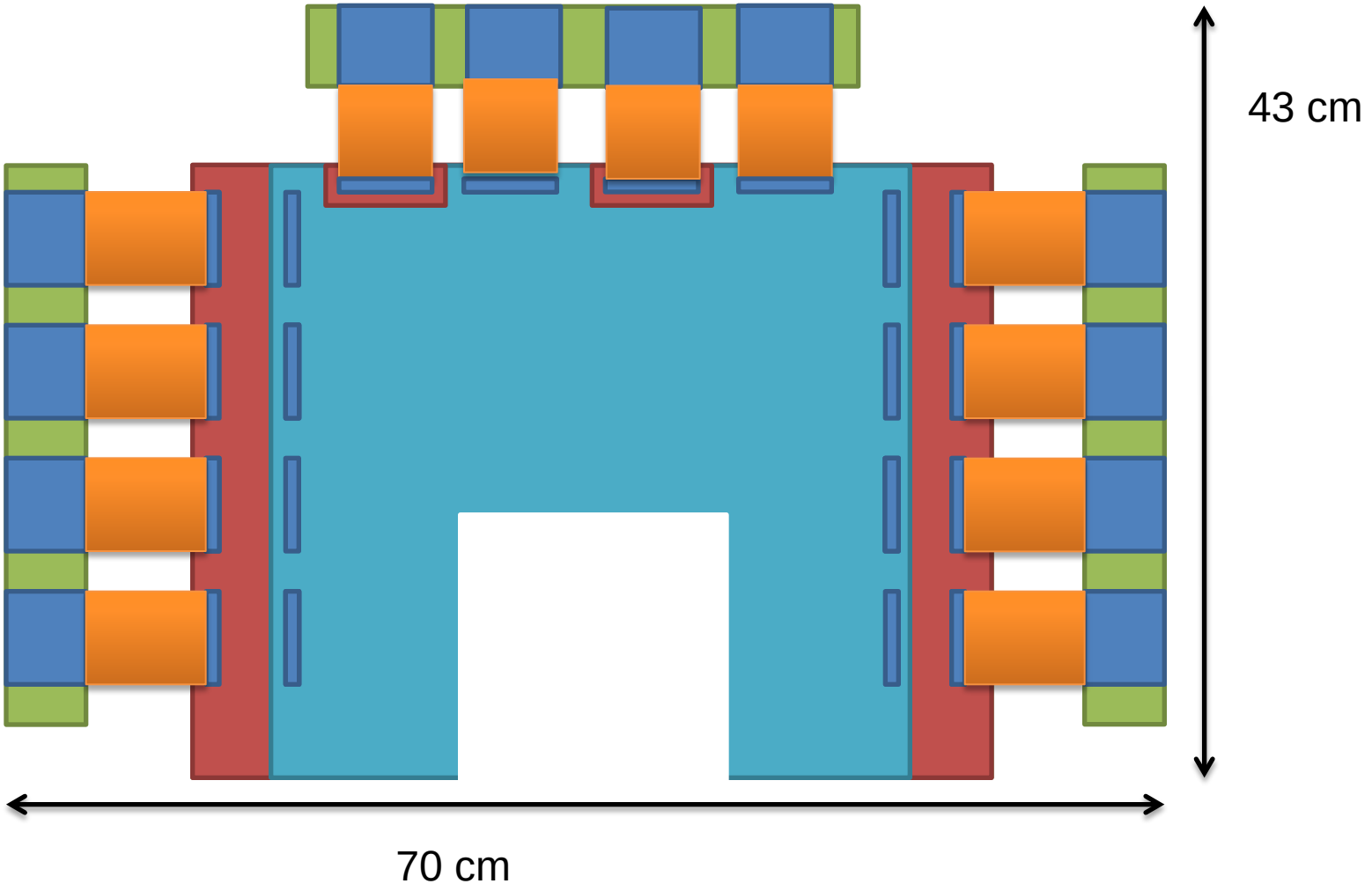


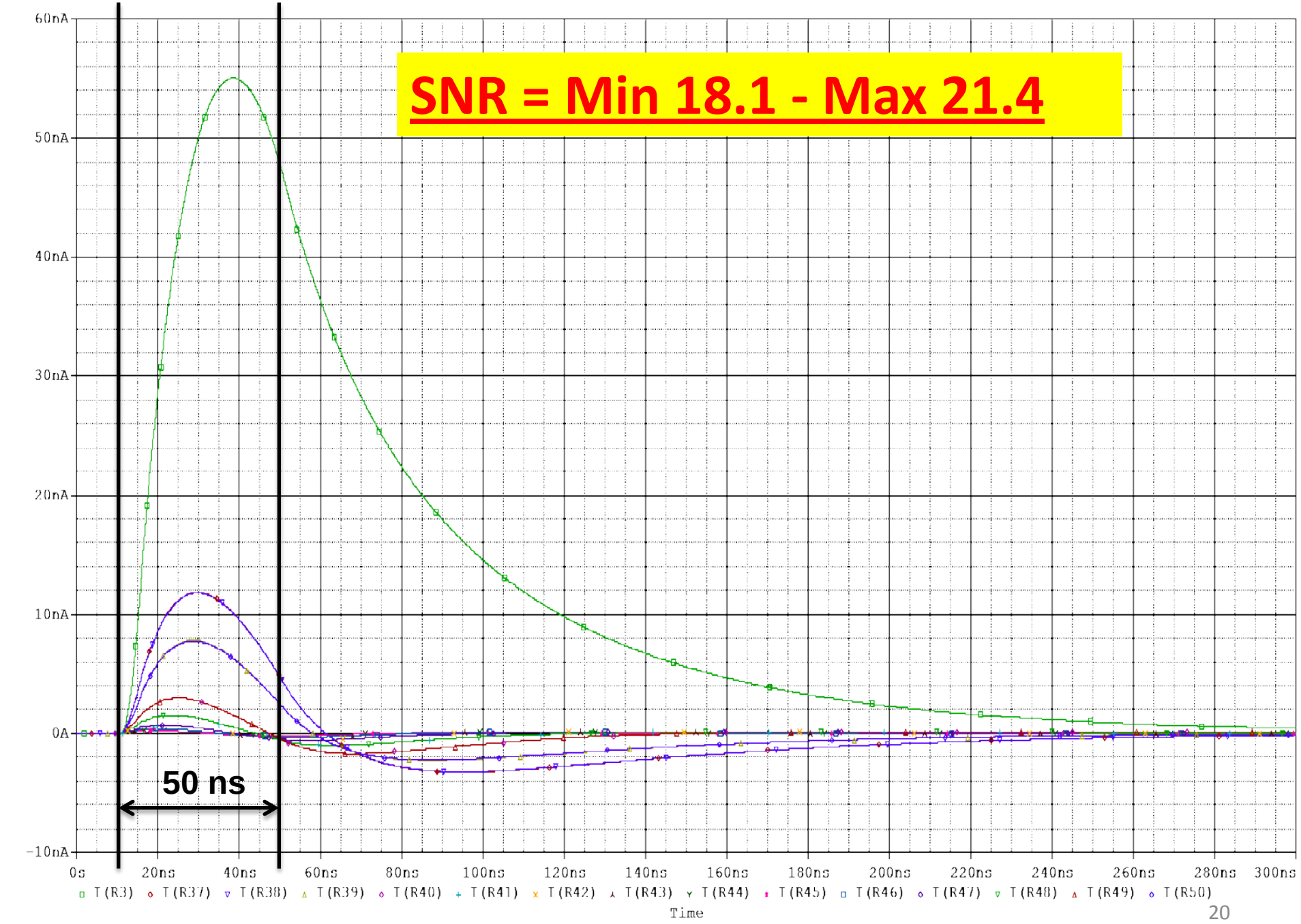
PIANO Y

PCB Y formato da 2 strati o Layer



Vista dall'alto dell'intero sistema PCB e Backplane (con i connettori aggiungivi)




SNR = Min 18.1 - Max 21.4
60nA
50nA
40nA
30nA
20nA
10nA
0A
-10nA
50 ns
0s
20ns
40ns
60ns
80ns
100ns
120ns
140ns
160ns
180ns
200ns
220ns
240ns
260ns
280ns
300ns
T(R36) T(R37) T(R38) T(R39) T(R40) T(R41) T(R42) T(R43) T(R44) T(R45) T(R46) T(R47) T(R48) T(R49) T(R50)
Time

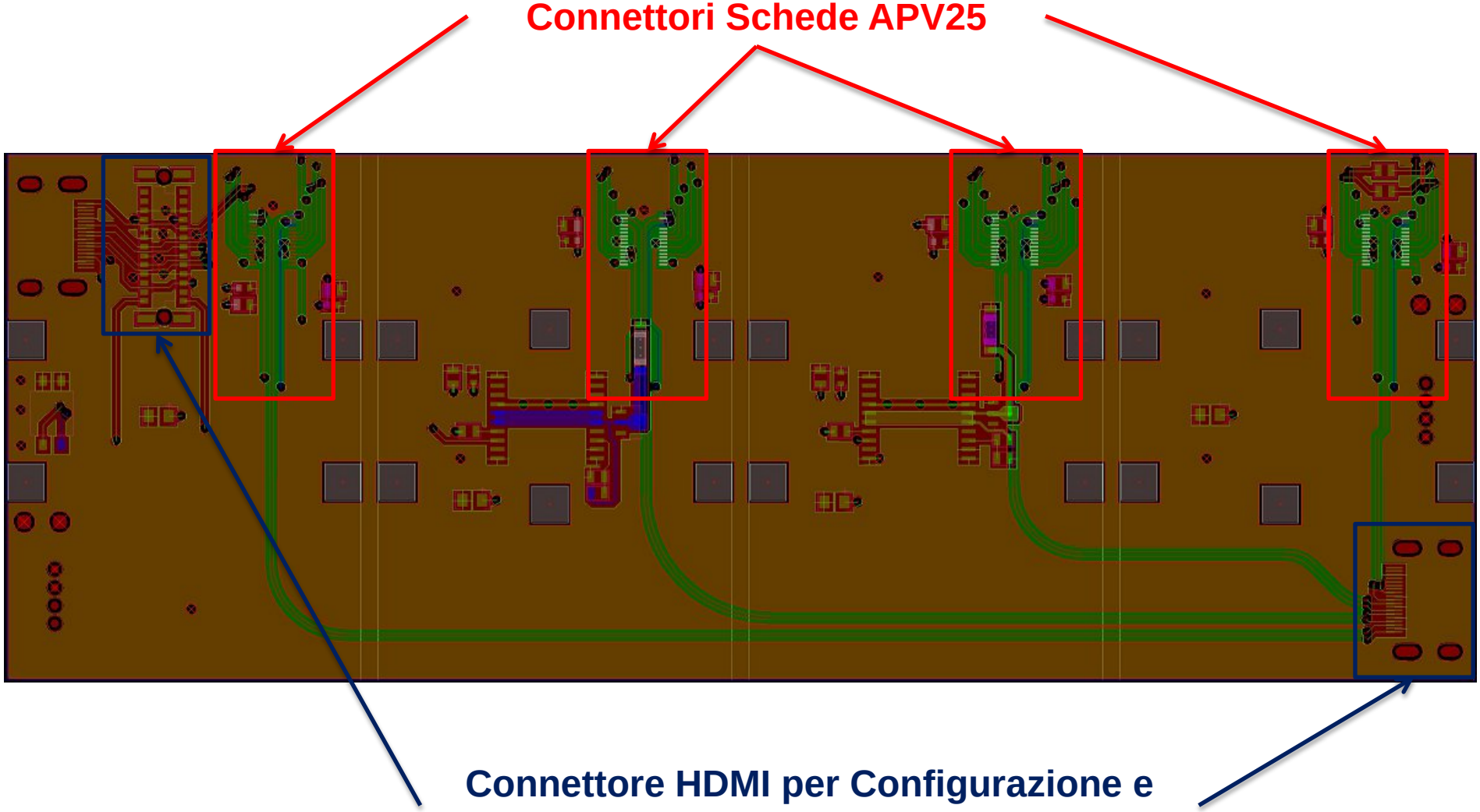
SNR del PCB X e PCB Y

SNR	PCB X	PCB Y
MIN	16.2	18.1
MAX	20.6	21.4

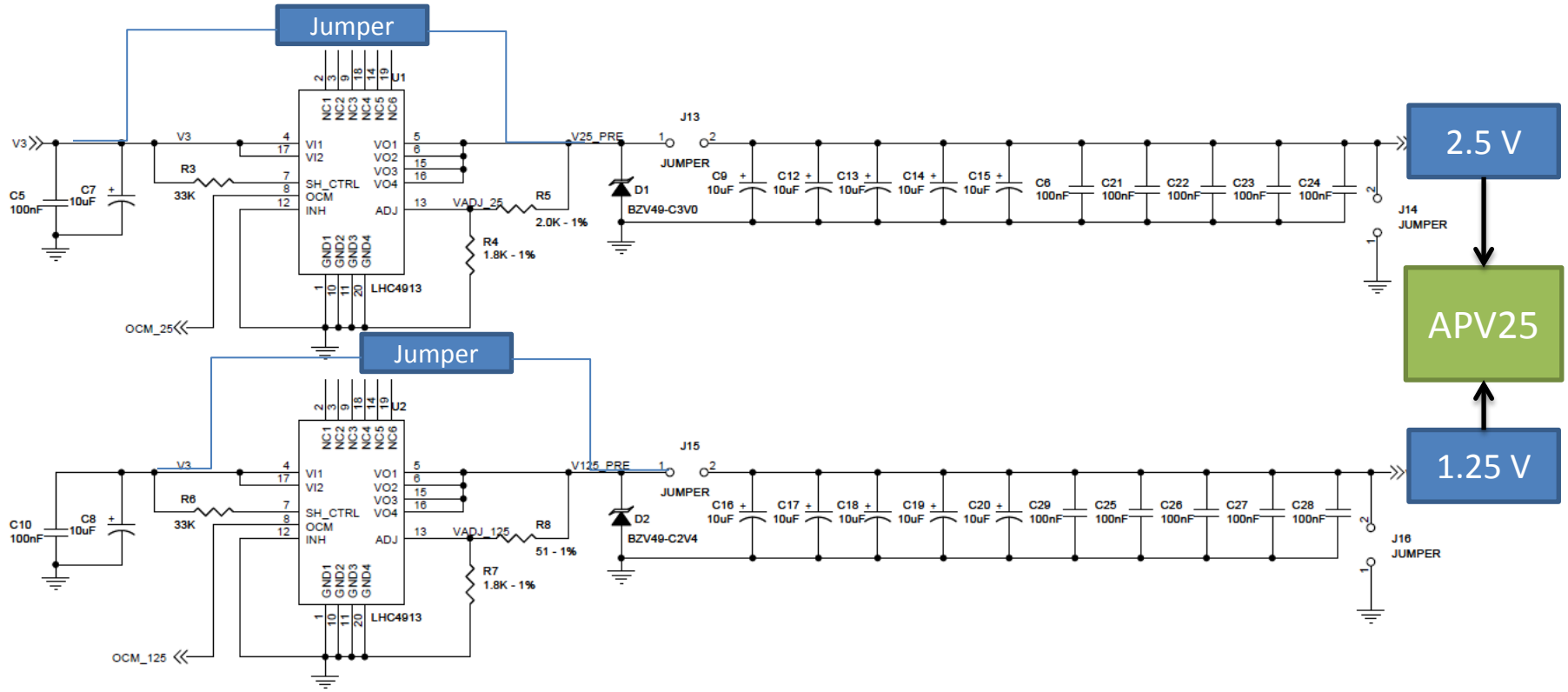
PCB Y pronto per la realizzazione del disegno finale in officina elettronica della Sezione con seguente realizzazione delle schede!!!

PCB Flessibile in Kapton

Back-Plane APV25



Regolatori di Tensione del Back Plane



Opportunità di:

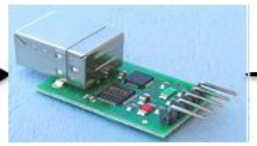
- Usare i regolatori di tensione sul Back-Plane

- Usare i regolatori di tensione sulla scheda APV25 (Solo test di Laboratorio)

- Usare il generatore di tensione per andare direttamente alle schede APV25

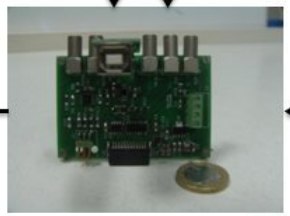
Setup per i test su APV25

PC



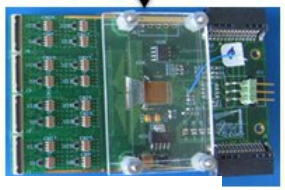
USB-I2C

Controller

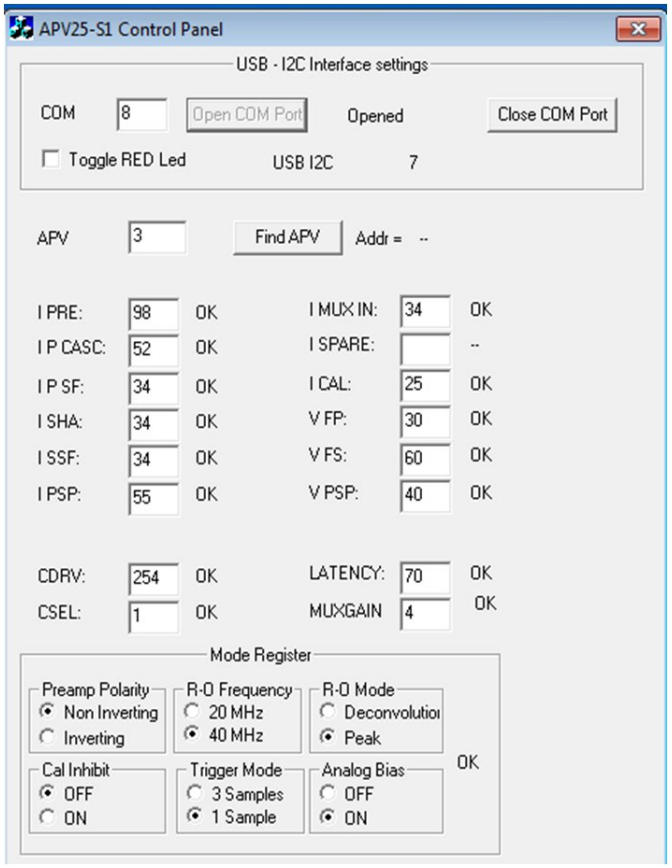


Test-Board

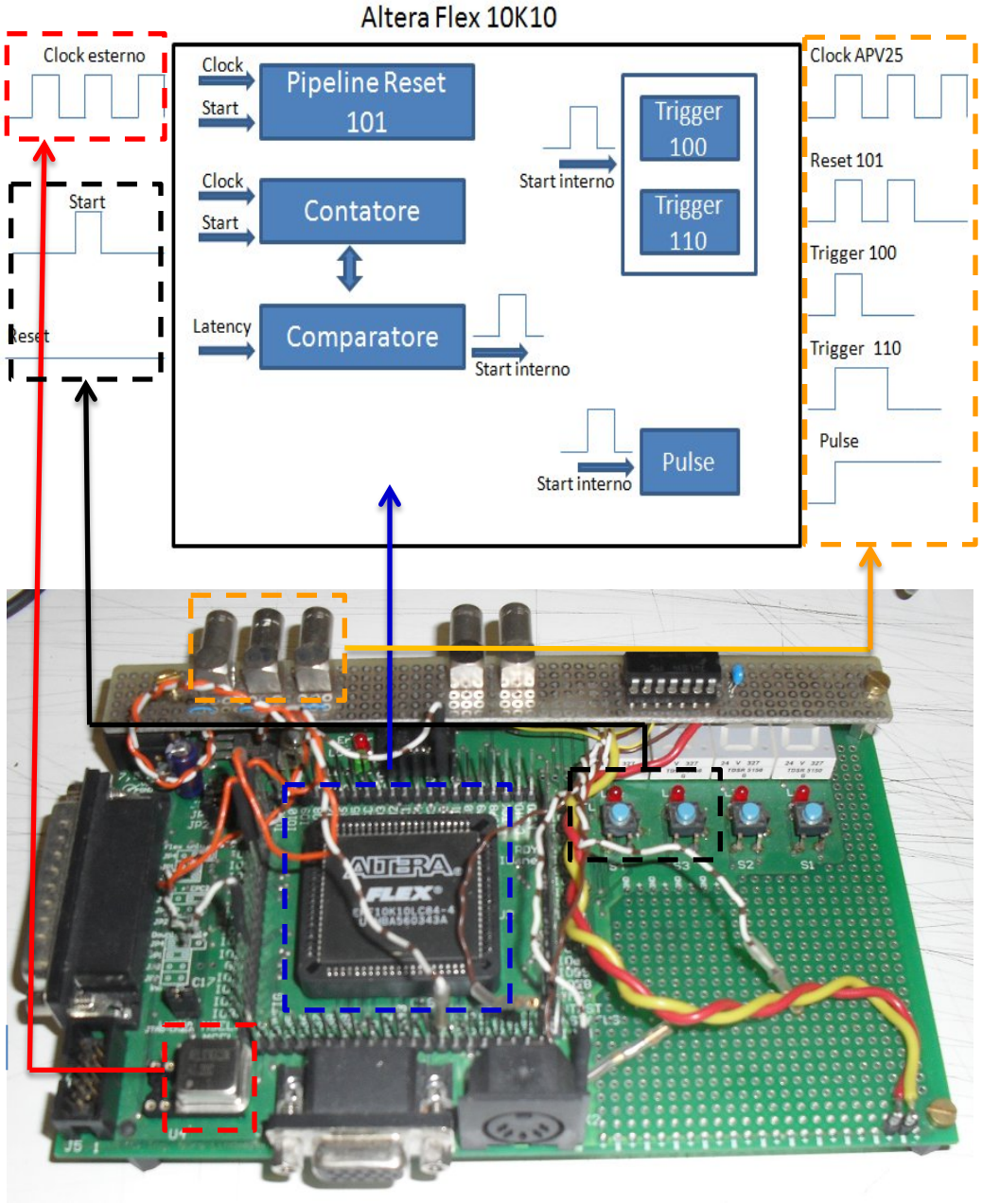
Agilent
MSO6032A



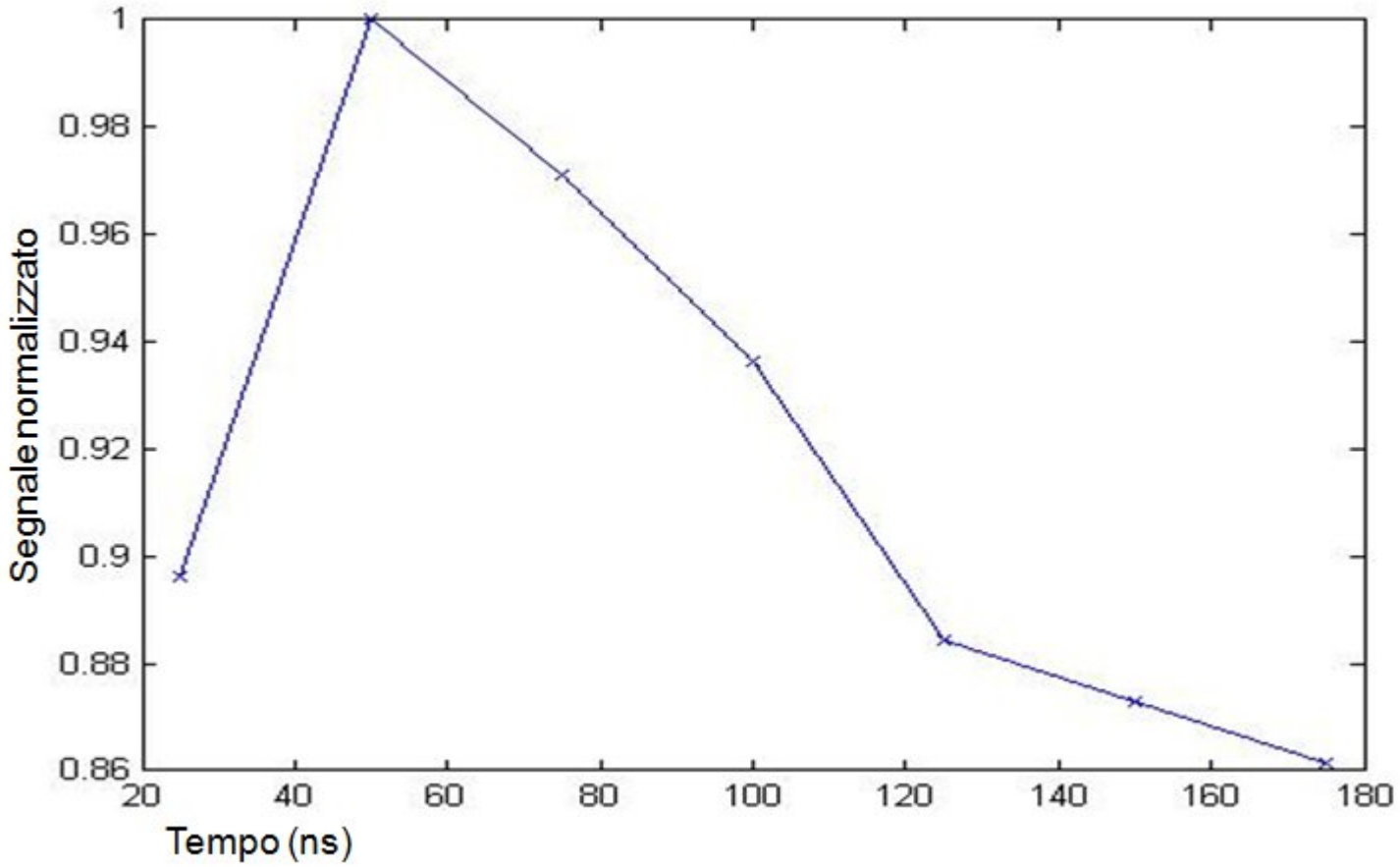
APV25



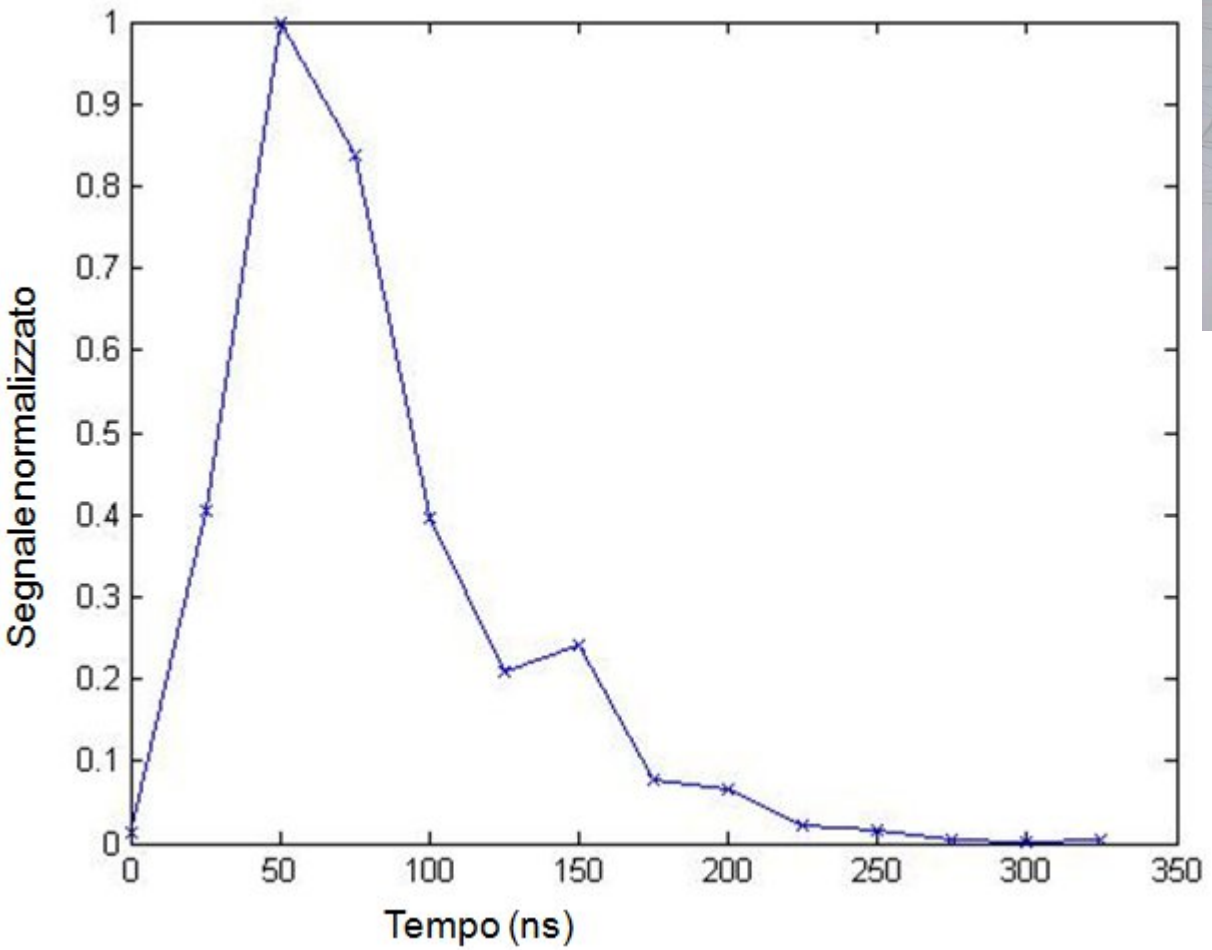
Controllore APV25

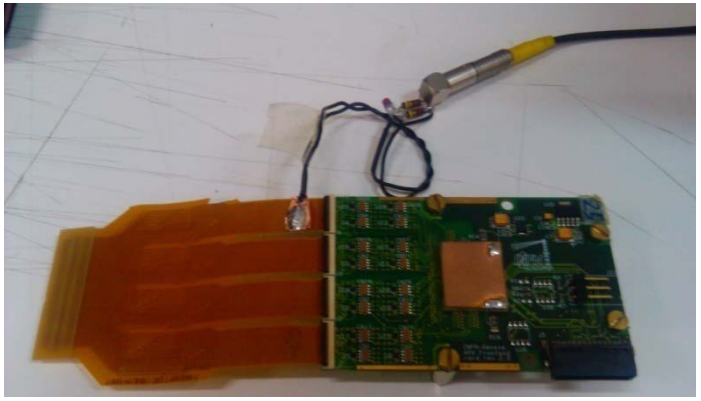


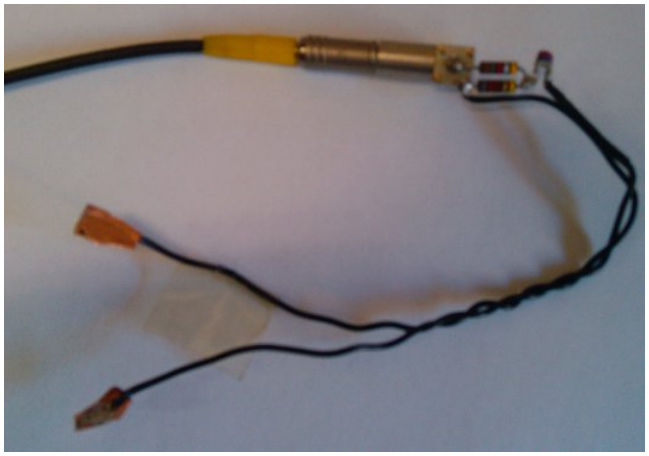
Ricostruzione del Segnale con autocalibrazione



Ricostruzione del Segnale Impulsaggio Esterno

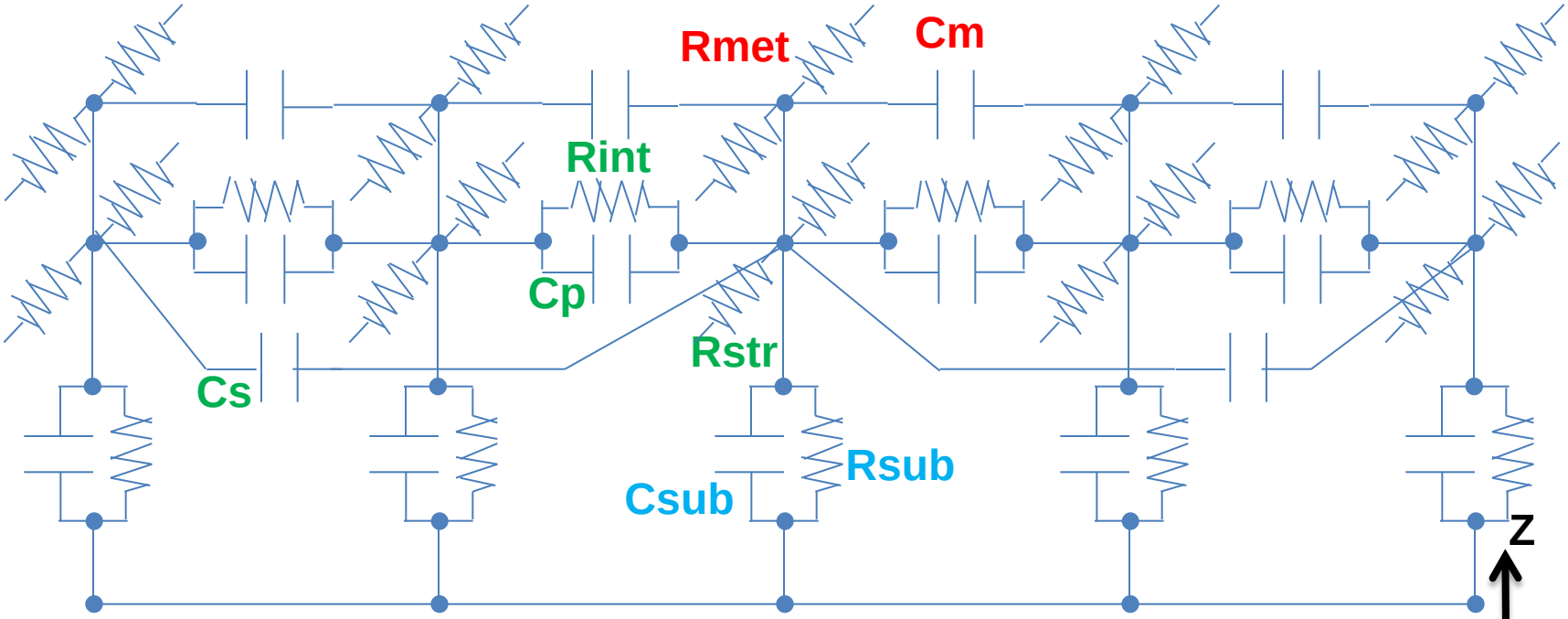






RISERVA

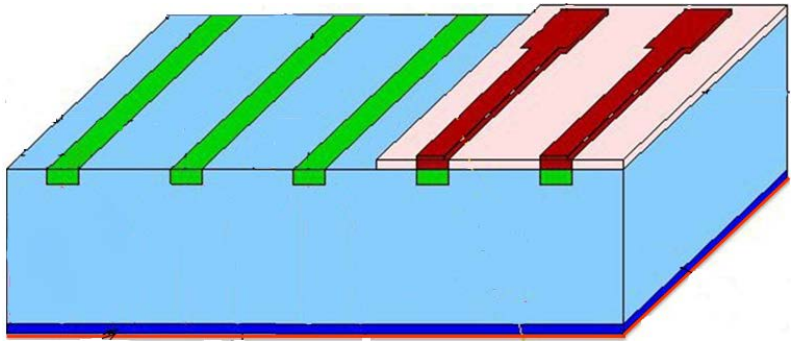
Modello Tridimensionale PSPICE 5 Strip



- **Modello del rivelatore**

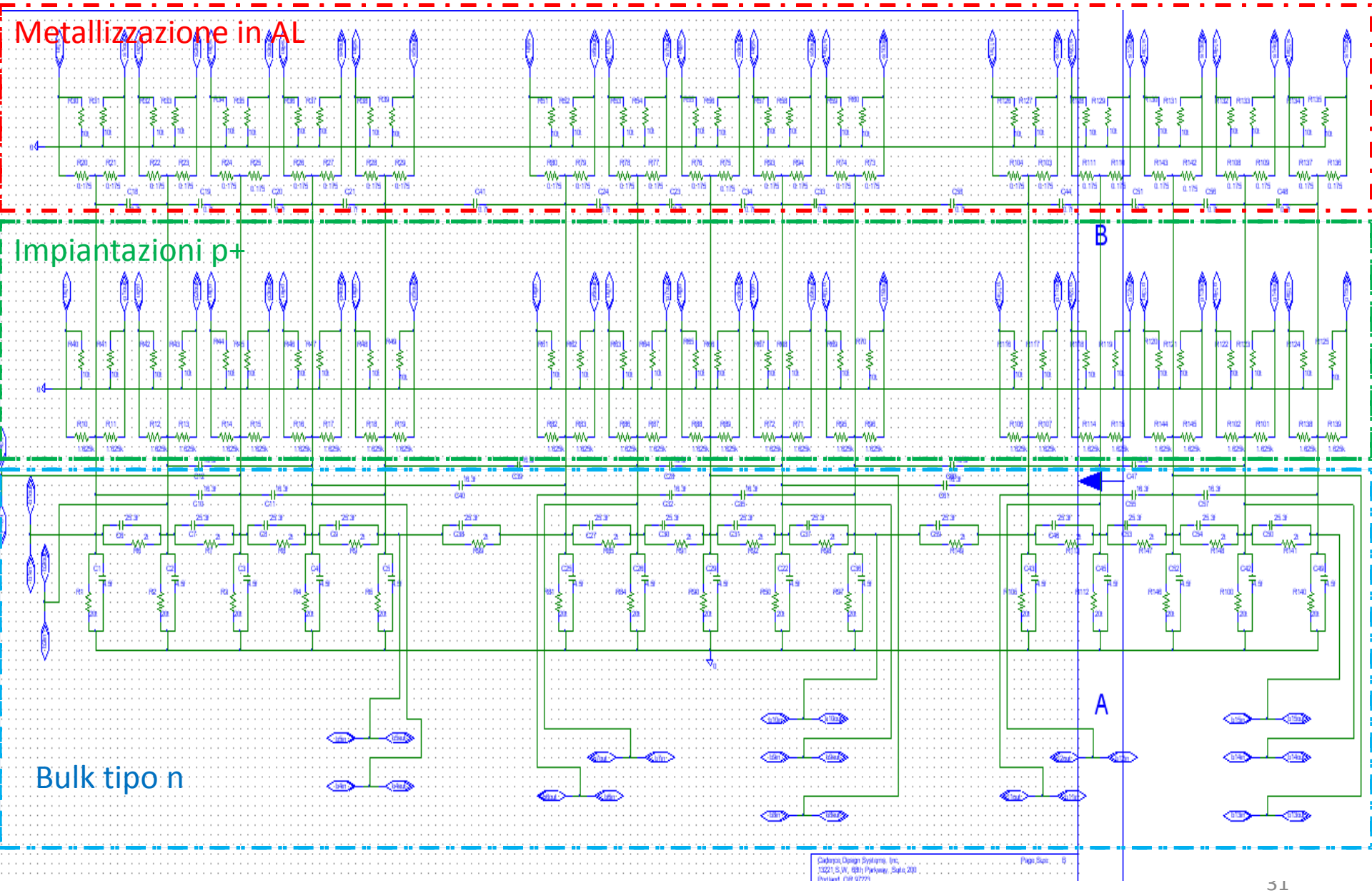
➔ **1 Cella: L_{strip} = 250 µm**

➔ **400 Celle: L_{strip} = 10 cm**

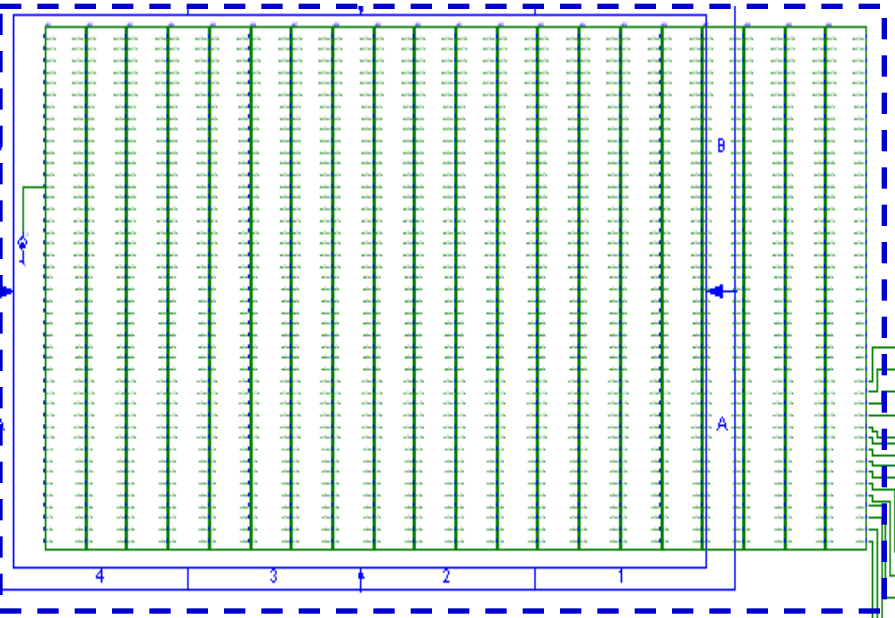


… modellizzazione finale estesa a 15 Strip

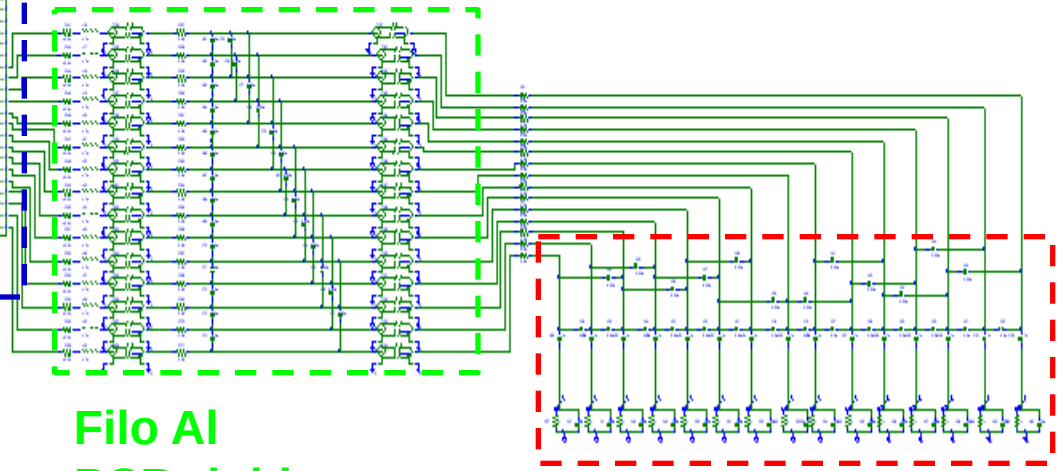
Modello PSPICE a 15 Strip



Simulazioni PCB rigido

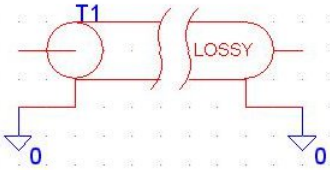


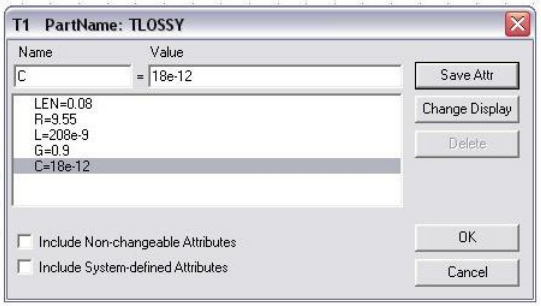
Rivelatore



Filo Al
PCB rigido
Connettore P5KS
PCB Kapton

Connettore ZIF
Ingresso APV25





R (Ω)	C (pF)	L (nH)	G (S)	Crosstalk (%)
9.55	122	401	0.02	0.1
9.55	20	761	2.6	9.5

Saldatrice ad ultrasuoni KS4526 e Microscopio Leica APO Z16