RDO Full/LpGBT model considerations

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ALCOR-RDO-DAM system (small) recap

ALCOR:

- ALCOR64 produces timestamps for **64 SiPMs**.
- The digital system is composed of **8 lanes serving 8 SiPM each**.
- **EIC mode**: ALCOR64 **sampling frequency 394 MHz**=4x98.5 MHz (bunch crossing frequency).
- Rollover time range: ~12 us → unordered datastream to the RDO.

RDO:

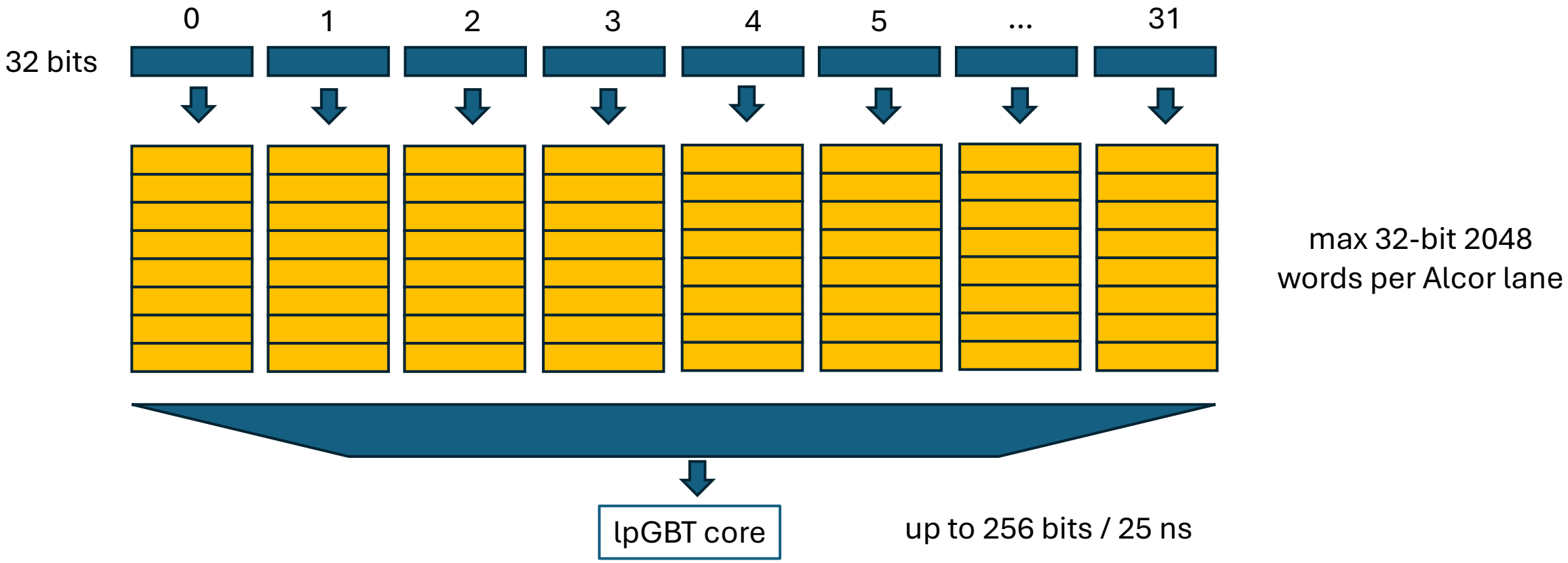
- RDO allows to **configure via SPI**, **read** and also **align** the ALCOR chips
- RDO reads **4 ALCOR64s** (4chips x 8lanes = **32 differential data lines** → RDO FIFO buffers)
- **VTRx+**: 10.24 Gb/s Uplink and 2.56 Gb/s Downlink
- Clock reconstruction + other chips control and configuration via I2C.

DAM:

- **LINK to GTU for CLOCK source (Rev tick, ecc..) to the RDO**
- Data buffering from the RDO + Data reduction using ML
- Each DAM serves up to **42 RDO links**

XCAU15P RAM resources

BRAM: 5.1 Mbits
distributed RAM: 2.5 Mbits



max 32-bit 2048 words per Alcor lane

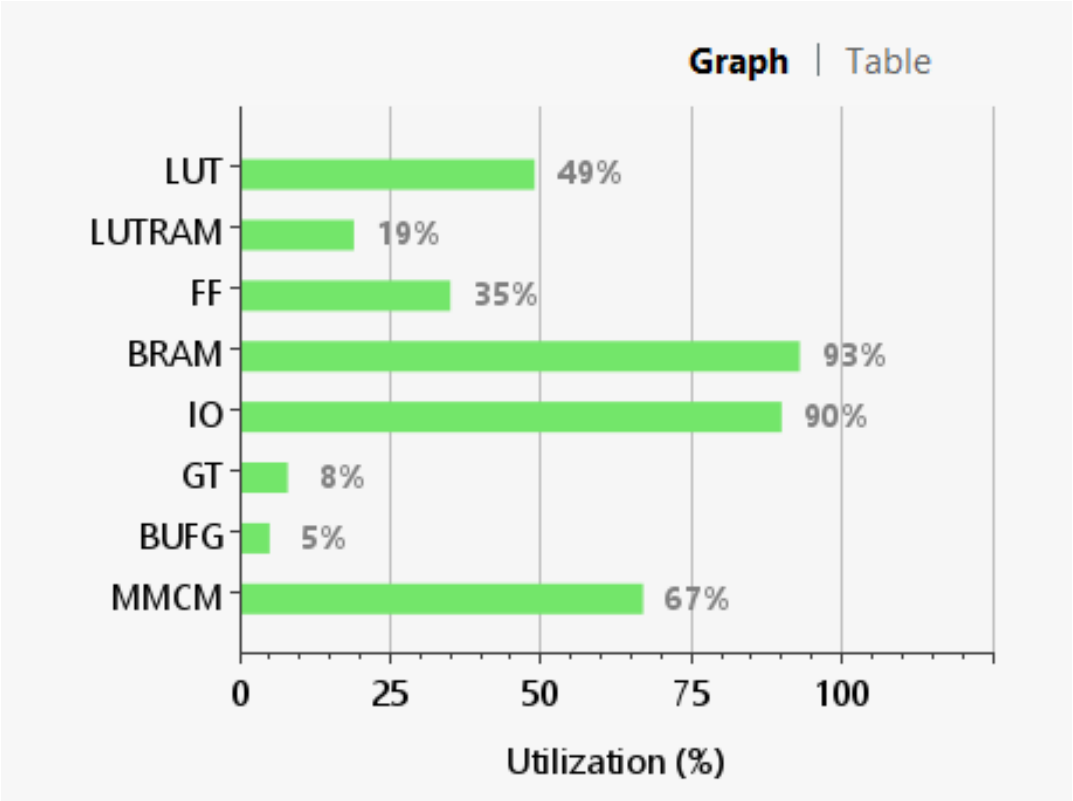
lpGBT / FULL core

payload	FEC12:	96 bits/BC	5.12 Gbps
	FEC5:	112 bits/BC	
	FEC12:	192 bits/BC	10.24 Gbps
	FEC5:	224 bits/BC	

payload	FULL:	256 bits/BC	10.24 Gbps

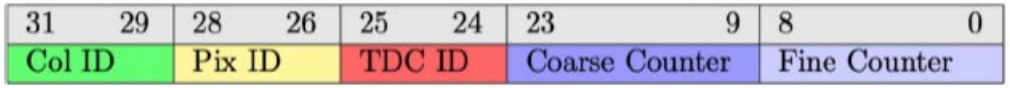
Current situation with IPbus

Beam test firmware resources:



ALCOR lane throughput

ALCOR data format



- **CTRL word frequency**: 0.6 kHz = 16 ctrlWord x Rollover frequency
- EIC Collision rate: ~500 kHz
- DCR: 3-300 kHz

Considering a **full lane firing** :
8.0 MHz = 500 kHz x 8 SiPMs x 2 words

Considering a **full lane DCR** :
4.8 MHz = 300 kHz x 8 SiPMs x 2 words

Lane MAX word rate
(500 kHz estimated)
8 MHz

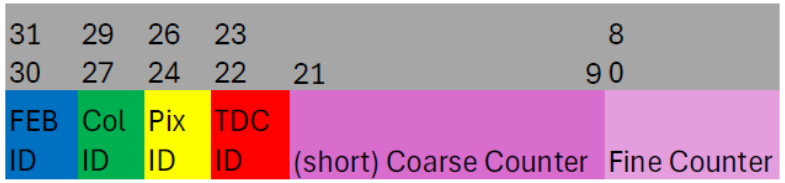
ALCOR MAX word rate
(500 kHz estimated)
64 MHz

RDO Readout models:

e-link

WORST DCR case: **300 KHz**
ALCOR possible latency: **128 clock cycles**
ALCOR SR mode
Uplink payload bandwidth: **8.96 Gb/s** (FEC5)

No data reduction:



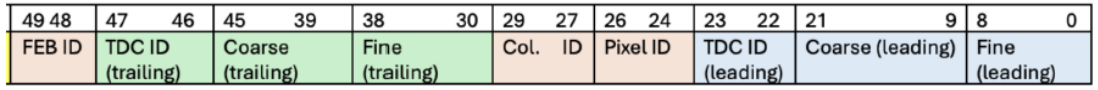
Thoughts on mapping DAQ dataflows on eLinks (2) – No data reduction

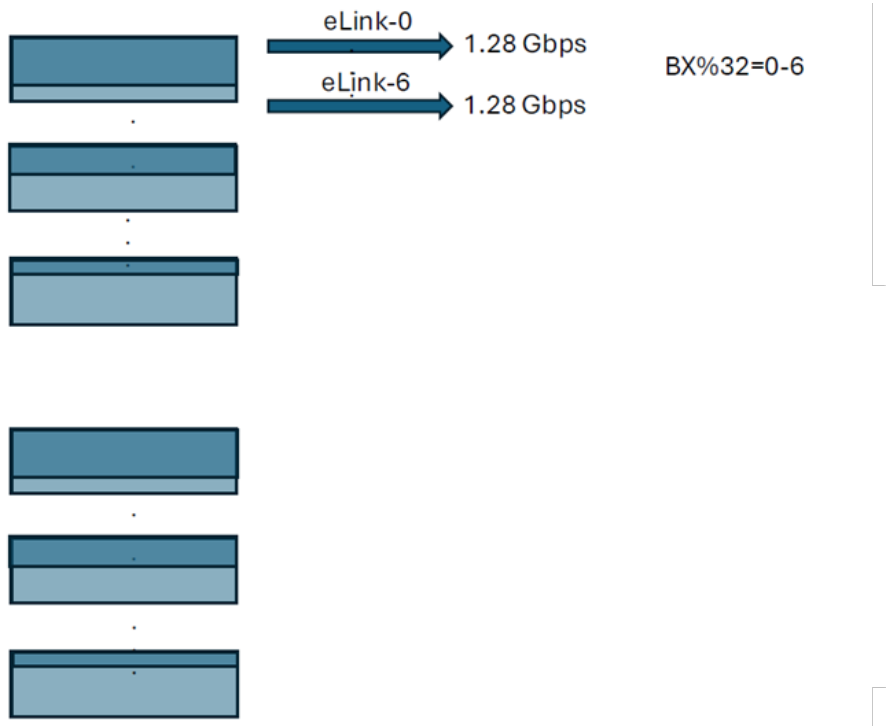
1.Direct Mapping (24 channels):
1. The first 24 ALCOR column streams (e.g., from FEB 0, 1, and 2) are mapped directly, one-to-one, to **eLinks 0 through 23**.
2. FEB 0, Col 0 -> eLink 0
3. ...
4. FEB 2, Col 7 -> eLink 23

2.Multiplexed Mapping (8 sources into 4 channels):
1. The remaining 8 ALCOR column streams (all from FEB 3) must be merged in pairs to be sent over the final 4 eLinks.
2. The RDO's FPGA will need logic to interleave or combine the data from two input streams into one output stream.
3. FEB 3, Col 0 + Col 1 -> eLink 24
4. FEB 3, Col 2 + Col 3 -> eLink 25
5. FEB 3, Col 4 + Col 5 -> eLink 26
6. FEB 3, Col 6 + Col 7 -> eLink 27

- Requisites for RDO firmware
  - Some little processing to ALCOR data format (shrink coarse counter, prepend FEB ID)
  - The FPGA firmware needs a **multiplexer (MUX)** block. This logic takes two 160 Mbps input streams (**assuming the 320 Mbps eLink bandwidth is sufficient for two merged streams**) and outputs a single 320 Mbps stream.

With data reduction:





RDO Readout models (1):

WORST DCR case: **300 KHz**
ALCOR possible latency: **128 clock cycles**
ALCOR SR mode
Uplink payload bandwidth: **8.96 Gb/s** (FEC5)

NO e-link

Hybrid model:

50	49 48	47 46	45 39	38 30	29 27	26 24	23 22	21 9	8 0
K CODE FLAG	FEB ID	TDC ID (trailing)	Coarse (trailing)	Fine (trailing)	Col. ID	Pixel ID	TDC ID (leading)	Coarse (leading)	Fine (leading)

AWORD (Alcor Word)

255	254	253	252	251 204	203 153	152 102	101 51	50 0
DATA FLAG FEB 3	DATA FLAG FEB 2	DATA FLAG FEB 1	DATA FLAG FEB 0	FREE FOR DCS	AWORD3 FEB 3	AWORD2 FEB 2	AWORD1 FEB 1	AWORD0 FEB 0

- this scheme could allow for lpGBT in hybrid mode so with FEC5 or FEC12
- push data from each FEB
- potentially we can send less bits (FEB ID is positional) but DAM should add it then

RDO Readout models alternatives:

NO e-link

aword

50	49 48	47 46	45 39	38 30	29 27	26 24	23 22	21 9	8 0
K CODE FLAG	FEB ID	TDC ID (trailing)	Coarse (trailing)	Fine (trailing)	Col. ID	Pixel ID	TDC ID (leading)	Coarse (leading)	Fine (leading)

255	254	253	252	251 204	203 153	152 102	101 51	50 0
DATA FLAG FEB 3	DATA FLAG FEB 2	DATA FLAG FEB 1	DATA FLAG FEB 0	FREE FOR DCS	AWORD3 FEB 3	AWORD2 FEB 2	AWORD1 FEB 1	AWORD0 FEB 0

aword aword aword aword

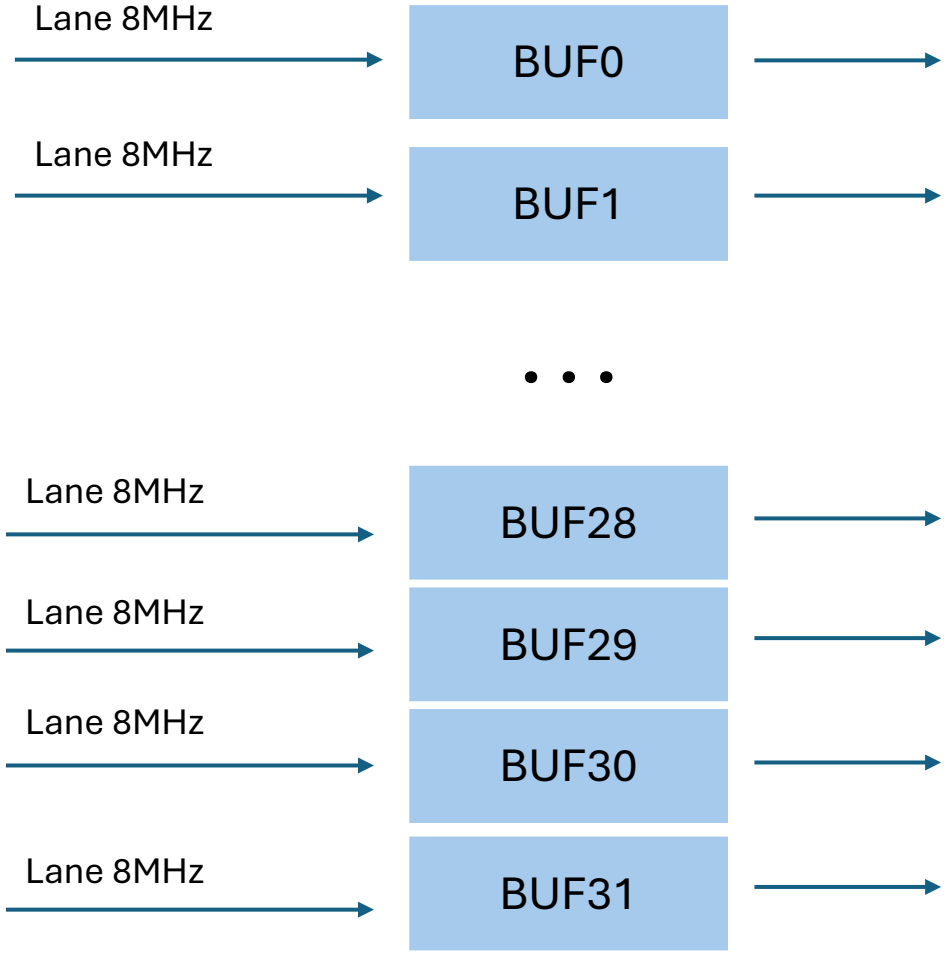
from any FEB#

RDO buffering stage

(Data reduction):

WORST DCR case: **300 KHz**
ALCOR possible latency: **128 clock cycles**
ALCOR SR mode
Uplink payload bandwidth: **8.96 Gb/s** (FEC5)

e-link



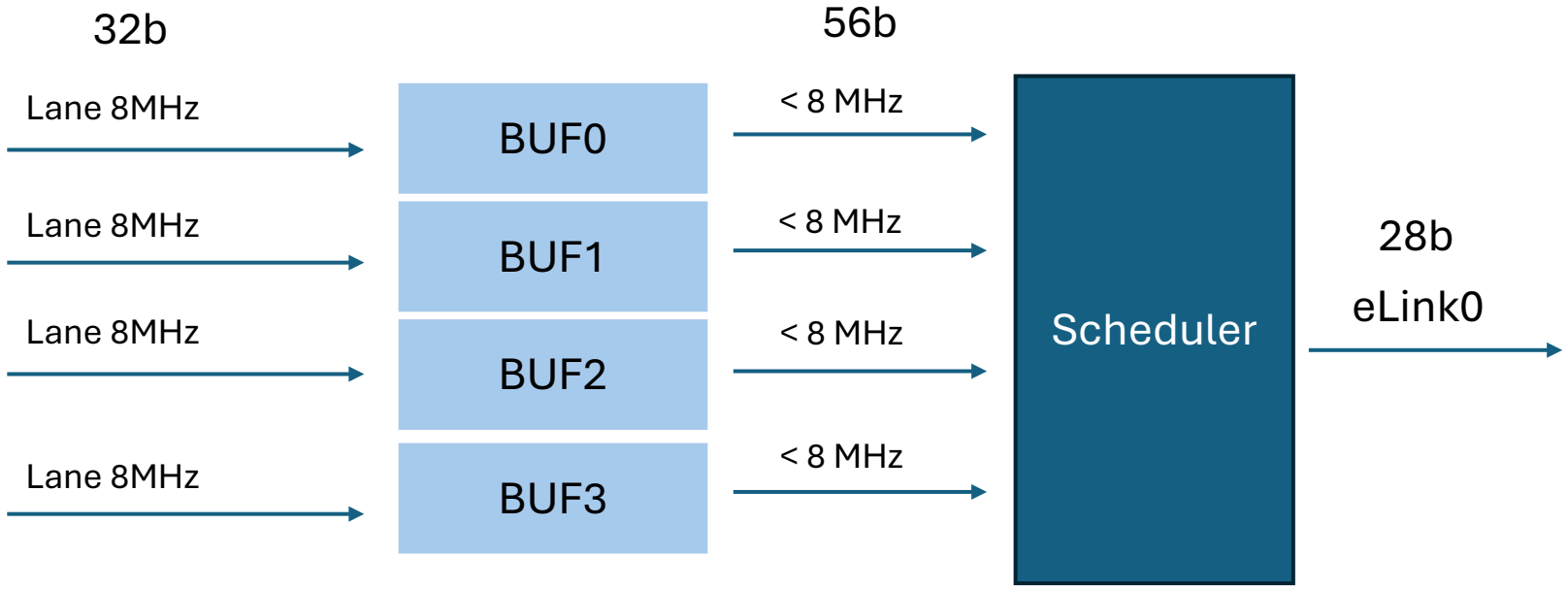
- BUF stage: each buffer waits for its falling edge data (possible latency 128 clock cycles) to generate the 51bit word (ctrl word sent directly).
- Scheduler with only 8 eLinks (64 MHz):
  - Sending early timestamps first.
  - Check all the FIFOs occupancy.

RDO buffering stage

(Data reduction):

WORST DCR case: **300 KHz**
ALCOR possible latency: **128 clock cycles**
ALCOR SR mode
Uplink payload bandwidth: **8.96 Gb/s** (FEC5)

e-link



Buffer of 512 words:

- 512 rising and 512 falling
- Rising edges waiting for falling ones

The **schedule**r includes:

- Buffer of 512 51b words
- Act on the occupancy and the timestamp to select the lane be read
- If half of the BUF is full, elements with only one word are sent as first object to the DAM
- A falling edge is directly sent to the DAM for evaluation

RDO buffering stage

(Hybrid model):

NO e-link

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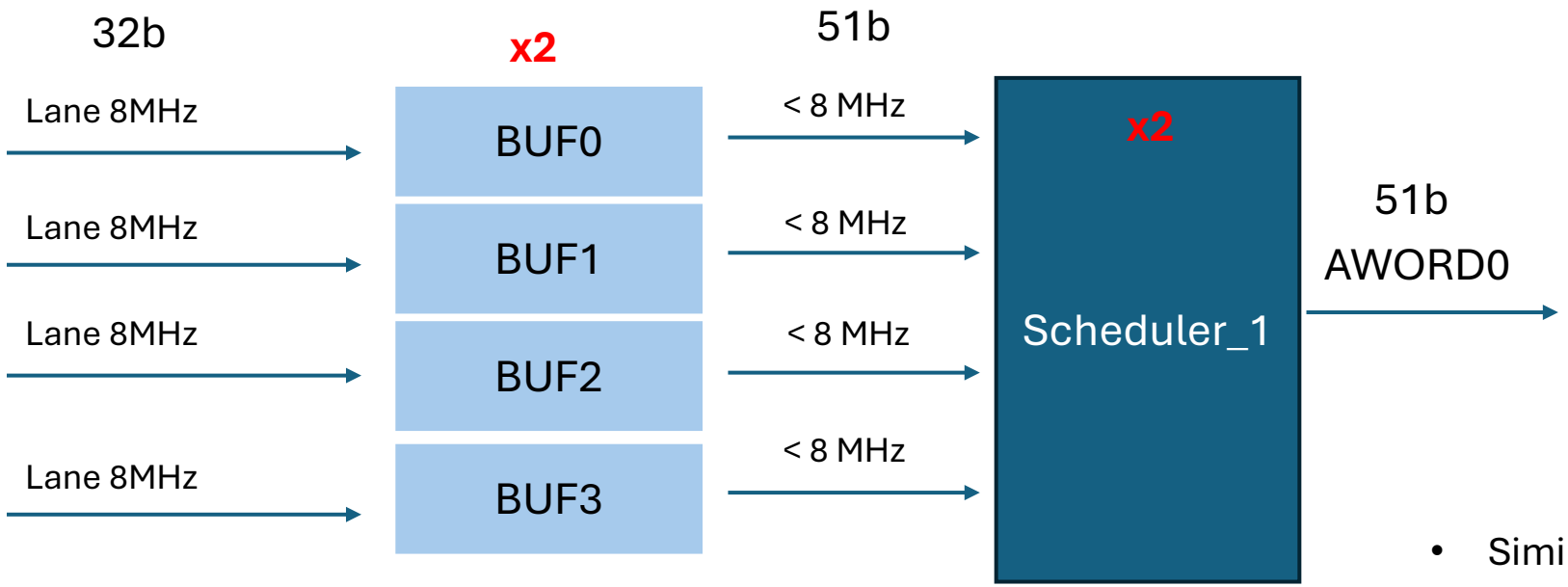
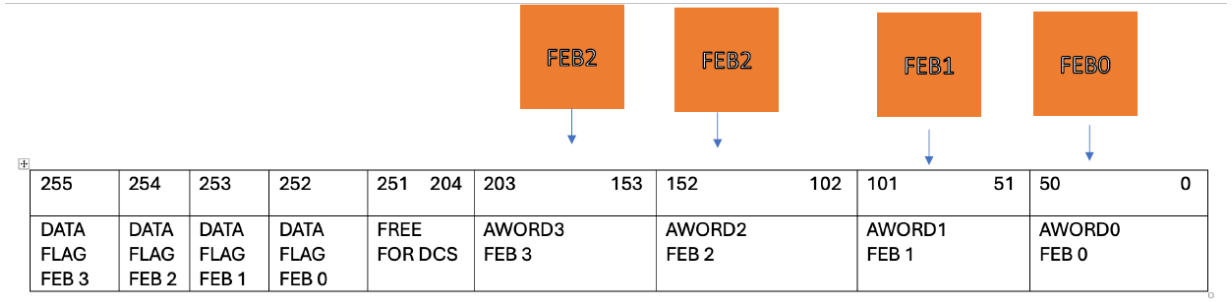
Uplink payload bandwidth: **8.96 Gb/s** (FEC5)





255	254	253	252	251 204	203 153	152 102	101 51	50 0
DATA FLAG FEB 3	DATA FLAG FEB 2	DATA FLAG FEB 1	DATA FLAG FEB 0	FREE FOR DCS	AWORD3 FEB 3	AWORD2 FEB 2	AWORD1 FEB 1	AWORD0 FEB 0

- Similar to the previous model.
- Segmentation for each FEB, BUT if some FEB is more noisy could be an issue
- Similar memory resources as DATA reduction.

Conclusions and Outlook

1. eLink vs NO eLink models need to be evaluated, we prefer to go without eLinks (also suggested by Filippo)

2. Simulations on the models are needed before taking a decision

3. We plan to implement a lpGBT FPGA core on the RDO to get some experience with this core