

dRICH Backend DAQ status update

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Summary of activities since last meeting

- Checked lpGBT flavour firmware versions on FLX-182
- Studied lpGBT protocol
- Some thoughts on how to map Alcor/FEB dataflow on eLinks
- Thoughts on requisites for RDO-DAM communication payload for the Data Reduction System on backend DAQ

lpGBT Firmware on FLX-182

- FLX182_LPGBT_12CH_LTICLK_GIT_phase2-master_rm-5.4_204_250925_1327 OK
- FLX182_LPGBT_16CH_LTICLK_GIT_phase2-release-5.3_rm-5.3_762_250531_1331 ?
 - Can't program FPGA, missing prj file (can't disable DDR calibration)

Instance	Module	Total LUTs	Logic LUTs	LUTRAMs	SRLs	FFs	RAMB36	RAMB18	URAM	DSP Blocks
felix_top	(top)	525065	512813	9156	3096	657519	400	776	294	0
xcvm1802		899840				1799680	612	1224	368	1968
% used		58,3509291				36,5353285	65,3594771	63,3986928	79,8913043	0

- FLX182_LPGBT_24CH_LTICLK_GIT_phase2-master_rm-5.4_204_250925_1327 NOT-OK



FLX182_LPGBT_12CH_LTICLK_GIT_phase2-master_rm-5.4_204_250925_1327

Project Summary

Overview | Dashboard

Status: ✔ Complete
Messages: ⚠ 3 critical warnings
⚠ 1124 warnings
Active run: [synth_1](#)
Part: xcv1802-vsva2197-1MP-e-S
Strategy: [Flow_AreaOptimized_high](#)
Report Strategy: [Vivado Synthesis Default Reports](#)
Incremental synthesis: [Automatically selected checkpoint](#)

Status: ✔ write_device_image Complete!
Messages: ⚠ 11 critical warnings
⚠ 3311 warnings
Active run: [impl_1](#)
Part: xcv1802-vsva2197-1MP-e-S
Strategy: [Performance_ExplorePostRoutePhysOpt](#)
Report Strategy: [Vivado Implementation Default Reports](#)
Incremental implementation: [None](#)

DRC Violations

Summary: ⚠ 7313 warnings
[Implemented DRC Report](#)

Timing

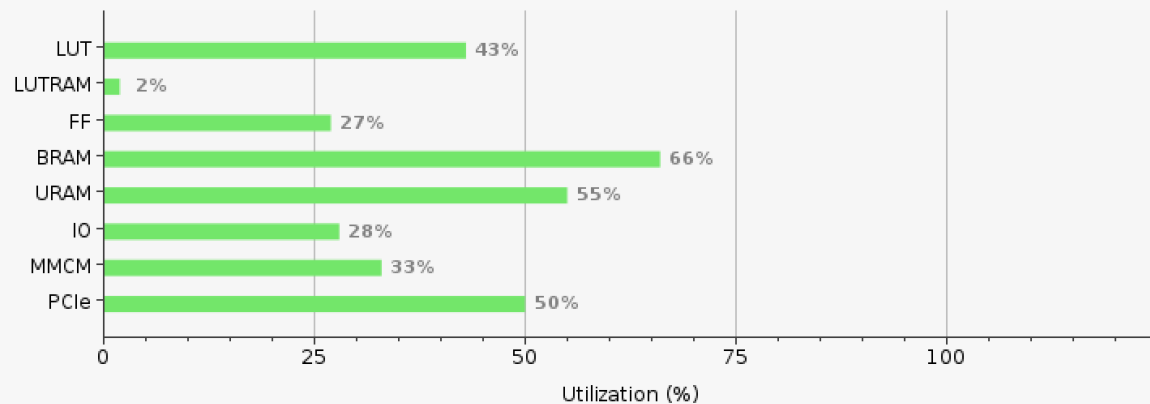
Setup | Hold | Pulse Width

Worst Negative Slack (WNS): -0.486 ns
Total Negative Slack (TNS): -250.613 ns
Number of Failing Endpoints: 2424
Total Number of Endpoints: 1180386
[Implemented Timing Report](#)

Utilization

Post-Synthesis | **Post-Implementation**

Graph | Table

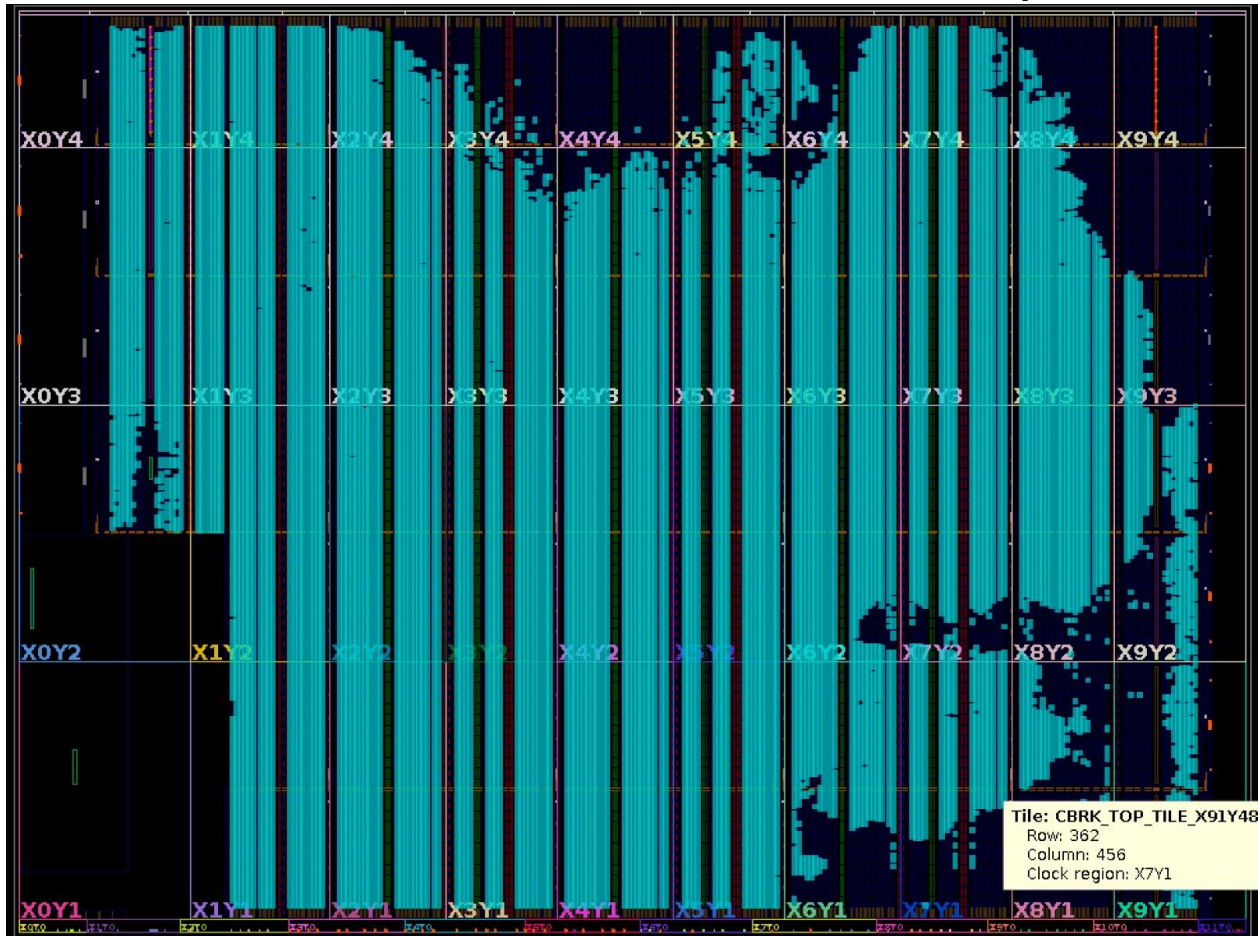


Power

Summary | On-Chip

Total On-Chip Power: 28.157 W
Junction Temperature: 100.0 °C
Thermal Margin: 0.0 °C (8.8 W)
Effective θ_{JA} : 2.7 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
[Implemented Power Report](#)

FLX182_LPGBT_12CH_LTICLK_GIT_phase2-master_rm-5.4_204_250925_1327



DRC | Methodology | Hard Block Planner | Power | **Timing** x

Design Timing Summary

Setup

Worst Negative Slack (WNS): -0.070 ns
Total Negative Slack (TNS): -0.214 ns
Number of Failing Endpoints: 5
Total Number of Endpoints: 1181070

Hold

Worst Hold Slack (WHS): 0.003 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 1010477

Pulse Width

Worst Pulse Width Slack (WPWS): 0.000 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 511407

Timing constraints are not met.

The **uplink transmit data from the lpGBT to the counting room**. The uplink data rate is programmable and can be either 5.12 Gb/s or 10.24 Gb/s. Additionally, two FEC codes can be used: FEC5 allowing to correct up to 5 consecutive wrong bits and FEC12 with a correction capacity of up to 12 bits. The effective data rate is thus determined by the selected data rate (5.12 or 10.24 Gb/s) and the FEC code used (FEC5 or FEC12)

- Transport of acquired data for off-detector processing, storage,

The **downlink transmits data from the counting room to the lpGBT**. The data is transmitted at 2.56 Gb/s in a 64-bit frame that are transmitted every 25 ns (the LHC bunch crossing period) :

- Timing distribution, detector control, trigger distribution

eLinks are associated with **ePorts** and **ePorts** are grouped in **eGroups**. Each **eGroup**, is composed of **4 ePorts**

- eLinks are “clustered” in groups of 4

The number of available groups is determined by the FEC uplink code in use;

- The number of available eLinks within a group is determined by the Group data rate;
- The possible data rates depend on the uplink bandwidth (5.12 or 10.24 Gbps)
- The data rate of each group can be set independently [es. 10.24@FEC5/FEC12 -> 320/640/1280 Mb/s]

- The data rate of each group can be set independently:
 - A couple of [over complicated] examples:
 - uplink 5.12 Gbps & FEC12: 8 eLinks x 160 Mbps + 4 eLinks x 320 Mbps + 2 eLinks x 640 Mbps
 - uplink 10.24 Gbps & FEC5: 8 eLinks x 320 Mbps + 4 eLinks x 640 Mbps + 3 eLinks x 1.28 Gbps

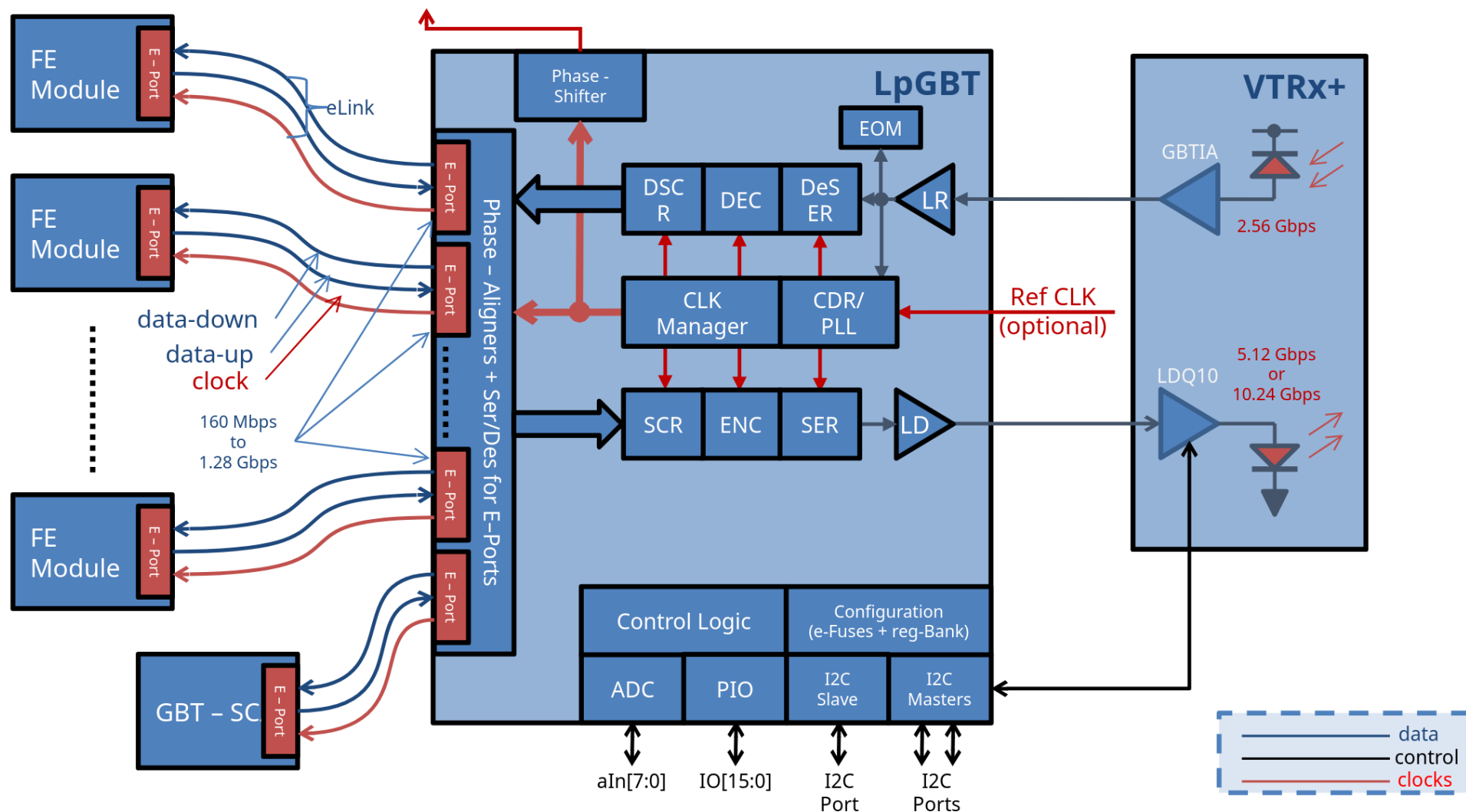
Input eLinks (uplink)												
uplink bandwidth [Gbps]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mbps]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

128bits @ 25 ns (40 MHz) -> 5.12 Gb/s
 256bits @ 25 ns (40 MHz) -> 10.24 Gb/s

Es. 10.24@FEC5 -> 7 *1280=8960 Mb/s max bw
 10.24@FEC12 -> 6 *1280=7680 Mb/s max bw

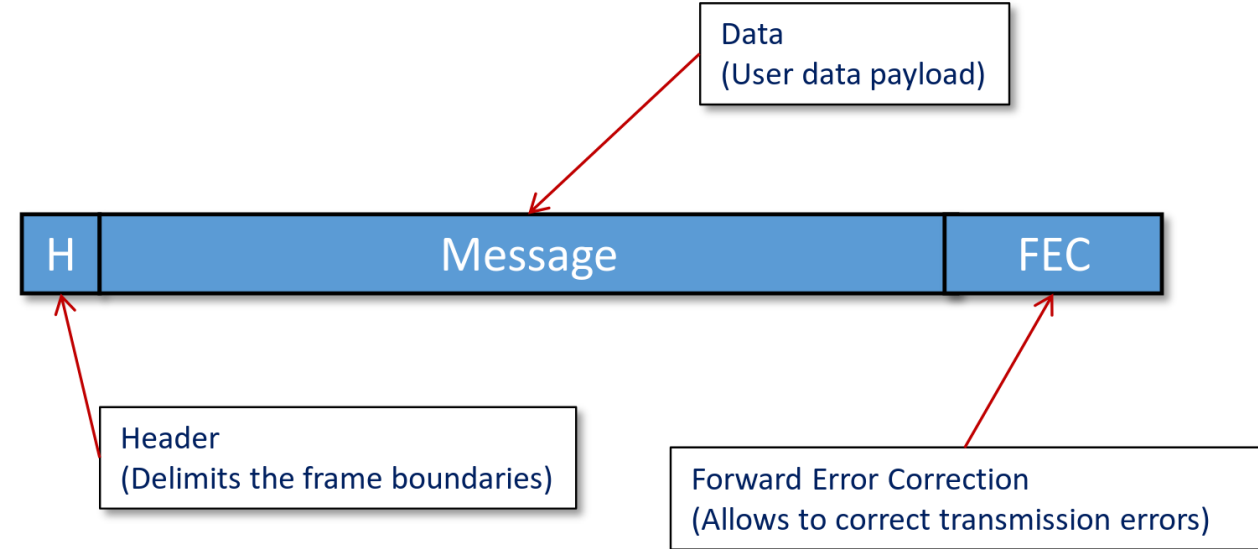
	uplink			
	5.12 Gbps		10.24 Gbps	
	FEC5	FEC12	FEC5	FEC12
Frame [bits]	128		256	
Header [bits]	2		2	
Data [bits]	116	102	232	204
FEC [bits]	10	24	20	48
Correction [bits]	5	12	10	24
Efficiency	91%	80%	91%	80%

IpGBT – Block Diagram Overview



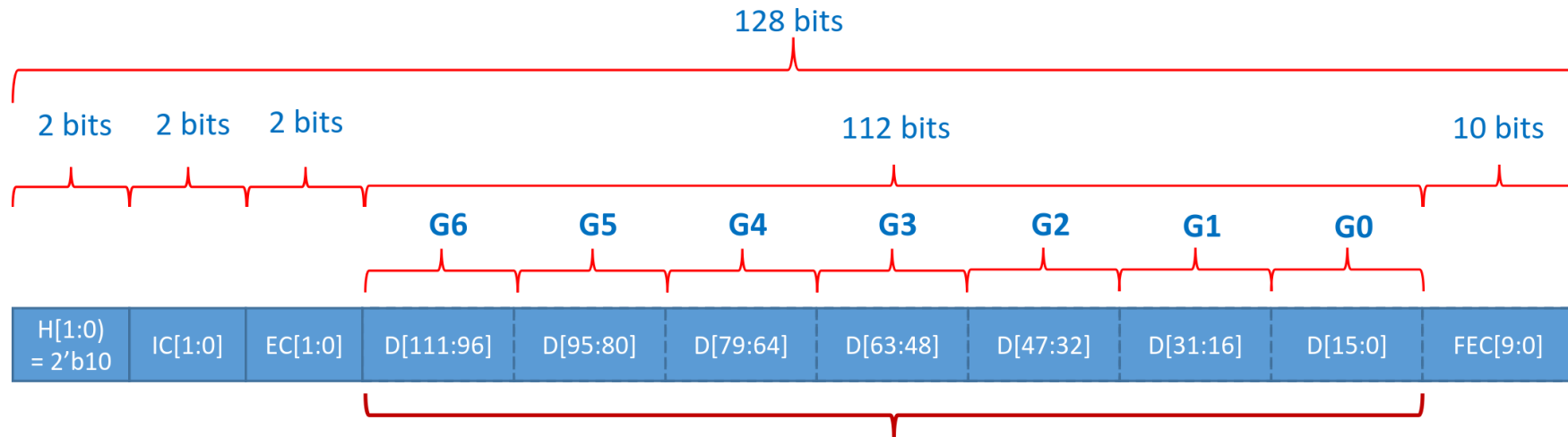
lpGBT: Data encoding

- The LpGBT supports the following data rates:
 - Down link: 2.56 Gb/s
 - Up-link: 5.12 / 10.24 Gb/s
- In all cases data is transmitted as a frame composed of:
 - Header
 - The data field
 - A forward error correction field: FEC5 / FEC12
- The data field is scrambled to allow for CDR at no [additional] bandwidth penalty
- Efficiency = # data bits/# frame bits



	Down-link 2.56 Gb/s	Up-Link			
		5.12 Gb/s		10.24 Gb/s	
		FEC5	FEC12	FEC5	FEC12
Frame [bits]	64	128		256	
Header [bits]	4	2		2	
Data [bits]	36	116	102	232	204
FEC [bits]	24	10	24	20	48
Correction [bits]	12	5	12	10	24
Efficiency	56%	91%	80%	91%	80%

Example: 5.12 Gbps FEC5 Uplink Frame



7 groups of 4 input e-Ports

Number of data ports:

- 28 eLinks @ 160 Mbps
- 14 eLinks @ 320 Mbps
- 7 eLinks @ 640 Mbps

Frame	Function	I/O Group
FRMUP[9:0]	FEC[9:0]	
FRMUP[25:10]	Data[15:0]	0
FRMUP[41:26]	Data[31:16]	1
FRMUP[57:42]	Data[47:32]	2
FRMUP[73:58]	Data[63:48]	3
FRMUP[89:74]	Data[79:64]	4
FRMUP[105:90]	Data[95:80]	5
FRMUP[121:106]	Data[111:96]	6
FRMUP[123:122]	EC[1:0]	EC
FRMUP[125:124]	IC[1:0]	
FRMUP[127:126]	H[1:0] = 2'b10	HFH[1:0] = 2'b10

Note: This is how you will see the uplink frame after it has been processed by the IpGBT-FPGA receiver but not how it is actually transmitted by the IpGBT ...

Uplink – FEC 5

- Dual data rate:
 - 5.12 Gb/s
 - 10.24 Gb/s
- Frame:
 - Header:
 - 2 / 4 – bits
 - 2'b10 (high) & 2'b01 (low)
 - IC field:
 - 2 – bit
 - 80 Mb/s
 - EC field:
 - 2 – bit
 - 80 Mb/s
 - Data field:
 - 112 / 224 – bit
 - 4.48 / 8.96 Gb/s
 - FEC field:
 - 10 / 20 – bit
- Error correction:
 - FEC:
 - Interleaving: 1 / 2
 - Symbol width: 5 – bit
 - Number of wrong symbols: 1 (× 1 / × 2)
 - Up to 5 / 10 consecutive bits
 - Efficiency: 91%
- eLinks:
 - Data
 - 28 eLinks @ 160 / 320 Mb/s
 - 14 eLinks @ 320 / 640 Mb/s
 - 7 eLinks @ 640 / 1280 Mb/s
 - EC
 - 1 eLink @ 80 Mb/s

FEC5		
	5.12 Gb/s	10.24 Gb/s
Option	7	7
Frame (bits)	128	2 x 128
Header (bits)	2	2+2
Coded header	no	no
User field (bits)	116	232
Code (bits)	10	20
16-bit multiplicity	7.250	14.5
Remainder bits	4	8
User Bandwidth (GHz)	4.64	9.28
# eLinks groups (16 bit)	7	7
eLinks bandwidth (MHz)	160/320/640	320/640/1280
#eLinks	28/14/7	28/14/7
EC bandwidth (MHz)	80	80/160
IC bandwidth (MHz)	80	80/160
Unassigned bits	0	4
Corrected (bits)	5	2 x 5
Efficiency	91%	91%

Uplink – FEC 12

- Dual data rate:
 - 5.12 Gb/s
 - 10.24 Gb/s
- Frame:
 - Header:
 - 2 / 4 – bits
 - 10 (high) & 01 (low)
 - IC field:
 - 2 – bit
 - 80 Mb/s
 - EC field:
 - 2 – bit
 - 80 Mb/s
 - Data field:
 - 96 / 192 – bit
 - 3.84 / 7.68 Gb/s
 - FEC field:
 - 24 / 48 – bit
- Error correction:
 - FEC:
 - Interleaving: 3 / 6
 - Symbol width: 4 – bit
 - Number of wrong symbols: 1 (× 3 / × 6)
 - Up to 12 / 24 consecutive bits
 - Efficiency: 78% (if accounting for the unassigned bits)
- eLinks:
 - Data
 - 24 eLinks @ 160 / 320 Mb/s
 - 12 eLinks @ 320 / 640 Mb/s
 - 6 eLinks @ 640 / 1280 Mb/s
 - EC
 - 1 eLink @ 80 Mb/s

FEC12

	5.12 Gb/s	10.24 Gb/s
Option	28	28
Frame (bits)	128	2 x 128
Header (bits)	2	2+2
Coded header	no	no
User field (bits)	102	204
Code (bits)	24	48
16-bit multiplicity	6.375	12.75
Remainder bits	6	12
User Bandwidth (GHz)	4.08	8.16
# eLinks groups (16 bit)	6	6
eLinks bandwidth (MHz)	160/320/640	320/640/1280
#eLinks	24/12/6	24/12/6
EC bandwidth (MHz)	80	80/160
IC bandwidth (MHz)	80	80/160
Unassigned bits	2	8
Corrected (bits)	12	2 x 12
Efficiency	80%	80%

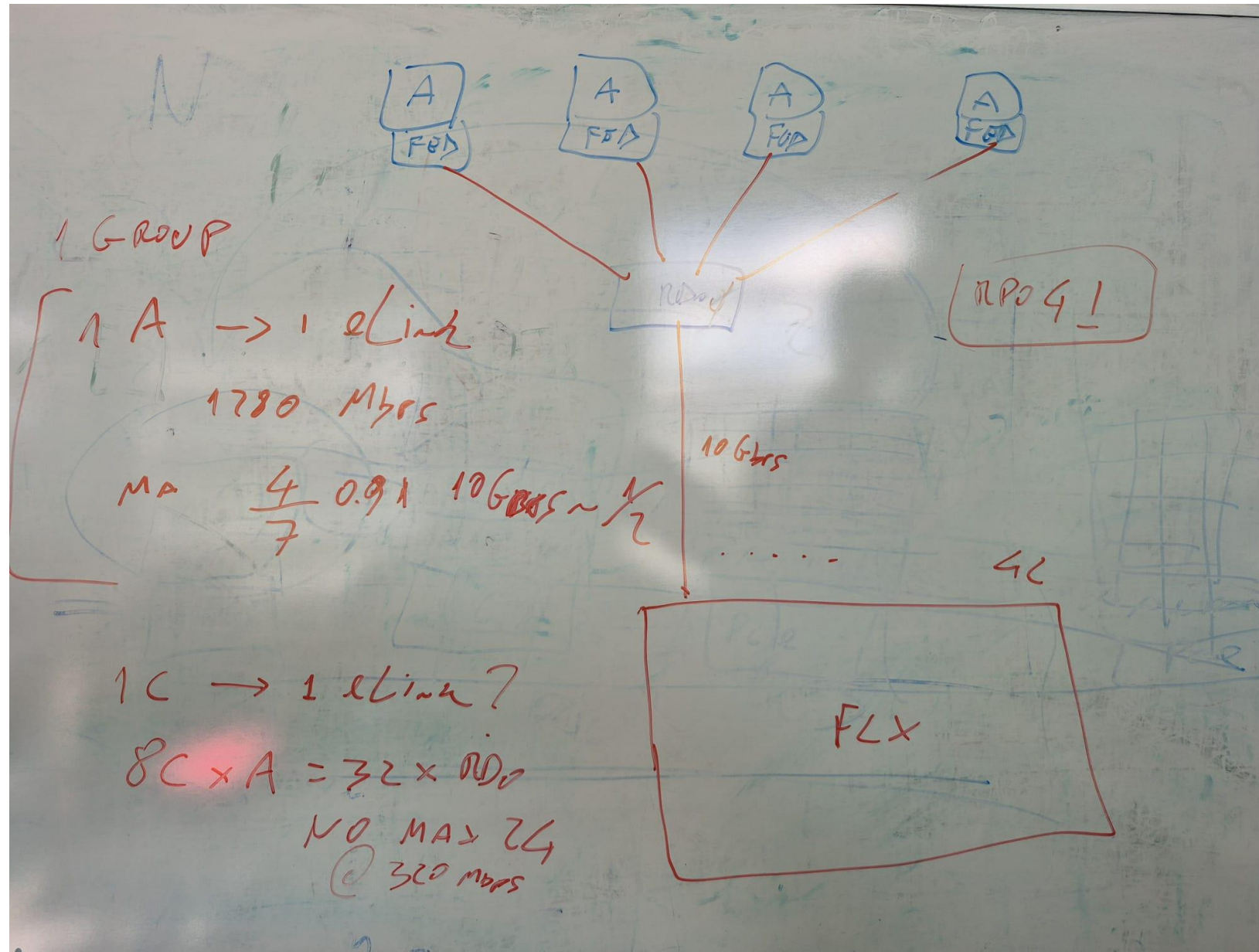
The FELIX firmware has two main flavours or modes, known as GBT [old version] and FULL:

- Both modes use the GBT protocol for the links towards the FE and support up to 24 links
- The GBT mode uses the GBT protocol to receive data from the FE
- BUT the FULL mode implements a light-weight protocol for this path, with a bandwidth of 9.6 Gb/s per optical link which accounting for 8b10b encoding means a maximum user payload of 7.68 Gb/s.
- FULL mode is intended for communication with other FPGA-based systems over the custom 8b/10b encoded protocol implemented as a single wide data stream with no handshaking or logical substructure (i.e. no E-links).

Example: ATLAS Liquid Argon Digital Processing Blade and L1Calo trigger systems use FELIX in FULL mode

- L1Calo uses a feature called streams: each of the 16 FULL mode links in use carries up to 9 streams, each transmitting messages at a rate of 100 kHz
- The New Small Wheel muon detector uses FELIX in GBT mode. Each FELIX card serves up to 200 E-links, each transmitting messages at the L1 trigger rate (100KHz?). The average size of a NSW message is 40B

Thoughts on mapping DAQ dataflows on eLinks



No data reduction: data format

- 128 clock cycles max spread in same event hits are NOT a problem
- 2 words for hit are NOT a problem (well...it depends on max rate...)

31	29	28	26	25	24	23	9	8	0
Col ID	Pix ID	TDC ID	Coarse Counter	Fine Counter					

ALCOR BUS

31	29	26	23			8
30	27	24	22	21		9 0
FEB	Col	Pix	TDC	(short) Coarse Counter		Fine Counter
ID	ID	ID	ID			

RDO to DAM

Thoughts on mapping DAQ dataflows on eLinks (2) – No data reduction

1. Direct Mapping (24 channels):

1. The first 24 ALCOR column streams (e.g., from FEB 0, 1, and 2) are mapped directly, one-to-one, to **eLinks 0 through 23**.
2. FEB 0, Col 0 -> eLink 0
3. ...
4. FEB 2, Col 7 -> eLink 23

2. Multiplexed Mapping (8 sources into 4 channels):

1. The remaining 8 ALCOR column streams (all from FEB 3) must be merged in pairs to be sent over the final 4 eLinks.
2. The RDO's FPGA will need logic to interleave or combine the data from two input streams into one output stream.
3. FEB 3, Col 0 + Col 1 -> eLink 24
4. FEB 3, Col 2 + Col 3 -> eLink 25
5. FEB 3, Col 4 + Col 5 -> eLink 26
6. FEB 3, Col 6 + Col 7 -> eLink 27

- Requisites for RDO firmware
 - Some little processing to ALCOR data format (shrink coarse counter, prepend FEB ID)
 - The FPGA firmware needs a **multiplexer (MUX)** block. This logic takes two 160 Mbps input streams (**assuming the 320 Mbps eLink bandwidth is sufficient for two merged streams**) and outputs a single 320 Mbps stream.

Data reduction: data format

- 128 clock cycles max spread in same event hits ARE a problem
- 2 words for hit ARE a problem
- SOLUTION(?): buffer 32 BX on RDO, then send to DAM

31	29	28	26	25	24	23	9	8	0
Col ID	Pix ID	TDC ID	Coarse Counter	Fine Counter					

31	29	28	26	25	24	23	9	8	0
Col ID	Pix ID	TDC ID	Coarse Counter	Fine Counter					

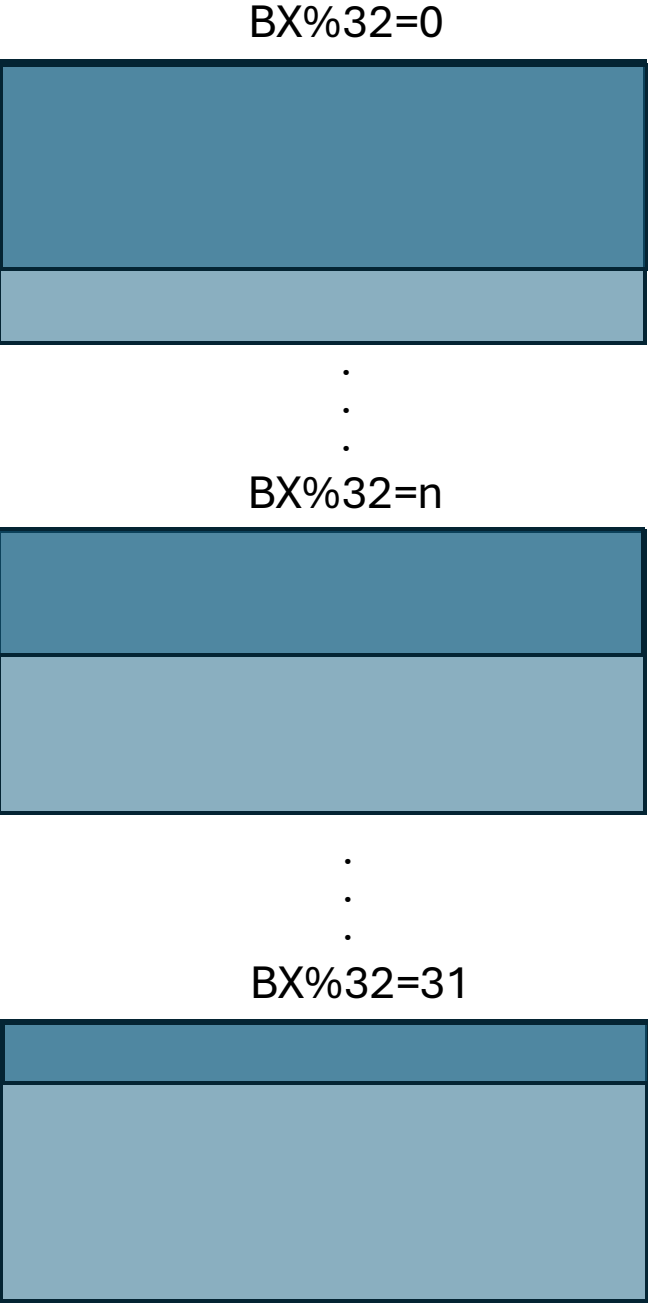


49	48	47	46	45	39	38	30	29	27	26	24	23	22	21	9	8	0
FEB ID	TDC ID (trailing)	Coarse (trailing)	Fine (trailing)	Col. ID	Pixel ID	TDC ID (leading)	Coarse (leading)	Fine (leading)									

ALCOR BUS

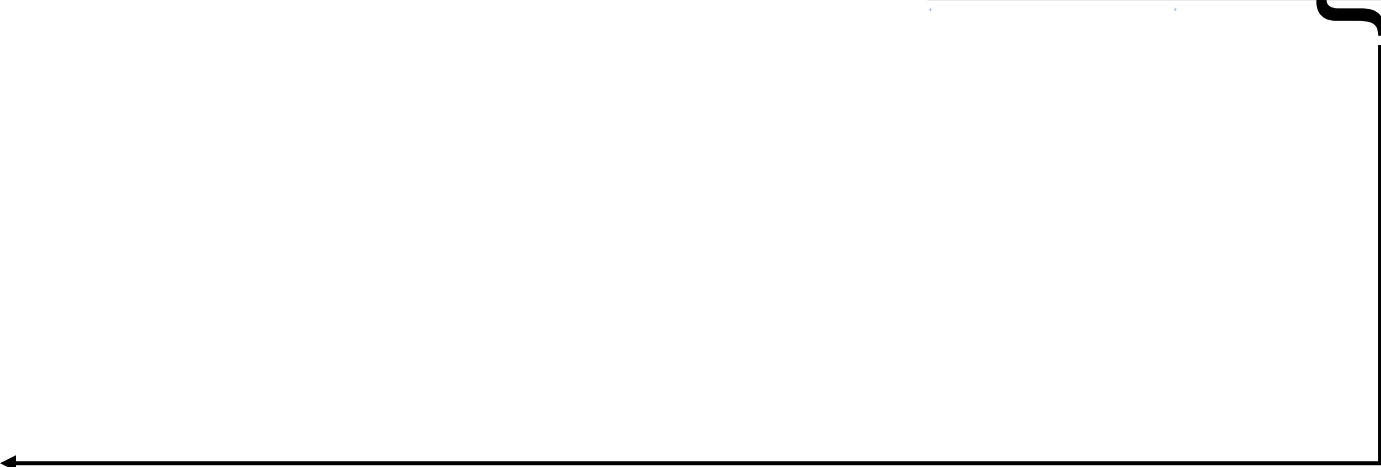
RDO to DAM

Buffering on RDO

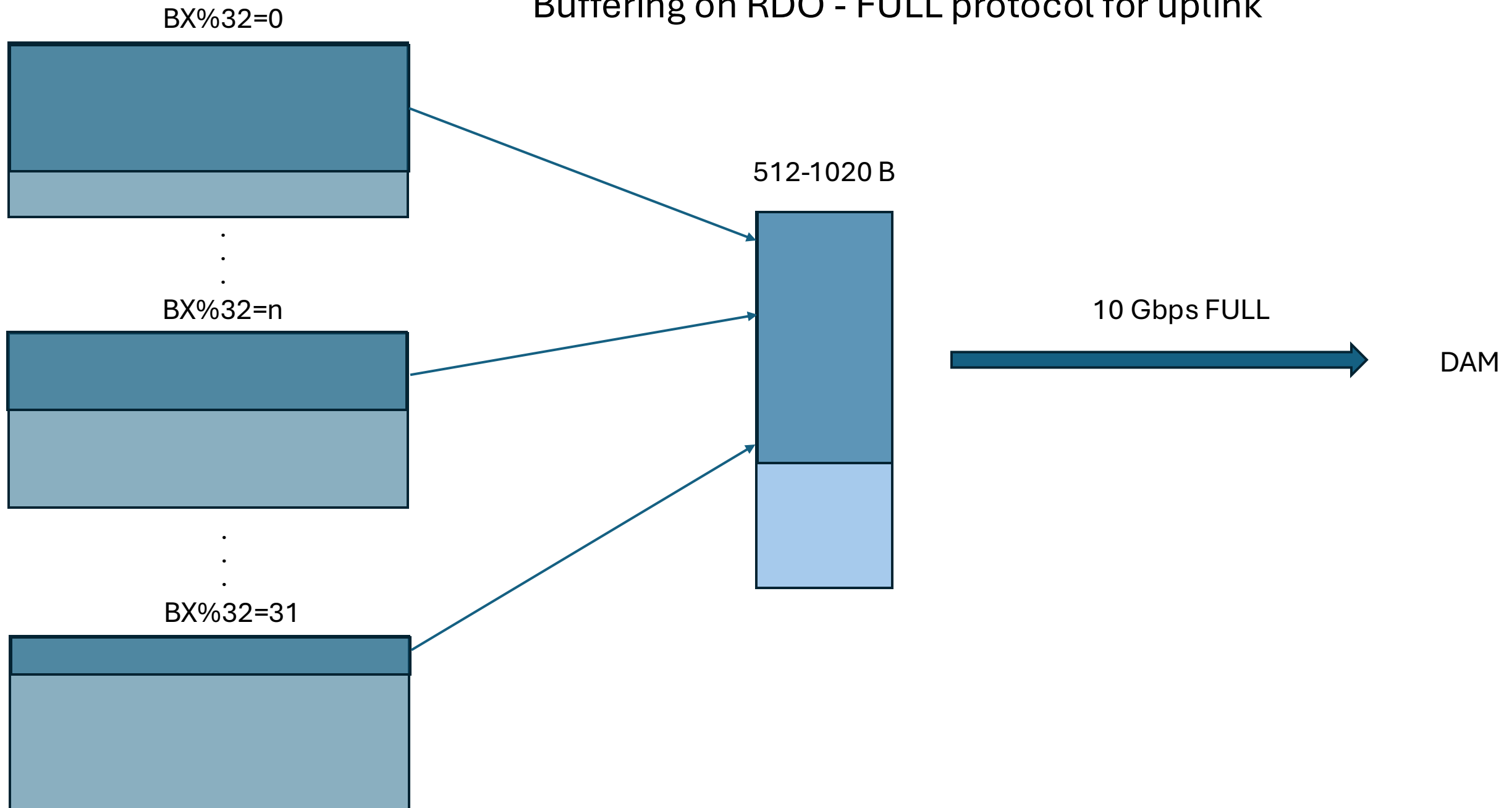


31	29	28	26	25	24	23	9	8	0
Col ID	Pix ID	TDC ID	Coarse Counter	Fine Counter					

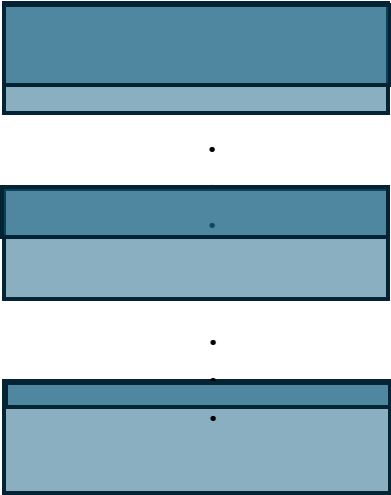
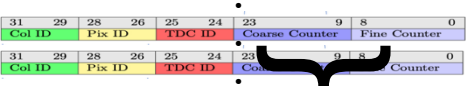
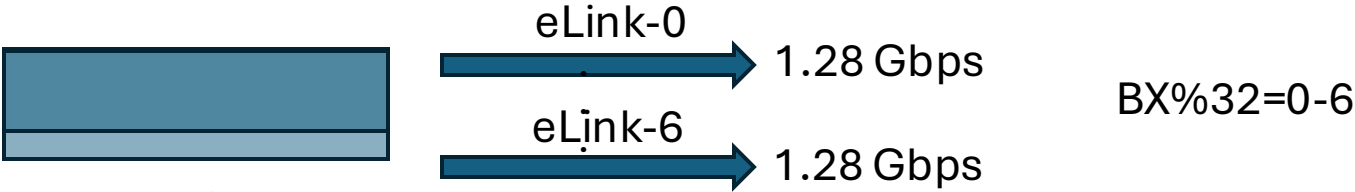
31	29	28	26	25	24	23	9	8	0
Col ID	Pix ID	TDC ID	Coarse Counter	Fine Counter					



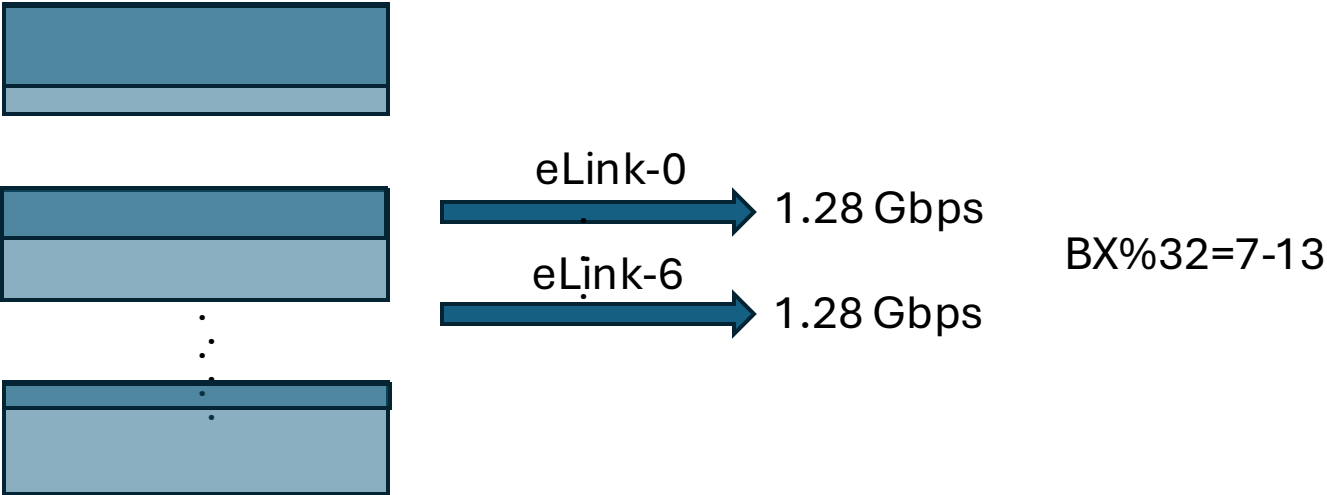
Buffering on RDO - FULL protocol for uplink



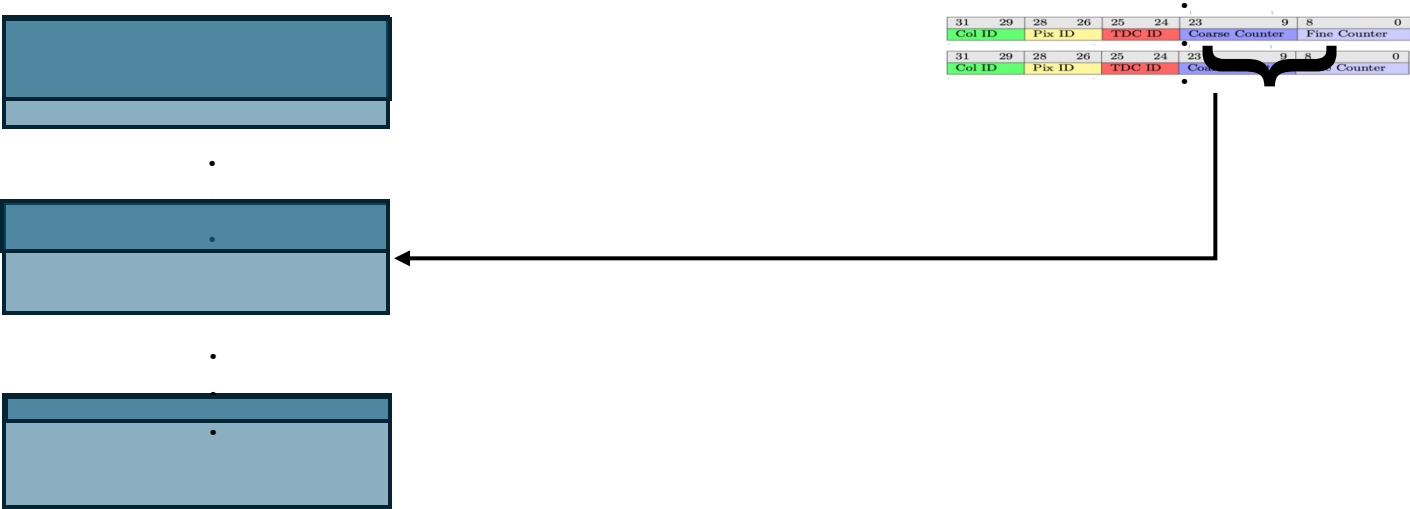
Buffering on RDO - lpGBT protocol for uplink (7 eLink @1.28 Gbps)



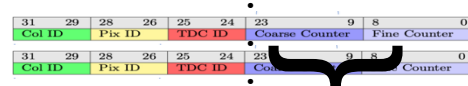
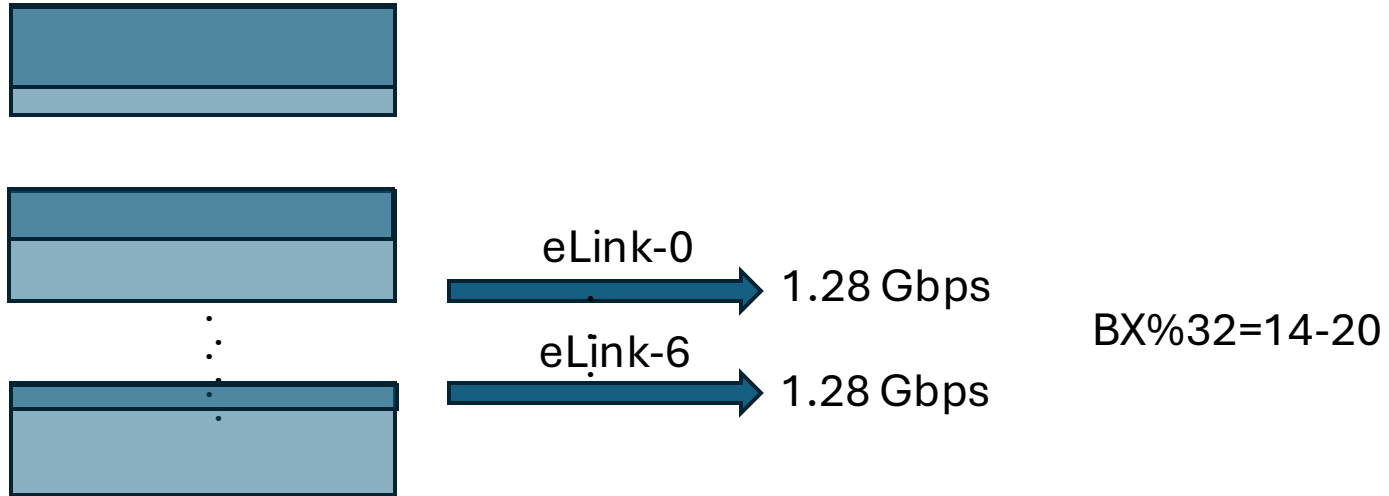
Buffering on RDO - lpGBT protocol for uplink (7 eLink @1.28 Gbps)



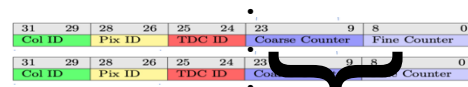
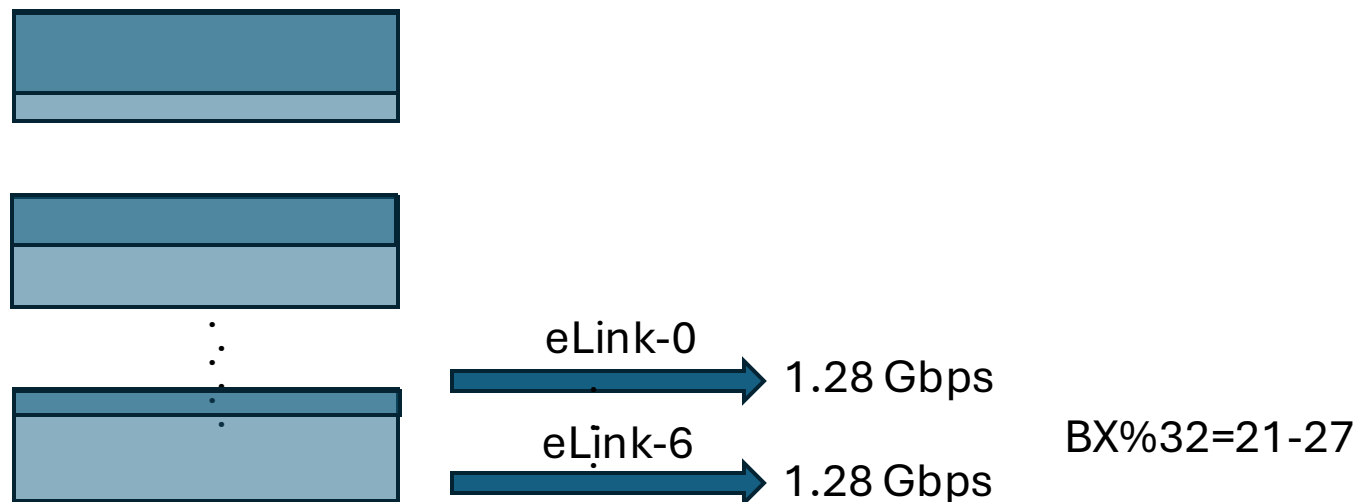
BX%32=7-13



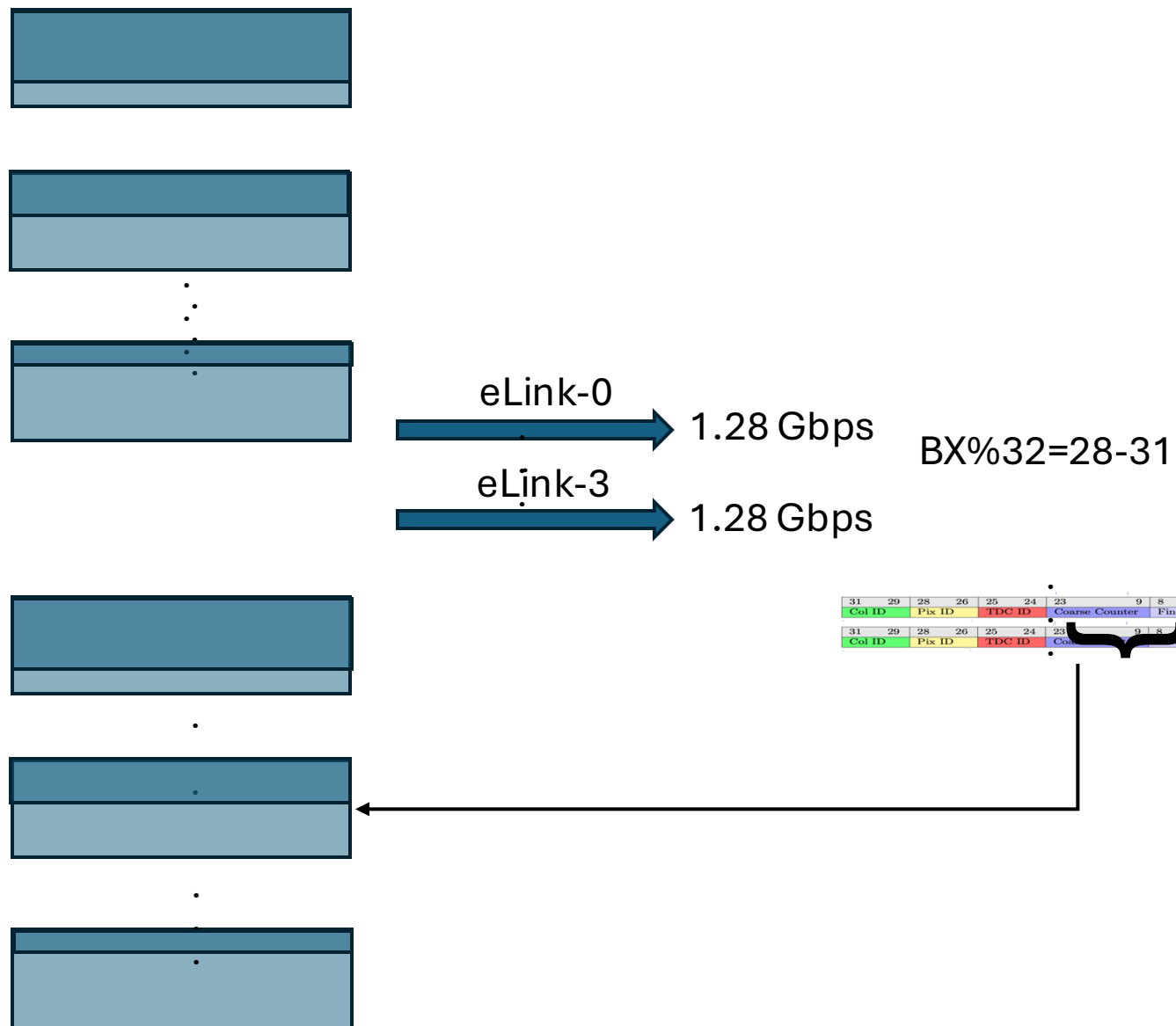
Buffering on RDO - lpGBT protocol for uplink (7 eLink @1.28 Gbps)



Buffering on RDO - lpGBT protocol for uplink (7 eLink @1.28 Gbps)



Buffering on RDO - lpGBT protocol for uplink (7 eLink @1.28 Gbps)



Discussion on payload content

- Testbed format: can be useful as a starting point
- Coarse timestamp vs finetime
- Event fragment building:
 - Distributed: 4 (Alcor) x 8 (Columns) on RDO, 42 (Channels) on DAM
 - Centralized: 4 (Alcor) x 8 (columns) x 42 (channels) on DAM