The electronics for the FDIRC can be seen as an upgrade of the electronics of the BABAR DIRC. The new requirements of the experiment (Trigger rate, background, radiation environment) and FDIRC specific requirements (resolution, number of channels and topology) have led to a similar but new design of the electronics chain.

The electronics will equip the 18,432 channels of the 12 sectors of the FDIRC. The electronics chain is based on a high resolution/ high count rate TDC, a time associated charge measurement on 12 bits and an event data packing sending event data frames to the data acquisition system (DAQ). The target performance of the overall electronics chain is a time resolution of 100 ps rms. This chain has to deal with a count rate per channel of 100 KHz, a trigger rate up to 150 KHz and a minimum spacing between triggers of about 50 ns.

The estimate radiation level is expected to be less than 100 rads per year. The use of radiation tolerant components or off the shelves radiation-qualified components is mandatory. However, the expected energy of the particles may make the latch-up effect almost impossible. Thus, the design has to take into account only Single Event Upsets. We selected the Actel family FPGA components for their non-volatile flash technology configuration memories, which are well adapted to radiation environment.

Several architectures have been considered which can be summarized has below:

- All electronics directly mounted on the FBLOCK.
- All electronics mounted next to the detector and linked to the PMTs by cables.
- A part of it on the detector (the Front-end boards) and the other part, called crate concentrator, situated close to the detector, (this board is in charge of interfacing with the Front-end, reading out event data, packing and sending it to the DAQ.

The first solution has been chosen as baseline for the TDR for two main reasons:

- The cost of the cables (PM to Front-end boards) is estimated to be close to 200 kEuros (1/3 of the price of the overall electronics cost), making this solution too expensive. Moreover, the possible option to have pre-amps on the PMT bases doesn't prevent from having electronics and power supplies on the detector.
- The large amount of data per channel leads to have the L0 derandomizer and buffer on the Front-end boards. The FCTS receiver could be individually located on each Front-end board but the number of cables needed pushes to distribute all the control signals on a backplane. Consequently the board dedicated to receiving and transmitting FCTS signals on the backplane naturally tends to also become the event data concentrator and the link to the DAQ.

The baseline design assumes a 16-channel TDC ASIC offering the required precision of 70 ps rms- embedding an analog pipeline in order to provide an amplitude measurement transmitted with the hit time. Thanks to a 12-bit ADC, the charge measurement will be used for electronics calibration, monitoring and survey purposes. The Front end board FPGA synchronizes the process, associates the time and charge information and finally packs them into a data frame which is sent via the backplane to the FBLOCK control board (FBC). The FBC is in charge of distributing signals coming from the FCTS and ECS, packing the data received from the FE boards to a n-event frame including control bits and transferring it to the DAQ.

The TDC chip

A former TDC chip offering the requested performances of resolution has already been designed for the SuperNemo experiment. It provides a time measurement with both a high resolution 200 ps step (70 ps RMS) and a large dynamic range (53 bits). The architecture of this chip is based on

the association of Delay Locked Loops (DLLs) with a digital counter, all of these components being synchronized to a 160 MHz external clock.

The SuperB chip – SCATS – will keep the same philosophy but the high input rate requirement lead to a complete re-design of the readout part, in order to minimize the dead time per channel. Instead of registers and multiplexer which are the bottlenecks of the SuperNemo chip readout, it makes use of an individual FIFO memory per channel in order to derandomize the high frequency bursts of input data. With this architecture, data from the DLLs and the coarse counters are transferred into the FIFO memory within two clock cycles. When the transfer is complete, the channel is automatically reset and ready for the next hit. Simulations of the readout state machine showed an output FIFO data rate capability of 80 MHz. Time ranges for the DLLs and the coarse counter can be easily customized by adjusting the output data format (16, 32, 48 or 64 bits). Therefore, the chip is suitable for various applications with either high count rate and short integration time or low count rate and long integration time.

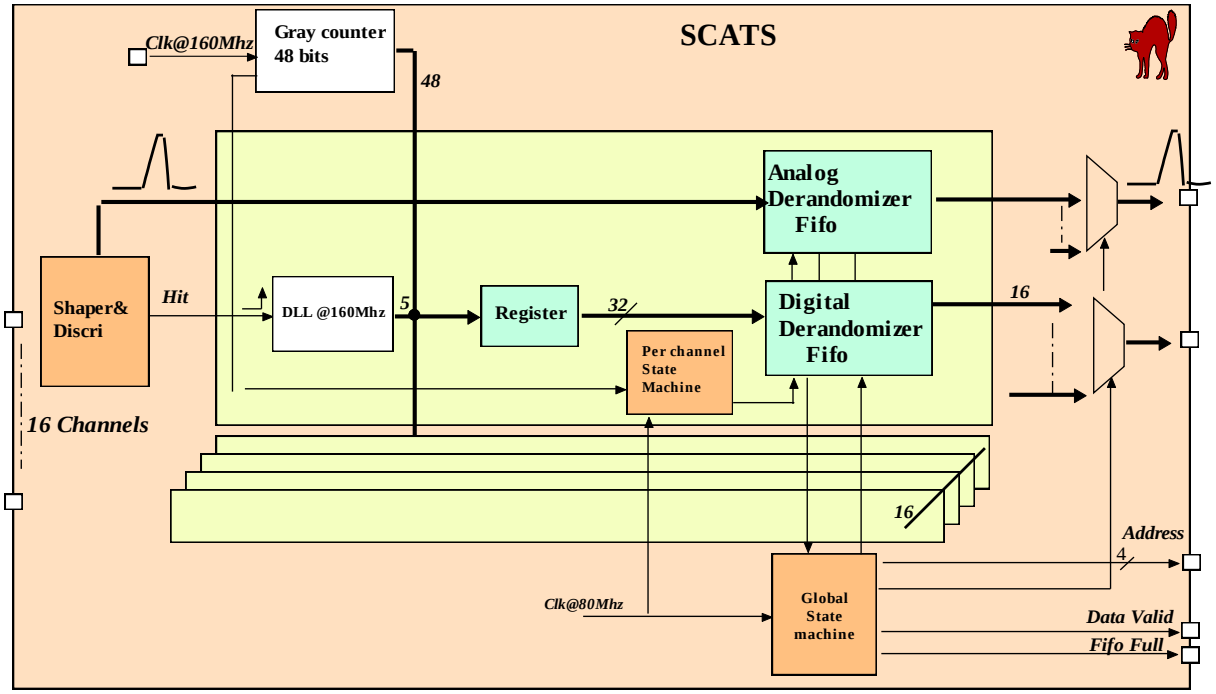


Fig 1: block diagram of SuperB FDIRC TDC chip -SCATS-.

A FIFO depth of 8 words has been selected after simulation with a exponential distribution model of delta time between hits (mean rate ~ 1MHz) applied to inputs. Thus the simulation gives a dead time ~ 1% with 500 kHz input rate on each channel.

To design this FIFO a full custom RAM has been developed. It permits reducing the size of the chip and consequently its cost.

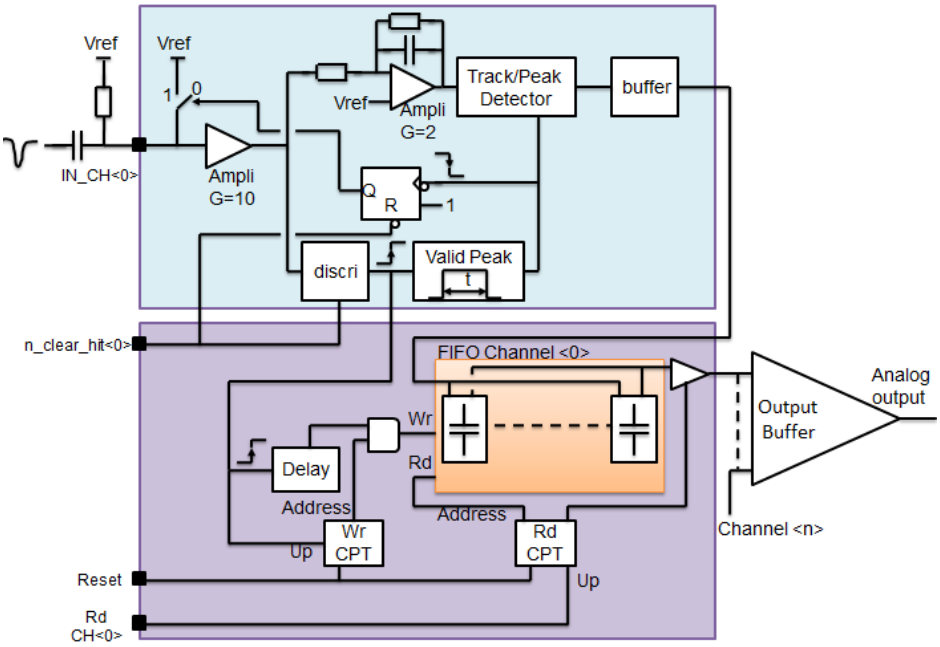
The chip is designed using known and proved mitigation techniques to face single event upset (SEU) issues due to the low-level radiation environment.

A first version of the chip without the analog FIFO and the discriminator has been submitted in November 2011 and the test are

We plan to submit in 2012 one chip PIF dedicated to the currently missing parts:

- A low walk (~ 50 ps) discriminator based on a CFD like design.
- A Track/peak detector to be able to sample the maximum of the signal.

- An analog pipeline synchronized with the digital FIFO and providing analog output for charge measurement.



PIF : one channel synopsis .

After testing and validation, it is foreseen to be included in the final version of SCATS taking benefit of sharing the FIFO pointers of the analog and digital parts. The chip will be assembled and submitted end 2013

The Front-end crate

The board input will fit the topological distribution of the PM on the FBLOCK. The PMs are arranged as a matrix of 6 in vertical direction by 8 in horizontal direction. Each column of 6 PMs will fit to one FE board. One vertical backplane (PM Backplane) will interface between the 4 connectors of each PM base to one connector of FE board. The PM Backplane is also in charge of distributing the High Voltage, thus avoiding HV cables to pass over the electronics. The FB_ crate will use as much as possible the elements of a commercial crate, in order to avoid the design of too many specific elements like board guides.

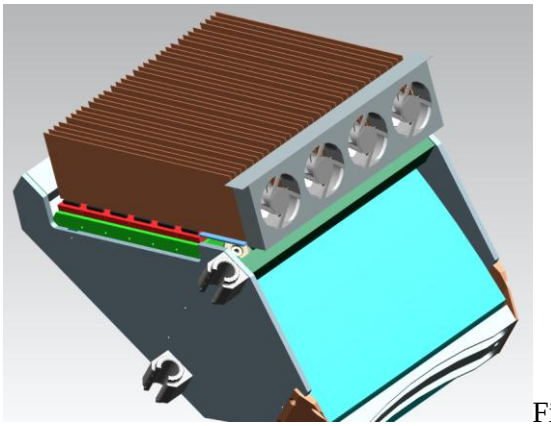


Fig 2
The FBLOCK equipped with the boards and fan tray

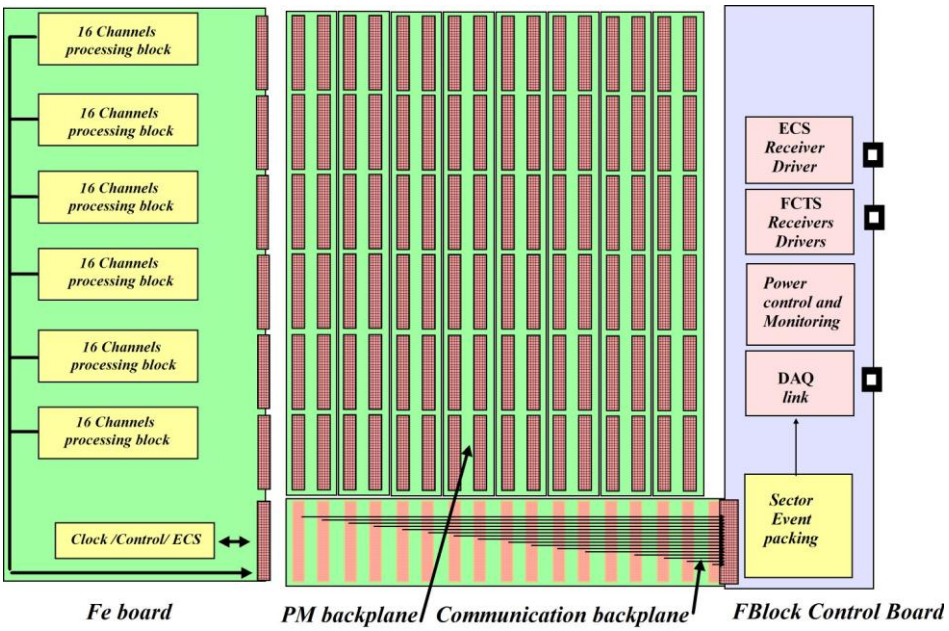


Fig 3 **: Front end crate**

The Communication Backplane

Distributes the ECS and FCTS signals from the FBC to the 8 FE boards thanks to point to point LVDS links.

Connects each FE board to the FBC for data transfer. A serial protocol will be used between FE board and the FBC in order to reduce the number of wires and consequently ameliorate the reliability. It will also distribute JTAG signal for FPGA board reprogramming and all signals for monitoring and control of the crate.

The PMT Backplane

It is an assembly of 8 motherboards, each one corresponding to a column of 6 PMTs. One motherboard receives 2 Fe-board. The 64 channels from 4 connectors per each PMT are merged on the motherboard into two connectors to get into the Front end board to get 16 channels per half PMT, i.e., 6 PMTs correspond to 96 channels per FE-board. It also insures the ground continuity between FE-boards – crate – FBLOCK.

Cooling and power supply

The electronics is located on the detector in a place enclosed by the doors. There are 2 major consequences: one is the problem of the cooling which must be carefully studied in terms of reliability and capability and the second is that the location is naturally shielded. Consequently the use of magnetic sensitive components as coils or fan trays is possible.

An estimation of the overall electronics consumption lead to ~ 6 kW, not including the external power supplies. This can be broken down to individual contribution as follows:

- Electronics: 0.325W/channel, 500 W/sector and 6 kW/system.
- HV resistor chain: 0.19W/tube, 9.1W/sector, and 109 W/system.

The cooling system must be designed in order to maintain the electronics located inside at a constant temperature close to the optimum of 30 degrees. The air inside the volume must be extracted while the dry, clean temperature controlled air will be flowing inside. Each FB crate will have its own fan tray like in a commercial crate. Targeting a difference of 10 degrees between inside and outside temperature drives to a rough estimate value of 300 m3/h per crate, 4000 m3/h can be considered as the baseline value for the whole detector.

The Front-end board

One Front-end board is constituted of 6 channel-processing blocks handling the 96 channels. The channel-processing block is constituted by one SCATS chip, one ADC, one Actel FPGA and the associated glue logics.

The FPGA receives event data from the TDC and the converted associated charge from the ADC. From one 16 bit bus of the 16 channels coming from the TDC, it de-serializes to 16 data path where events are keeping in a buffer until they are thrown away if there are too old (relatively to the trigger) or sent upon its reception.

The PGA master receives event data from the 6 channel processing blocks and packs the event.

The FE board transfers the event frame in differential LVDS to the FBC via the communication backplane.

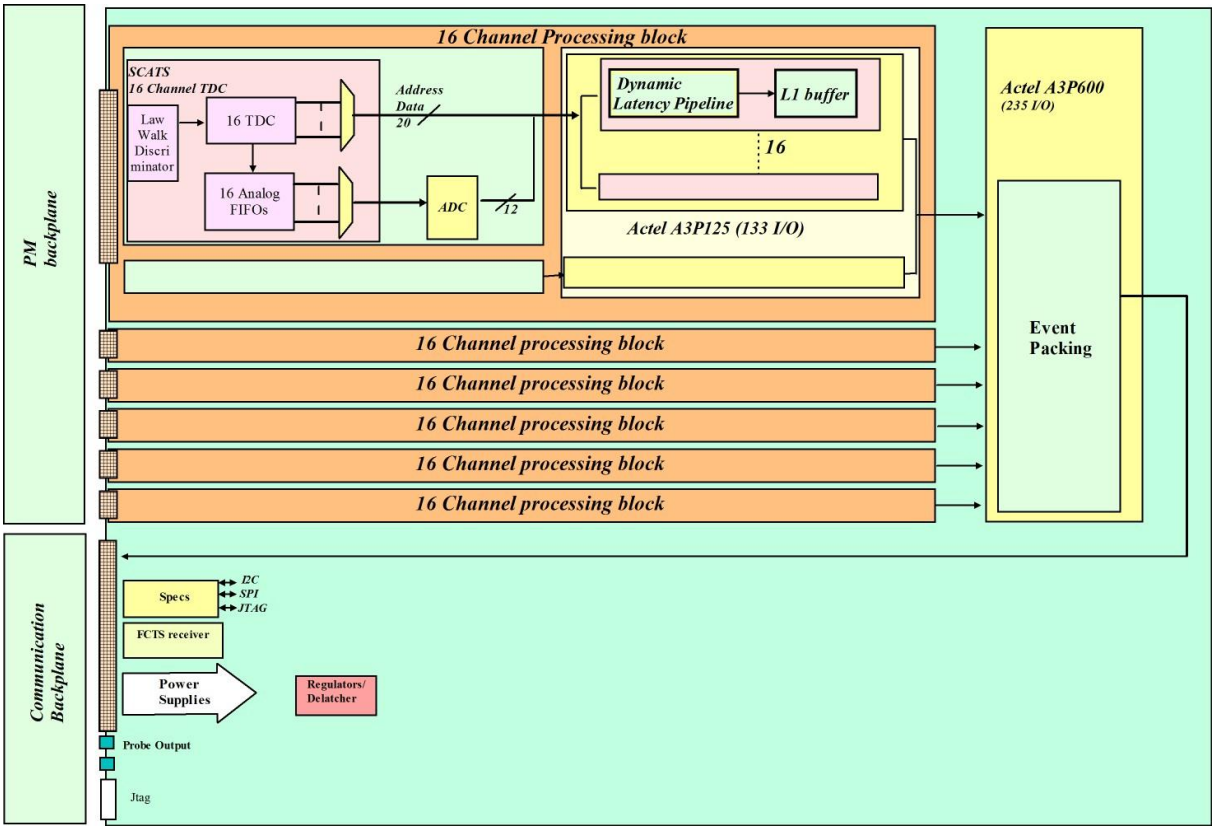


Fig 4 : **the Front-end board connected to the two backplanes**

The crate controller board (FBC)

The FBC is the board which gathers the front-end data, control and monitors the crate. There is one board per crate. The board handles several functionalities:

- Receives the event data from the Front-end boards via the communication backplane, constitutes an event data frame for the DAQ.
- Spy data building for monitoring and commissioning purposes.
- Distributes the ECS (SPECS) signals to the front end. Distributes the JTAG.
- Deserialize Clock and control signals from FCTS.
- Monitor the crate: temperature, power supplies, fans.