SuperB IFR electronics: update

A.Cotta Ramusino
on behalf of the IFR collaboration

SuperB IFR electronics: update

- **writing of TDR:**
  - highlights
- **preparing for the coming irradiation tests at LNL and IRMM-Geel:**
  - "GELINA", a neutron time –of-flight facility
  - SiPM test setup
  - EASIROC, CLARO and RAPSODI ASICs test setup

- details of the SiPM installation

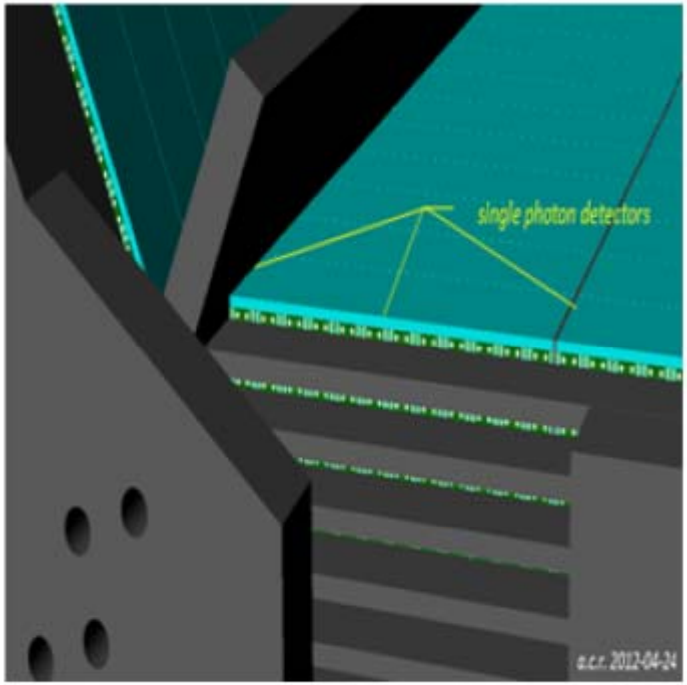


Figure 1.2: detector modules (with the metal enclosure removed) of IFR barrel, layer 0

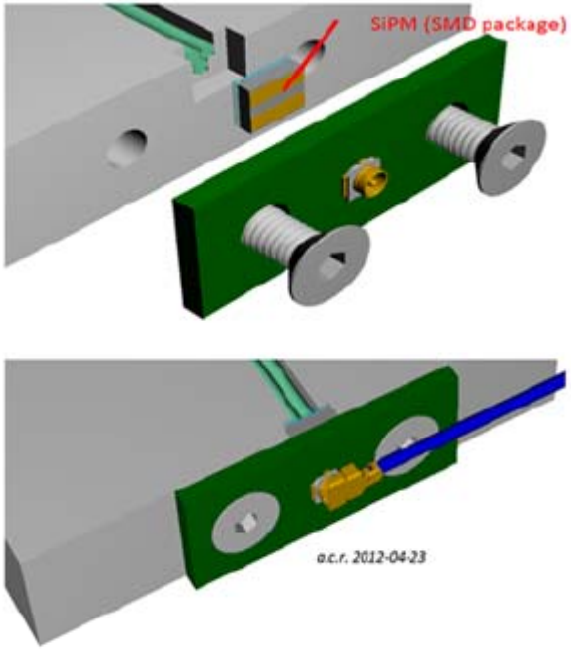
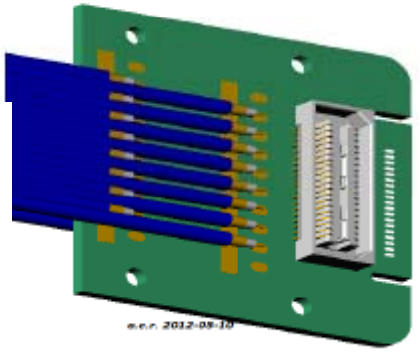


Figure 1.1: details of the three WLS fibers and the PCB for the SiPM



igure 1.18: Detail of the multi coaxial connector assembly

- outline of a dedicated ASIC for reading out the IFR SiPM

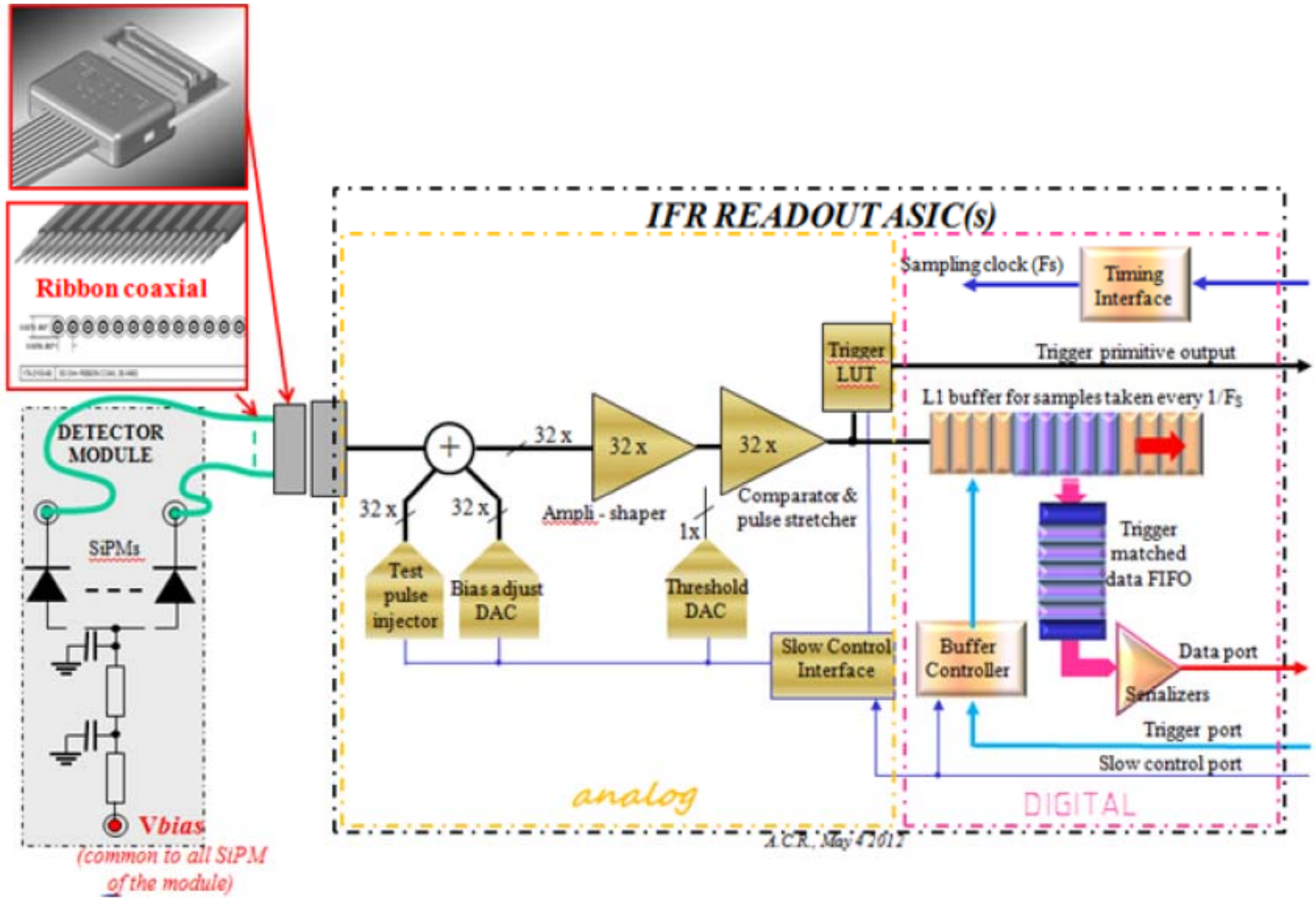


Figure 1.15: block diagram of the IFR readout ASIC

SuperB IFR electronics: TDR highlights

- locations of on-detector electronics

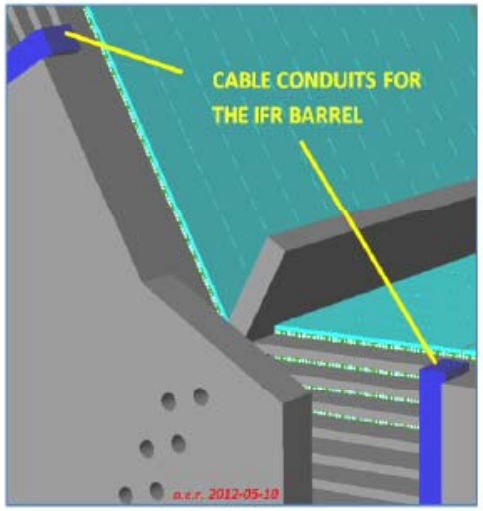


Figure 1.16: The IFR cable conduits for 2 sextants

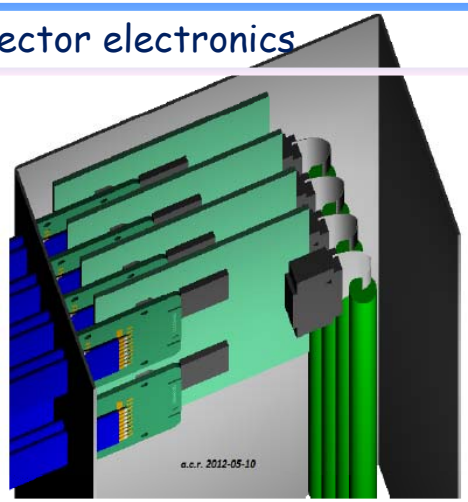


Figure 1.17: Detail of front end cards installed in the IFR cable conduit

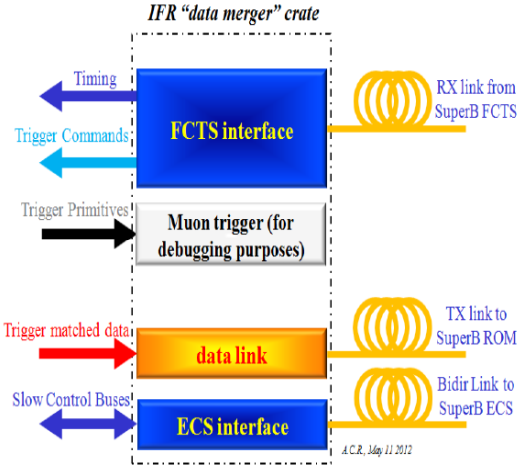


Figure 1.20: Main functions performed by the electronic units in the data-merger crate

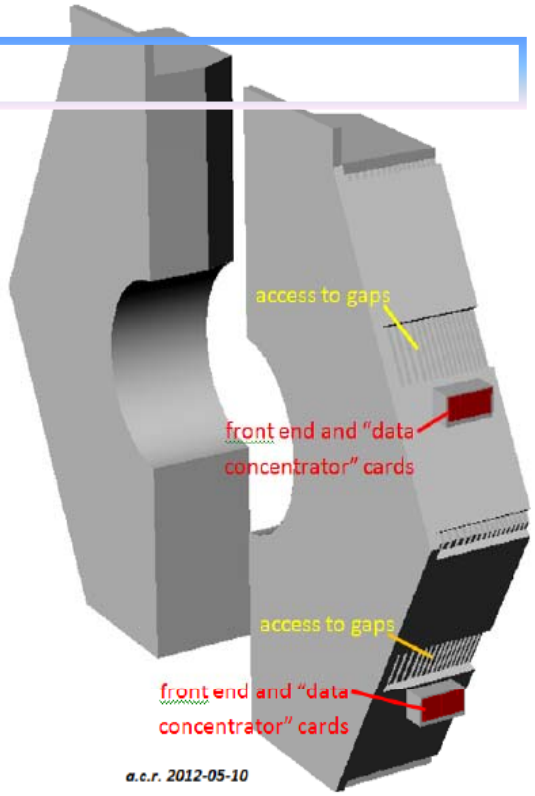


Figure 1.19: Perspective view of IFR endcaps

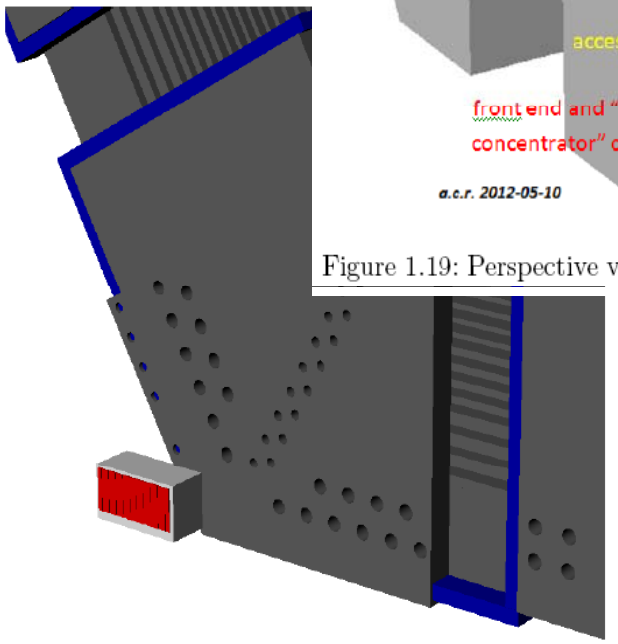
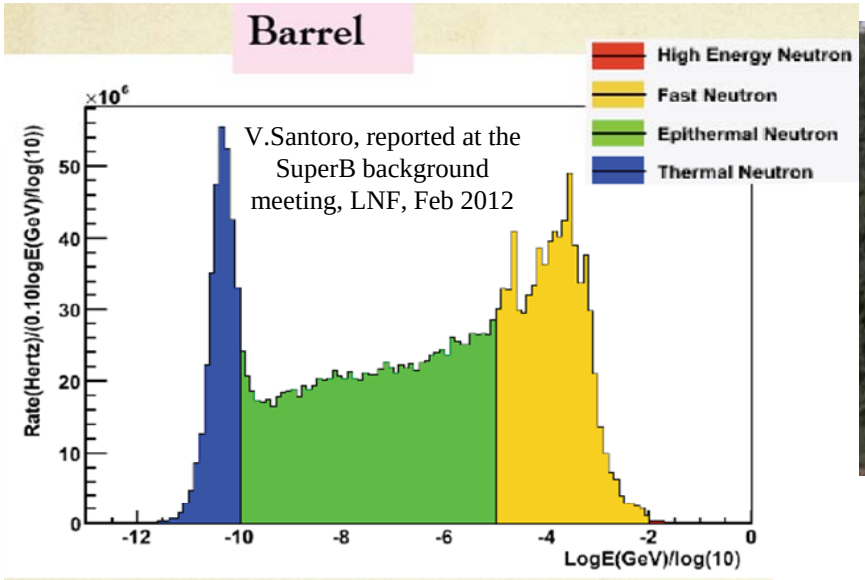


Figure 1.21: The location of one of the 6 data merger crates for the barrel

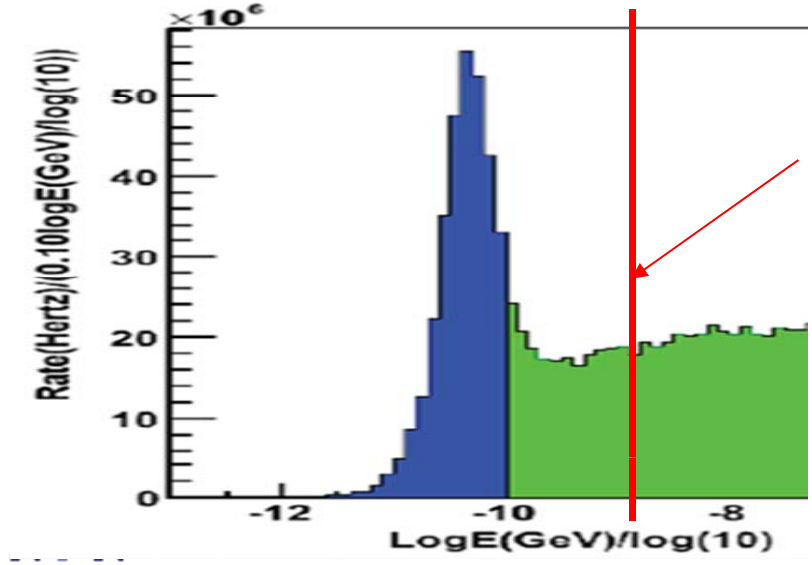
SuperB IFR electronics: preparing for irradiation tests

- "GELINA", neutron time -of-flight facility at the Institute for Reference Materials and Measurements (IRMM)



V.Santoro, reported at the SuperB background meeting, LNF, Feb 2012

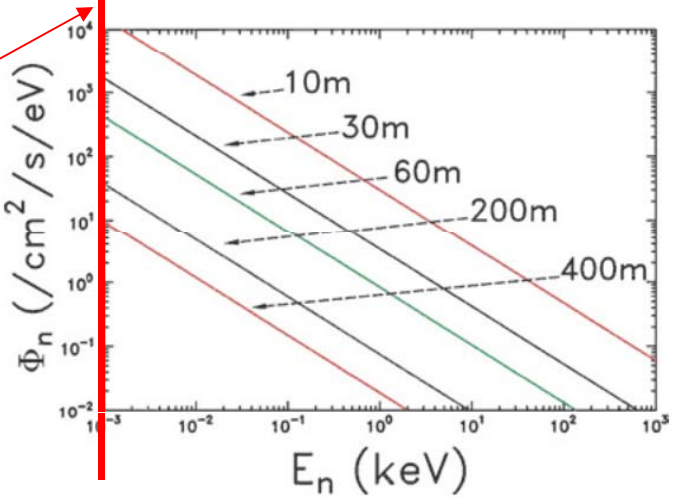
http://irmm.jrc.ec.europa.eu/about_IRMM/Pages/index.aspx



1 eV

GELINA neutron time-of-flight facility

The neutron flux in GELINA.



SuperB IFR electronics: preparing for irradiation tests

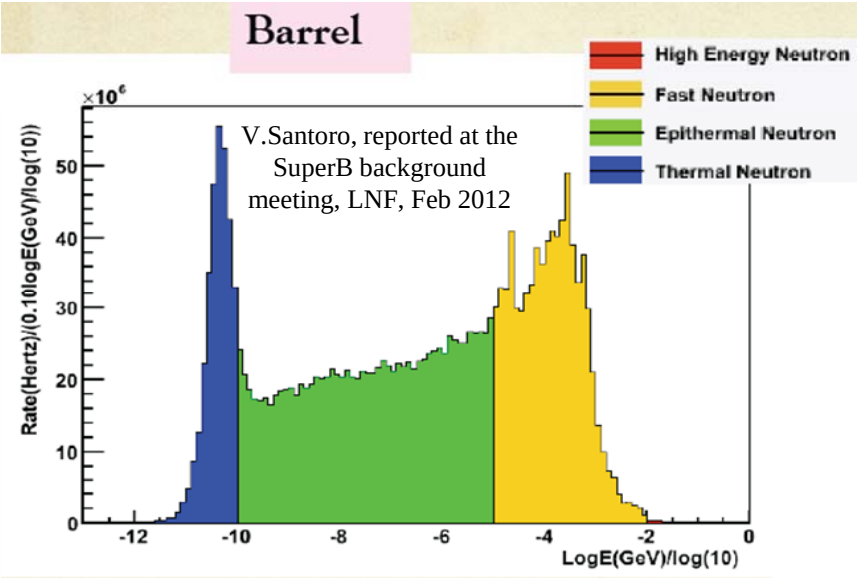
Main goal of the SiPM test at the GELINA neutron time-of-flight facility at IRMM-Geel:

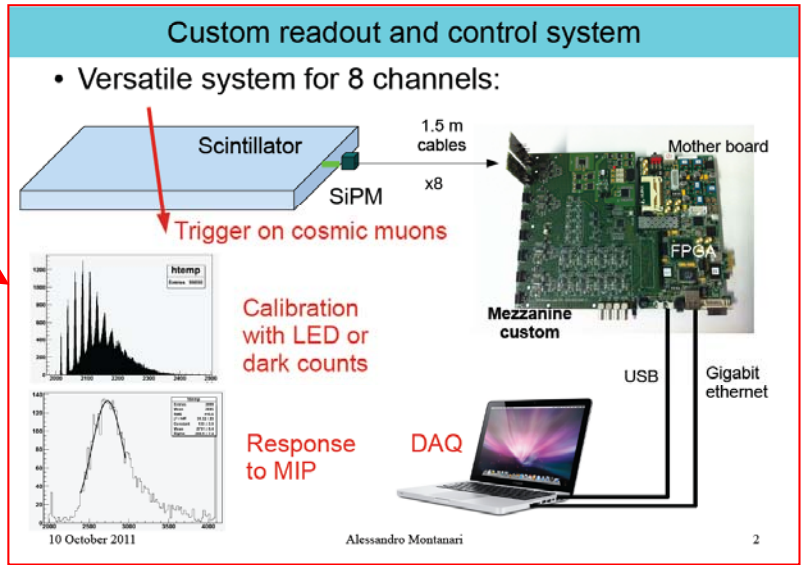
- to study SiPM damage induced by thermal neutrons (cfr. background neutron energy spectrum for IFR)
- to verify effectiveness of thermal neutron shields

- **specification for electronics:**
  - parallel testing of a sufficient number of SiPM samples of different layout and of different manufacturers
  - monitoring of significant SiPM operational parameters such as:
    - bias current (by commercial DAQ system)
    - dark current / dark count (by ABCD board)
    - gain monitoring: to do this we plan to illuminate the SiPMs and to evaluate the SIPM gain by collecting pulse amplitude histograms with the electronics provided by the collaborators of INFN Bologna
    - temperature monitoring (by commercial DAQ system)

Secondary goal:

- to study effects of thermal neutrons on FPGAs and ASICs in 0.35um AMS technology.
- to study effects of thermal neutron on COTS such as LDO regulators



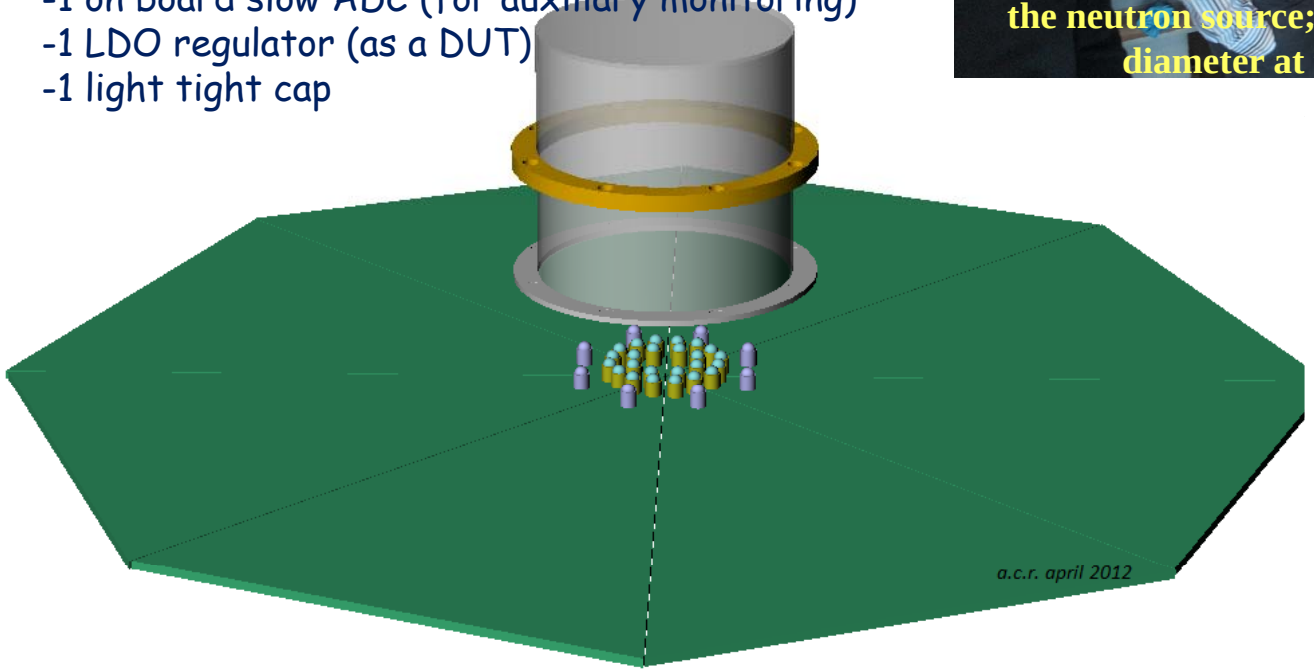


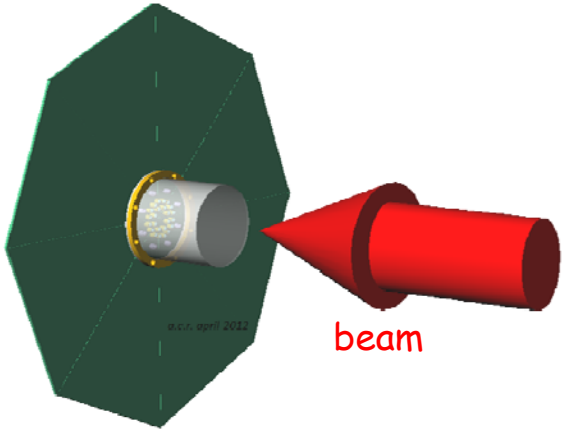
SuperB IFR electronics: preparing for irradiation tests

- SiPM test fixtures: proposed arrangement

A wheel made of 8 PCB in form of octagonal slices is foreseen. Each slice will host:
-3 SiPM of an homogeneous type: all are read by an "IFR-ABCD" card; one is also readout by the Bologna readout card.
-1 DAC for setting the SiPM bias corrections, since the 3 SiPM share a common "high side" bias voltage.
-1 LED to provide light pulses for gain monitoring
-1 temperature sensor (Pt100)
-1 on board slow ADC (for auxiliary monitoring)
-1 LDO regulator (as a DUT)
-1 light tight cap

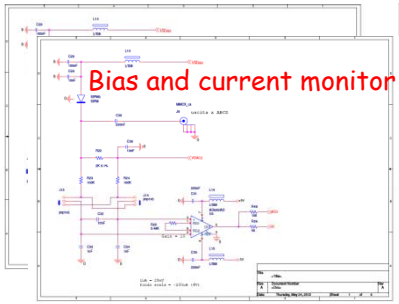
IRMM's Dr. Peter Schillebeeckx indicating the test station at 10m from the neutron source; the beam is 5cm in diameter at this location

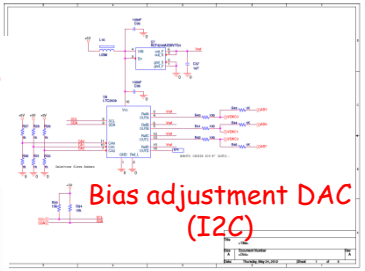


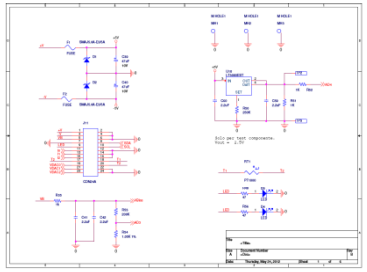


SuperB IFR electronics: preparing for irradiation tests

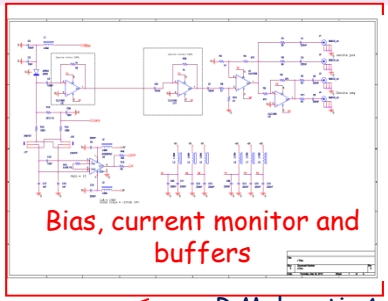
- SiPM test fixtures: schematic of a unit for 3 SiPM

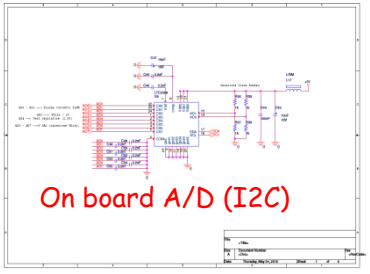




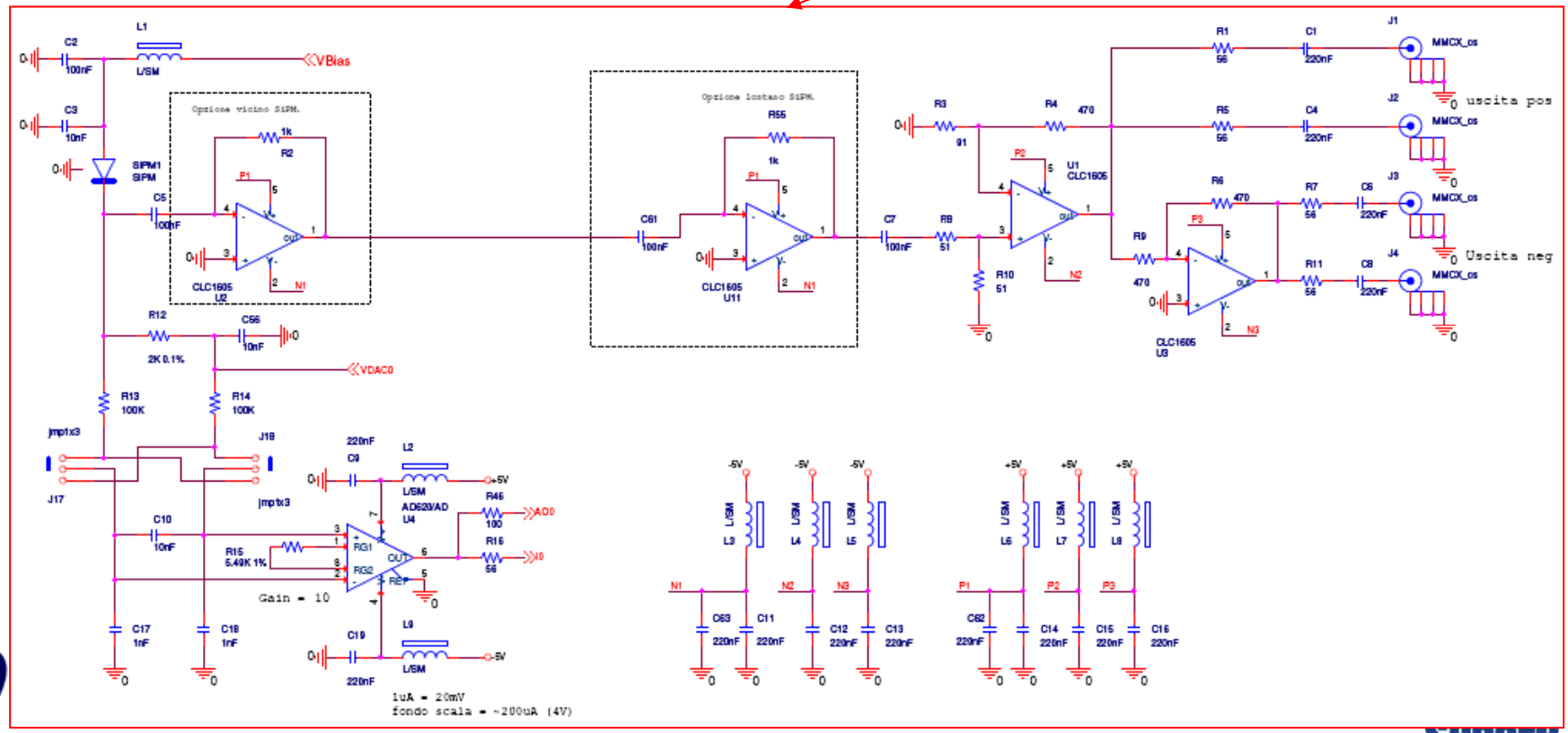


LDO reg (as a DUT) and I/O connectors



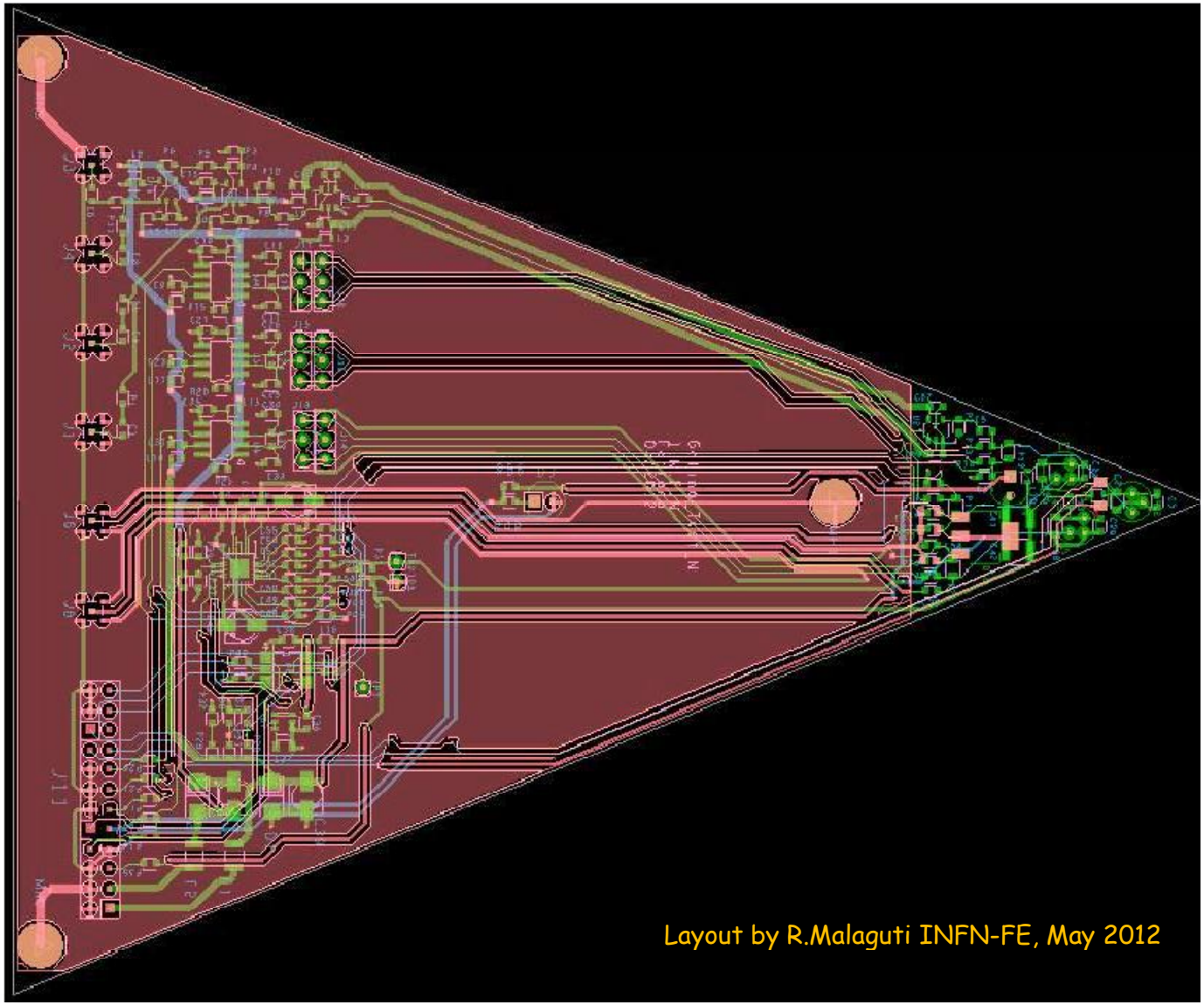


R.Malaguti, A.C.R., INFN-FE apr-may 2012



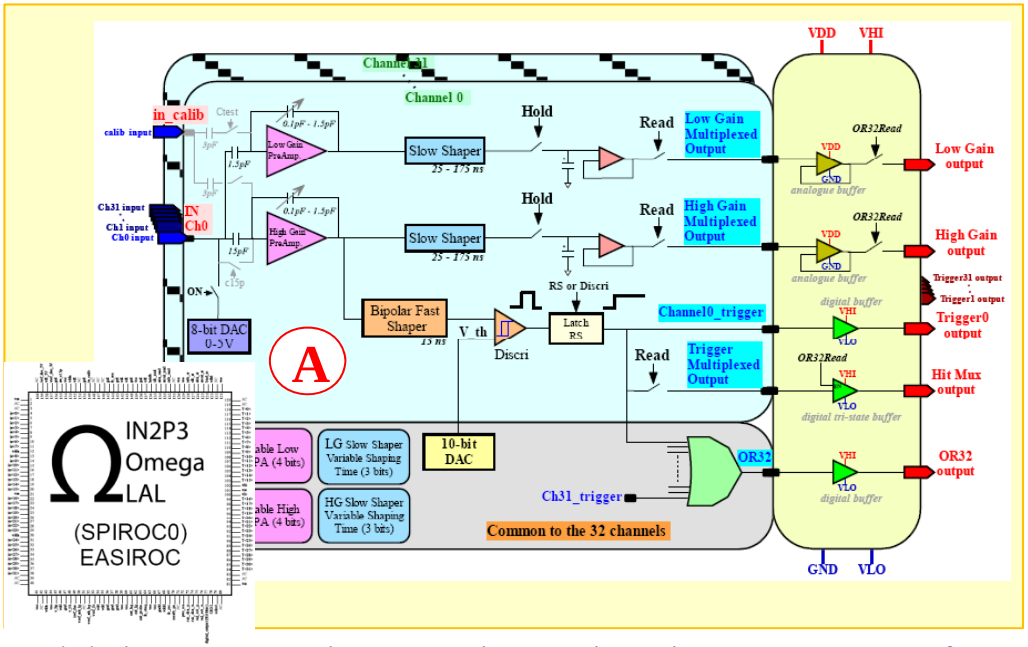
SuperB IFR electronics: preparing for irradiation tests

- SiPM test fixtures: layout of a unit for 3 SiPM



Layout by R.Malaguti INFN-FE, May 2012

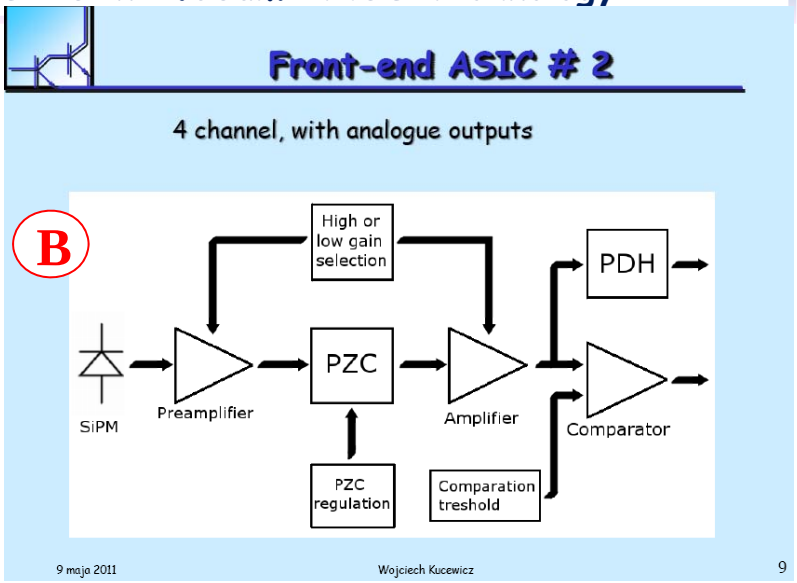
goal of the ASIC test at the INFN Laboratori Nazionali di Legnaro (LNL) and at the GELINA: to assess permanent damage and SEL cross section of ASICs in 0.35um CMOS technology

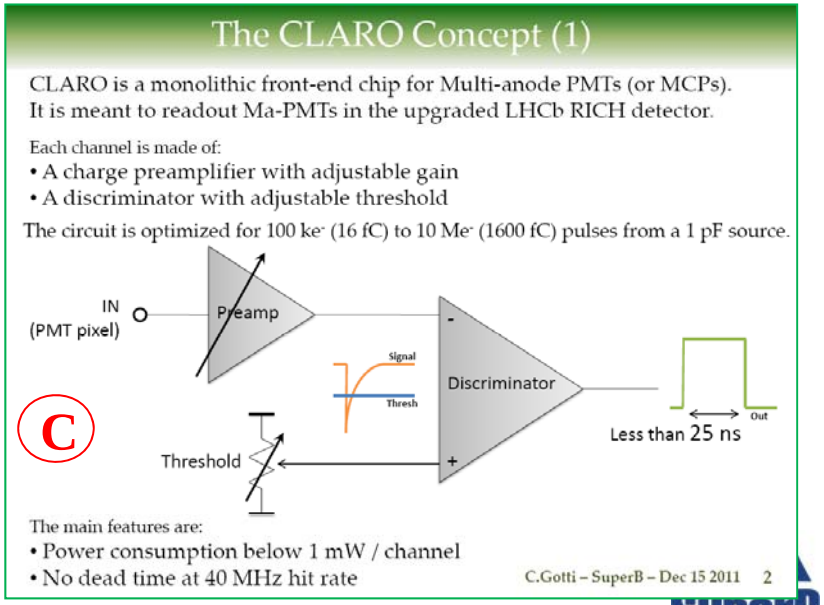


(A)The EASIROC has been designed by the Omega group of LAL and it has been extensively used and tested in Ferrara thanks to evaluation board provided by LAL. It has already described in previous presentations

(B)The RAPSODI ASIC#2 has been designed by **Woitek Kucewicz** of AGH University in Cracov Poland. It has already been introduced in previous presentations

(C)The CLARO ASIC has been designed by **Gianluigi Pessina and Claudio Gotti** and presented at the 2nd SuperB meeting last December.





goal of the ASIC test at the INFN Laboratori Nazionali di Legnaro (LNL) and at the GELINA: to assess permanent damage and SEL cross section of ASICs in 0.35um CMOS technology

- **permanent (total dose effects) damage test:**

1) the ASIC under test is characterized before irradiation: for the CLARO and the EASIROC ASICs we are going to record the linearity response of the internal DACs and the S-curves for the comparators. The RAPSODI ASIC#2 chips have been characterized by the designer, W.Kucewicz
2) the same characterization is repeated after irradiation and differences, if evident, are analyzed.

- **Single Event Latchup (SEL) test:**

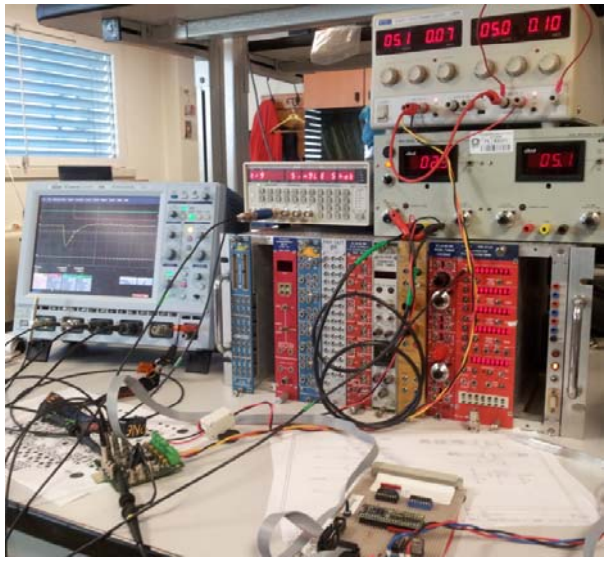
1) the ASIC is powered, throughout the irradiation period, by means of a SEL detector circuit which cuts the ASIC supply voltage if a large and sudden increase in the supply current is detected. An off-the-shelf digital I/O module is used to remotely reset the circuit and count the occurences.

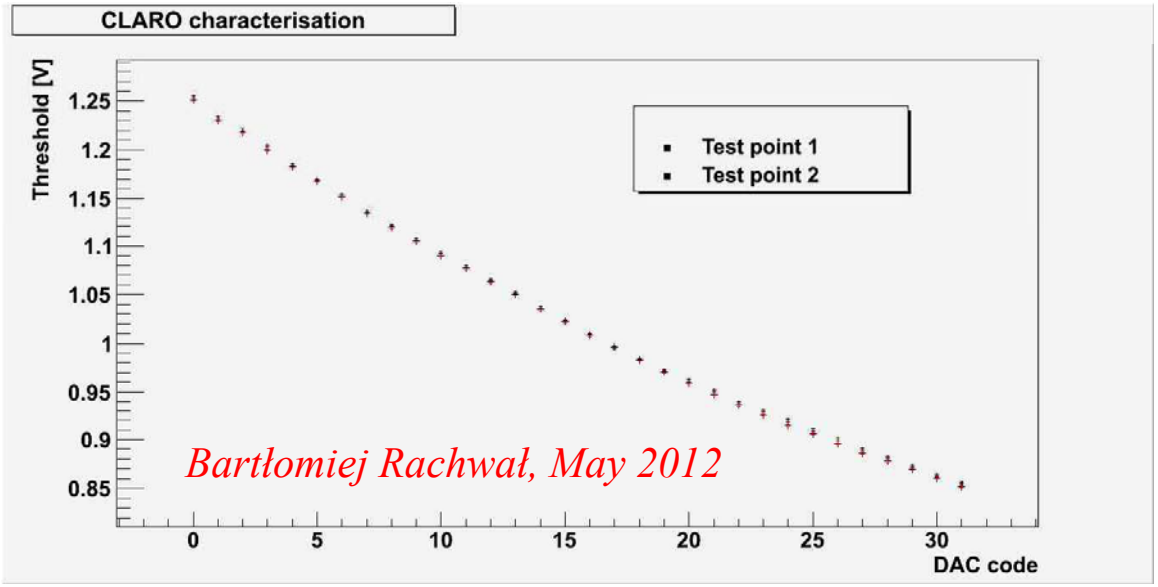
- **Single Event Upset (SEU) test:**

Since the CLARO and the RAPSODI ASIC#2 do not have any readback digital register this test can only be conducted for the EASIROC chip (and it has already been conducted infact at the LNL facility on 2011).

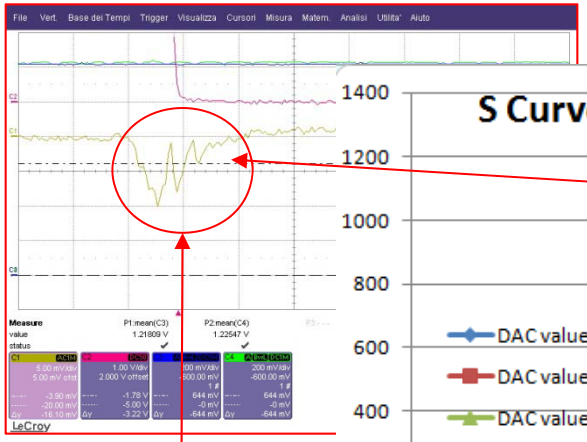
SuperB IFR electronics: preparing for irradiation tests

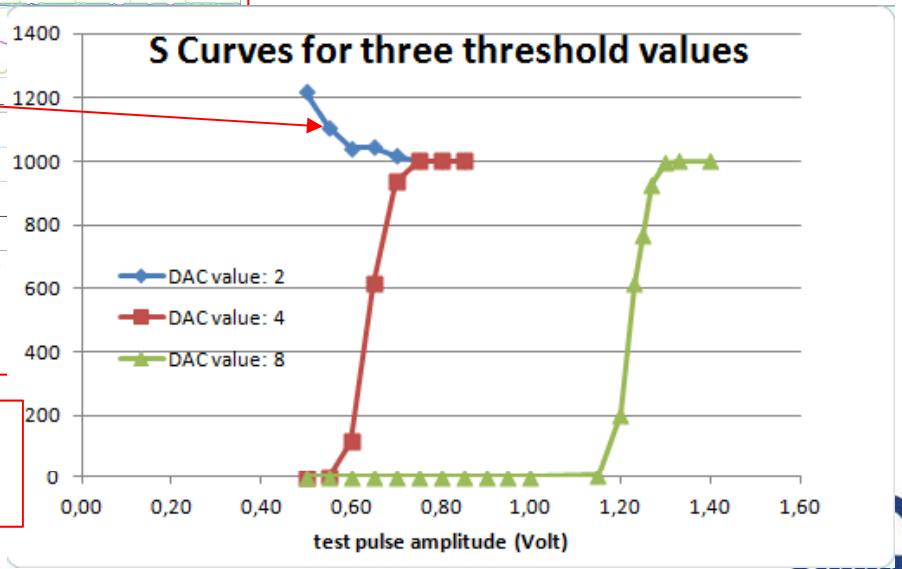
- pre-irradiation characterization of the target ASICs





CLARO characterization test setup at INFN_FE.
The tests have been performed by Bartłomiej Rachwał, visiting PhD student from Cracow University

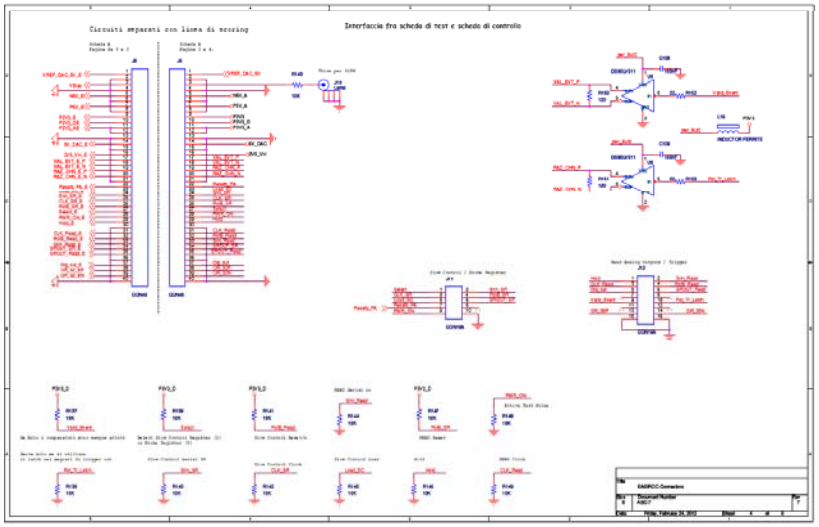


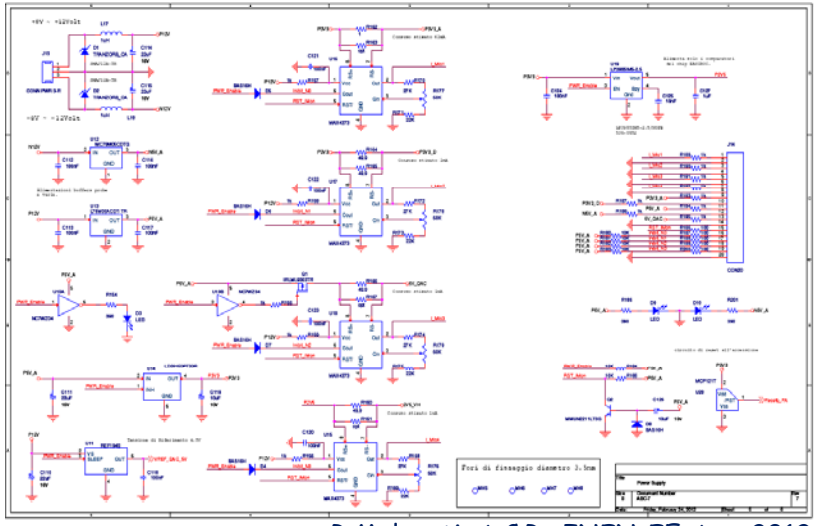


Monitoring the analog and digital outputs introduces some artifact at lower threshold settings

SuperB IFR electronics: preparing for irradiation tests

- *ASICs test fixtures: the Single Event Latchup detection/protection board*





R.Malaguti, A.C.R., INFN-FE Apr. 2012