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PEOPLE
MARIE CURIE ACTIONS

Intra-European Fellowships (IEF)
Call: FP7-PEOPLE-2013-IEF

PART B

“APIMAP”
Advanced Parallel Implementations for associative Memory APplications

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MAIN ETHICAL ISSUES THAT MUST BE ADDRESSED

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AREAS EXCLUDED FROM FUNDING

- Research activity aiming at human cloning for reproductive purposes.
- Research activity intended to modify the genetic heritage of human beings which could make such changes heritable (Research related to cancer treatment of the gonads can be financed).
- Research activities intended to create human embryos solely for the purpose of research or for the purpose of stem cell procurement, including by means of somatic cell nuclear transfer.

Include the Ethical issues table below. If you indicate YES to any issue, please identify the pages in the proposal where this ethical issue is described. Answering 'YES' to some of these boxes does not automatically lead to an ethical review. It enables the independent experts to decide if an ethical review is required. If you are sure that none of the issues apply to your proposal, simply tick the YES box in the last row.

B1 Research and technological Quality (maximum 8 pages)

- ***Research and technological quality, including any interdisciplinary, multidisciplinary aspects of the proposal***

The Physics programme at CERN's Large Hadron Collider (LHC) has been extremely successful since the early phase of data taking in the year 2010. The detectors were designed to search for new discoveries in the head-on collisions of protons of extraordinarily energy. Among the most interesting searches are the origin of mass, space extra dimensions, fundamental forces unification, dark matter candidates evidence in the Universe.

Moreover, the LHC upgrade, currently called the Super LHC (SLHC), will provide continuously increasing instantaneous luminosity, and will widen our capability to search new phenomena that are beyond the scope of our current theory of matter and energy, the Standard Model (SM). In the next few years an impressive harvest of data will be collected at the LHC and at the same time R&D at the technological frontier will be pursued for SLHC. These experiments will have a fundamental impact on physics and technology for the next 20 years.

There are good reasons to expect that these new researches will have heavy quarks as well as tau leptons, the so-called third fermion generation, in the interesting events. These third generation objects are excellent probes to search for New Physics. Tracking devices, and in particular the Silicon devices that are becoming the preponderant tracking technology, play an essential role in the identification of the third fermion generation.

On the other hand the electronics required to process the signals from the detectors is taking a very important role, and it must be state of the art. The most interesting processes are very rare and hidden in an extremely large level of background. Implementing the most powerful selections in real time is therefore essential to fully exploit the physics potential of experiments where only a very limited fraction of the produced data can be recorded. A drastic real-time data reduction must be obtained. This makes on-line event reconstruction a critical component at any hadron collider experiment. The trigger must be extremely intelligent and powerful. A multi-level trigger is an effective solution for an otherwise impossible problem at LHC. The level-1 (L1) trigger is based on custom processors and reduces the rate from 40 MHz to ~100 kHz . The level-2 (L2) is based on standard CPUs. The L2 output rate is ~1 kHz. The Level-3 (L3) selection, called Event Filter at Atlas (EF) is performed by CPU farms, which write to tape about 100 events/s (at LHC L2 and L3 are also called High Level Trigger, HLT). The proponents of this project are and have been active essential participants of all these events. With this project we hope to directly address the main technological challenges of hardware, software and data analysis necessary to identify heavy flavour objects and jets with a tau lepton. The high-occupancy environment at the LHC and even more at the SLHC, will require a huge computing power to reconstruct so complex events. Addressing the challenging physics goals at the terascale requires a high degree of sophistication from the detectors and significant technological breakthroughs especially in: (a)Sophisticated triggering and real time processing; (b) Use of very deep sub micron electronics.

The first important goal of this project is the *realization* and *optimization* of the Associative Memory (AM) system to make it work in the FastTracker (FTK) processor for the Atlas experiment at LHC and its evolution for new applications. FTK is a high-performance "super-processor" based on the combination of two innovative technologies: powerful FPGAs (Field Programmable Gate Arrays) working with standard-cell ASICs (Application-Specific Integrated Circuits), the Associative Memory (AM) chips, for utmost gate integration density. Optimal partitioning of complex algorithms on a variety of computing technologies has been already proved to be a powerful strategy (see next paragraph), which turned the past hadron collider experiment CDF at the Tevatron accelerator in the Fermilab Laboratory, Chicago (USA) into a major player in the field of B-physics, on par with dedicated experiments operating at e+e- colliders.

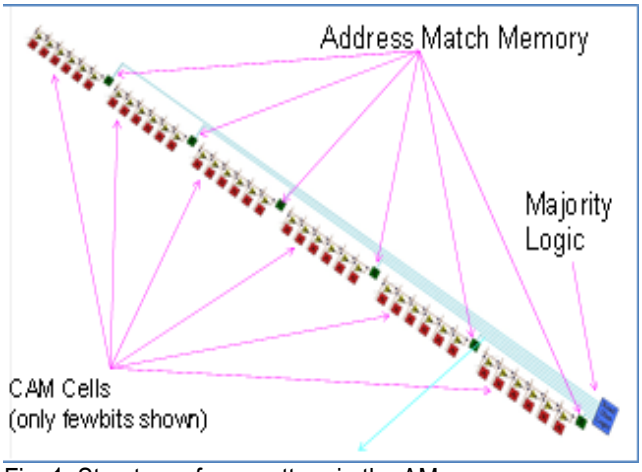

Fig. 1. Structure of one pattern in the AM

The key role in the novel technology is played by the custom multicore Associative Memories (AM) that is intensively used to filter out the relevant information of the data to be further processed by Field Programmable Gate Arrays (FPGAs) executing higher level algorithms. The AM implements the maximum parallelism and offers the best timing performances, since it solves its task in the time data are loaded on it.

Here is described the **key innovative**

conceptual and design difference between the AM and commercially available Content Addressable Memories (CAM). In the AM each pattern is stored in a single memory location like in the commercial CAM, but differently from the CAM, it consists of N independent words of M bits each. Figure 1 shows the structure of one pattern, that is one AM location. Each word refers to a particular item to be identified in a flux of data that is private of the words that occupy that position in the pattern. In fact data are sent on N parallel buses, one for each word of the pattern. Each word is provided with reserved hardware comparators and a match flip-flop. All words in the AM can make independent and simultaneous comparisons with the data serially presented to its own bus. Any time a match is found, the match flip-flop is set. A pattern matches when a majority of its flip-flops are set. This is promising for unstructured data processing.

Additionally the FTK architecture benefits from the FPGA computing power to eliminate the main drawbacks of AMs. In fact the AM does not scale to large image sizes having high resolution, so the AM performs a first low resolution filtering function. The FPGA complements the AM task with its flexibility and configurability, adapting its logic to perform any necessary “refining processing” of the low resolution AM result. In addition the AM has a specific architecture that helps to identify not only perfect features, but also partial, or noisy versions of them. The FTK architecture is actually subdivided into 2 sequential steps of increasing resolution. In step 1 the dedicated VLSI device, the AM, finds track candidates with low spatial resolution, called roads. In step 2, the real tracks are searched within the roads and fitted to determine their parameters with the best. Tracks with PT>1 GeV/c are finally selected to tag secondary vertexes or to search for hadronic taus or to perform high quality track-based isolation of muons, electrons and gammas.

The AM performs the most CPU intensive part of the pattern recognition, exploiting dedicated highly parallel structures. It exploits the idea of a pattern matching algorithm based on pre-calculated and stored track candidates, which are compared in parallel with the actual event. It has to solve a very difficult problem since the silicon detector has millions of channels and the number of track candidates is very large (~10**9). For this reason a high density dedicated chip has been developed for the AM.

FPGAs execute important pre/post processing functions, complementary to the intensive pattern-recognition performed by the AM. Pre-processing corresponds to (a) cluster finding in the silicon data, performed by ATCA boards called Data Formatters (DF); (b) smart database for immediate retrieval of full resolution detector clusters associated to roads found by the AM, performed by Data Organizers (DO). Post-processing includes (a) the track fitting performed by Track Fitters (TF) and (b) duplicate-track cleanup performed by the Hit Warrior (HW). The most important function is the track fitting, which refines the candidate tracks in order to determine the track parameters with the full silicon detector resolution. The TF makes use of methods based on local linear approximations and learn-from-data techniques for online misalignment corrections. The fit calculation consists of many scalar products, easily packed inside FPGAs. The approximations introduced to maximize the speed do not significantly affect the fit performance.

Maintaining the FTK dual structure based on the cooperation of VLSI dedicated AM and programmable FPGAs, the future FTK plan includes R&D for achieving further technology performance, miniaturization and integration of the current state of the art prototypes to fully exploit new applications within and outside the High Energy Physics field. We plan to associate an FPGA to each AMchip. The FPGA will control, configure and handle the AM providing the flexible computing power to process the shapes selected by the AM. The goals of this new elementary unit made of 2 chips are (a) maximum parallelism exploitation, (b) low power consumption, (c) execution times at least 1000 time shorter than the best commercial Control Processing Units (CPUs) performing the same task, distributed debugging and monitoring tools suited for a pipelined, highly parallelized structure, high degree of configurability to face with the best efficiency different applications. The standard FTK limits will be solved by the higher FPGA parallelism, like for example the FPGA bottlenecks for certain applications, in particular when the AM chip low resolution causes a high rate of fakes and an overload for the high resolution FPGA work. The best solution that we want to investigate today is the multi-packaging of the FPGA and the AM-chip in the same package. This objective will be achieved by using the new FTK ASIC prototypes in 65 nm VLSI-technologies (Very Large Scale Integrated Technologies). The new chip will count with serial buses for all data paths and will allow the storage in the memory bank of 128 Kpatterns per die. We also have a very interesting offer from Xilinx for Kintex bare dies that can be fit in the same package together with the AMchip, communicating mainly through high speed serial links. All the FTK functions (pattern matching and pre/post processing functions) will be squeezed in a single chip (SIP: System in Package)! These new elementary Units could be clustered on small boards, joined by an Ethernet switch or inserted on a PCI express bus, or integrated in the very powerful ATCA technology.

- ***Interdisciplinary and multidisciplinary aspects of the proposal***

There are important reasons, outside HEP, for the research proposed in the present program. Our approach to use powerful modern electronics is extremely flexible and its spread outside the realm of HEP would be extremely beneficial. The strategy of the "optimal mapping of a complex algorithm in different technologies" is a general approach that can speed up enormously any calculation by providing a high degree of parallelism.

Handling complex electronics components (dedicated AM chips and FPGAs) is less straightforward than programming a multi-core CPU, since it requires availability of FPGA hardware and knowledge of computer-aided-design (CAD) tools. For this reason we think that the HEP development in this area is important to show the potential of these devices and to spread the skills needed to use them with top efficiency. There are already examples showing that the use of a tuned combination of CPUs and FPGAs could expand not only in physics experiments, but also in other academic and even non-academic fields, for example in financial applications. The “Workshop on High Performance Computational Finance” is an instance of the many occasions for discussing FPGA acceleration techniques in the financial domain.

These techniques could be very important in the area of medical imaging for real-time diagnosis, when the patient is under examination. The computing power is a limiting factor for some high quality applications. High-resolution medical 3D image processing, for example, demands enormous memory and computing power.

The same approach could be very incisive for astrophysical and meteorological calculations, for robotic automation, and for security applications.

It could be essential for neurophysiologic studies of the brain. Recent advances in ICT and neuroscience allowed to study and model “in silico” a significant part of the human brain. The brain is certainly the most complex, powerful and fast processing engine and its study is very challenging. Understanding how the brain processes information or how it communicates with the peripheral nervous system (PNS) could provide new potential applications, new computational systems that emulate human skills (e.g. by using the directed fusion of diverse sensory information) or exploit underlying principles for new forms of general purpose computing. Significant improvements could be gained in terms of performance, fault tolerance, resilience or energy consumption over traditional ICT approaches.

The use of the associative memory processor for brain studies is particularly fascinating. The most convincing models that try to validate brain functioning hypotheses are extremely similar to the real time architectures developed for HEP. A multilevel model seems appropriate also to describe the brain organization to perform a synthesis certainly much more impressive than what done in HEP triggers. The AM pattern matching has demonstrated to be able to play a key role in high rate filtering/reduction tasks. We can test the AM device capability as the first level of this process, dedicated to external stimuli pre-processing. We follow the conjecture of reference [Punzi & Del Viva (2006) Visual features and information theory JOV 6(6) 567]: the brain works by dramatically reducing input information by selecting for higher-level processing and long-term storage only those input data that match a particular set of memorized patterns. The double constraint of finite computing power and finite output bandwidth determines to a large extent what type of information is found to be “meaningful” or “relevant” and becomes part of higher level processing and longer-term memory. The AM-based processor will be used for a real-time hardware implementation of fast pattern selection/filtering of the type studied in these models.

The second row of figure 2 shows the quality of the image when filtered accepting only the “good patterns” stored in the AM. The image edges are clearly detected and maintained, even if the information is reduced to the 5% of the original content. We could apply this filtering function to medical images, to extract the salient features and apply after fast but complex reconstruction algorithms to them. We would measure the extracted features in a very short time and automatic fashion providing a computer-diagnosis. The reduction of execution time of image reconstruction to be applied after the AM filtering function, would exploit the computing power of parallel arrays of Field Programmable Gate Arrays (FPGAs) as we do in FTK to find clusters of contiguous pixels above a certain

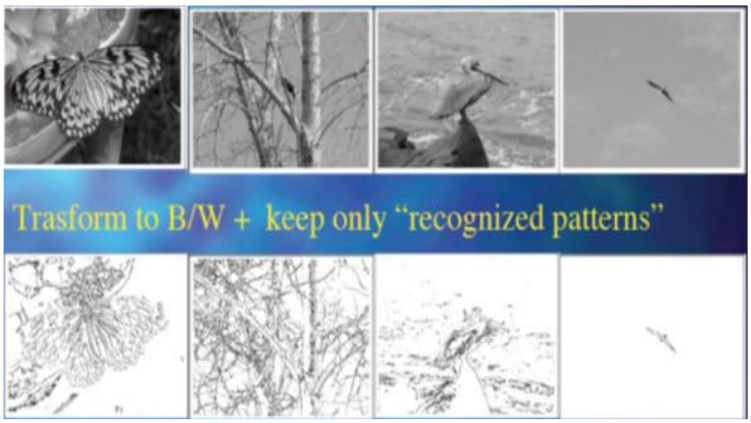

Figure 2

programmable threshold. Producing measurements that characterize their shape, we can measure quantities of interest in medical applications like the size of the found spots, how circular or irregular the spot is. The algorithm can be extended to 3-D images.

- **Appropriateness of research methodology and approach**

The FTK team's major tasks are to complete component design, test each board independently, test each board with those boards to which it communicates, integrate the board types and carry out global integration, and prepare a system for data taking in 2015.

Dedicated trigger hardware usage has been recently reduced at LHC, in favor of large, commercial CPU farms to reduce the risks associated with dedicated hardware, often considered powerful but difficult to commission, upgrade and inflexible. However the use of FPGAs and ASICs do not suffer from these disadvantages if the design and the commissioning are pursued with the correct methodology. FPGA flexibility allow rapid system improvement since the same hardware can be reused, just developing new firmware. The FTK commissioning can take place while the experiment takes data. A very careful test procedure can be devised to reduce to a negligible level the commissioning impact on detector operation and functionality. Each new board has to be fully tested first at home, after that on real data, using a parasitic connection to the experiment, before being included in the real ATLAS data taking stream. We have a specific test stand on the experiment where data can be spied and used to test the new prototypes before being added to the standard TDAQ operation. We call it the *Vertical Slice*, since it uses data from a very thin portion of detector, but it is complete from its front end to the Level 2 CPUs. The chosen procedure shows that the high degree of organization and standardization allows many successful migrations to different configurations in very short times and in a smooth way.

In addition to this activity (certainly the most important at least in 2014-2015), the FTK group will pursue the development of further integration concepts to increase "*power and degree of parallelism*" of the system, without increasing "*size and consumption*", thanks to a ***miniaturization*** process that will increase the logic density.

The specific methodology for the APIMAP project is described for the 3 main objectives of my work (see section B4): (A) FTK algorithms design development and optimization; this will be achieved in particular through firmware optimization and tests in a standalone test stand (B) participation to integration/commissioning; development of firmware and software for management, monitoring, diagnostics and control of FTK. This will concern first of all the activity on the Vertical Slice and in a second period the commissioning of the FTK Demonstrator that in 2015 will take data for the first time in the central part of the detector. Finally, (C) exploration and development of Associative Memory applications outside HEP.

(A) A large effort is required to optimize and standardize the architecture as much as possible and to produce the needed firmware and software for extensive tests of the hardware and firmware. I will focus mainly on the pre/post processing functions, which require high data throughput and extreme performance to be taken from latest generation FPGA devices. In particular the optimization will involve both the commissioning and R&D activities: (a) the 2-D clustering algorithm on pixel data for the 2015 commissioning; (b) the firmware of the Kintex FPGA that will be directly connected to a single AMchip to provide all the necessary ancillary logic (DO, TF functions, in addition to control, configuration) for the miniaturized FTK (FTK SIP).

(B) I will work on the monitoring components of the FTK system. Monitoring is critical for such a data intensive application. Monitoring requires special buffering in order to be able to trace the errors of synchronization on inputs. I will develop the monitoring modules necessary for the DF, DO and TF modules and I will assist in the monitoring system development for the complete system.

(C) I have a strong background in developing high performance image processing modules on FPGA devices (see Section B3). This experience will be put into good use in the research exploration process to find new applications for the pattern matching capabilities of the Associative Memory chips (see the work plan in the Secion B4).

- **Relationship to the 'state of the art' of research in the field**

The CDF experiment at Fermilab was the best of the state-of-the-art for triggering at a hadron collider. It had a very strong tradition in this field, since a large part of the trigger was implemented with dedicated hardware, and has been operational for many years, constrained to work within very short latencies (few μs). It has been upgraded several times during the 20-year life of CDF, to exploit technology advances. It has been equipped with power ful tracking processors at L1 (the L1 eXtremely Fast Tracker, XFT) and L2 (the Silicon Vertex Tracker, SVT). SVT was the most powerful trigger processor operating at a collider experiment so far and it is a perfect baseline for our project. My scientist in charge was part of the team that had a leading role in its design,

construction, commissioning and management. SVT performed online track reconstruction in the silicon detector (SVX) and the central drift chamber (COT) with sufficient accuracy, almost the offline resolution, to identify tracks from b-quark decays by their large impact parameters (IP>100 μm). SVT has been essential for the Bs mixing frequency measurement, the rare B-decay searches (B0s->mu mu), the observation of heavy baryons (Sigma_b and Sigma_b*), the first observation of the rare charmless decay modes of the B0s and Lambda_b, the search for CP violation in D0->hh di-hadron decays, and the evidence for charm mixing. These extremely challenging measurements would have been completely out of the CDF reach without the SVT. Since B-physics had a limited budget in terms of allocated trigger bandwidth, the better purity allowed CDF to increase by several orders of magnitude its efficiency for the hadronic B decay modes. Trigger selections based on the reconstruction of secondary decay vertices allow collecting otherwise inaccessible hadronic decay modes. The availability of the hadronic decay modes at CDF determined the quality of the CDF B0s mixing measurements. Also for high-PT physics CDF has demonstrated the possibility of successfully using purely hadronic channels in the study of the top quark, in Higgs searches, and even in the reconstruction of the Z0 boson, thanks to the secondary vertex b tagging. The AM was already the central device of the SVT system at CDF.

Triggering at a hadron collider is a field where the speed and the high parallelism of both the AM and CAM devices have been extremely successful. Pattern matching has been adopted in different ways, depending on the trigger level where it was used. Commercial CAMs have been used in the H1 experiment at the unique positron-proton collider HERA, hosted by DESY in Hamburg, Germany. Basically, each bit of a CAM word corresponded to a detector channel. The whole event, made of a single large word, had to be submitted to the memory bank at once, i.e. in the same clock cycle. In order to limit the number of channels to the largest CAM widths, usually smaller than 1000 bits, only a small detector section was analyzed. Detector data come in the form of a sequence of addresses of hit channels. Thus, additional hardware must reformat the incoming data before sending them to the CAM. When the used detector section is sizable, the number of bits per word becomes prohibitively large for this method. Here comes the major difference between the AM and the CAM. In the AM each pattern is also stored in a single memory location, but it consists of N independent words of M bits each (see figure 1 description). This structure allows applications to modern complex detectors.

- **Originality and innovative nature of the project**

FTK was so innovative that the group needed 15 years to convince the ATLAS community to adopt it.

The very precise silicon detectors used at LHC, which contain hundreds of thousands or millions of channels, raise the problem of the complete tracking of large numbers of high multiplicity events. With tens or hundreds of particles produced by multiple primary collisions and traversing several detector layers in all directions, this is a formidable challenge even for the off-line analysis. The feasibility of a complete high-quality tracking for real time event selection has been considered impossible in large experiments at very high rates. Without FTK, real-time tracking is performed in a limited detector region or on a small subset of events, selected previously using other detectors.

The innovation for the high event rate real time tracking at hadron colliders is mostly based on the possibility of the selection of events with b quarks and taus in the trigger. Historically, these events were selected based on lepton identification. Trigger selection based on the specific track configuration inside the jets opens up the possibility of studying the hadronic decay channels of heavy fermions, inaccessible to lepton methods. High trigger efficiency for these processes requires sensitivity to the generic hadronic decays of the heavy fermions. The challenge comes from the enormous background from QCD produced light quark and gluon jets, which can be suppressed using tracking. Tracks coming from a secondary vertex or not pointing to the beamline identify b quark jets, while τ jets can be separated from background using the number of tracks within a narrow cone and the number in a larger isolation region.

FTK really will change radically the ATLAS trigger menu, enlarging the physics capability. High performance of dedicated hardware and flexibility of general purpose CPUs are obtained through the use of programmable devices. Three key features allow FTK to carry out its job in few tens of microsecs: a highly parallel and pipelined architecture, custom VLSI pattern recognition, and a linear track fitter implemented with FPGA technology,

- **Timeliness and relevance of the project**

Finally in June 2013 the FTK TDR was submitted and unanimously approved by ATLAS. In 2015 the FTK Demonstrator has to take data for the first time, to produce the first important results.

This is an important and exciting time to collect the fruits of so many years of efforts. We need to demonstrate to the high energy community the capability of the FTK online tracker. The very precise LHC silicon detectors, which contain hundreds of thousands or millions of channels, increase the problem of complete tracking in large numbers of high multiplicity events. With tens or hundreds of particles produced by multiple primary collisions and traversing many detector layers in all directions, this is a formidable challenge even for off-line analysis. The feasibility of complete high-quality tracking for real time event selection has been considered impossible in LHC experiments at very high rates. As a consequence, real-time tracking is planned for a limited detector region or on a small subset of events, selected previously using other detectors. Many physicists dismiss the possibility of complete on-line tracking in LHC experiments because they see the problem as too formidable. The goal of this research is to change this opinion by demonstrating that up-to-date technology, exploited with suitable organisation and algorithms, permits the development of high-performance tracking triggers sensitive to secondary vertices and complex structures like taus.

The FTK strategy has a particularly relevant impact now that the LHC community is starting to consider the design of new architectures for the SLHC upgrade. The CDF experience with data, in particular the online tracking at CDF and the FTK R&D project, could have a significant impact on the discussion of future architectures.

- **Host research expertise in the field**

Istituto Nazionale di Fisica Nucleare (INFN). INFN studies the fundamental constituents of matter, and conducts theoretical and experimental research in the fields of subnuclear, nuclear, and astroparticle physics. Fundamental research in these areas requires the use of cutting-edge technologies and instrumentation, which the INFN develops in its own laboratories and in collaboration with the world of industry. INFN works in close collaboration with the academic world. It is a major player in international HEP research and has a particular impact in hadron collider physics: it strongly contributes to all LHC experiments and has been member of the CDF experiment since 1980, having played a particularly important role in the SVT project. The idea of real-time b-quark selection in the CDF experiment was born in 1985 inside INFN by Prof. Luciano Ristori and Mauro Dell'Orso (see L. Ristori, M. Dell' Orso, "VLSI Structures for Track Finding" Nuclear Instrument and Methods in Physics Research, Volume A278). Ristori was awarded the 2009 Panofsky prize of the American Physical Society. The FTK idea for LHC was born in INFN in 1998 by Paola Giannetti, my scientist in charge. Mauro Dell'Orso is the international coordinator of the IAPP FTK project 324318 funded by FP7. INFN had a leading role in the CDF b-quark trigger definition and evolution and finally in the CDF B-physics analyses. The group created in Pisa (which included Mauro Dell'Orso and Paola Giannetti from the beginning) around the Associative Memory main idea proposed SVT at CDF and its upgrade. The experience gained during the development and construction of the AM device in Pisa at the beginning of the 90's ("The AMchip, a Full-custom CMOS VLSI Associative Memory for Pattern Recognition", IEEE Trans. On Nucl. Sci. Vol 39, N4, 1992) was a very important step toward further development. It was the starting point for the following studies on different technologies: (a) FPGA technology used for a user-friendly, low-density associative memory ("A programmable associative memory for track finding" NIM A, Volume 413, 1998); (b) third generation standard cell technology AM. The Pisa group also managed the AM chip and the board production for SVT and its upgrade. They managed the production and assembly of hundreds of boards and thousands of AMchips. The gained experience is not limited to the AM device. Many different 9U VME boards were developed, strongly based on the use of FPGAs and Complex Programmable Logic Devices (CPLD). Pisa has studied the density, complexity, and performance of these devices for many years, following an evolution that is well beyond the limits imagined just a few years ago. Pisa prepared the test procedures to validate the chips and the boards and performed the tests on the boards. Pisa installed the system at Fermilab and developed the software for its management, monitoring and diagnostics. The group developed the physics case for the SVT proposal and a realistic simulation of the system to be able to predict the SVT capabilities to produce B-physics results. The performance of the system was as good as expected from the simulation. SVT was installed efficiently and without particular problems. The original SVT has taken data since the year 2000. Pisa participated actively in the data taking, the b-quark trigger definition and evolution and finally the B-physics analyses. In conclusion, the group had a dominant role in b-quark physics at the Tevatron and in the related technologies. It has vast experience in all phases of this project.

- **Quality of the group/scientist in charge**

The FTK Pisa group is leaded by dr. Paola Giannetti and prof. Mauro Dell'Orso.

Supervisor- The fellow supervisors at Pisa, dr P. Giannetti is Director of Research since 2002.
Here is a short summary of the projects she proposed and leaded:

1. The FTK processor for LHC experiments; she was the project leader in the 1999-2001 of the INFN funded FTK R&D project.
2. Three trigger upgrades at CDF (2002-2008); she was responsible of INFN funds for them:
   - the SVT upgrade,{ "The Silicon Vertex Trigger upgrade at CDF", Nucl. Instrum. Meth. A572, 361 (2007)
   - the calorimetric trigger upgrade {"The CDF level 2 calorimetric trigger upgrade". IEEE Transaction on Nuclear Science, Volume 56, Issue 3, pp 1685-1689, 2009 }
   - the Gigafitter for online tracking. as upgrade of the Track Fitter {"GigaFitter: Performance at CDF and perspective for future applications", Nucl. Instr. and Meth. A, vol. 623, pp. 540-542, 2010.}

Today she is the FTK deputy project leader at ATLAS and responsible of INFN funds (2008, 2012]).

Prof. M. Dell'Orso, is full professor at the University of Pisa since 2010. His Research activity is shortly described:
1987-11: CDF analysis – Development and construction of SVT, the on-line tracker for CDF
SVT upgrade for the high luminosity (with P. Giannetti).
1999-02: The R&D FASTTRACK experiment, funded by INFN; study and prototype construction of a Fast Tracker, a processor for on-line tracking at high luminosity colliders, suitable for the CERN-LHC experiments (with P. Giannetti).
2002-10: Study and proposal of FTK, an on-line tracker at ATLAS (with P. Giannetti, M. Shochet).
2003-05: Manager of the Pisa Research Unit for the project named "Automatic pattern recognition for experimental physics", within the PRIN-2003 "Tools for selection and analysis of rare events for the new generation of Astroparticle and Fundamental Physics experiments" coordinated by L. Peruzzo.
2006-08: Manager of the Pisa Research Unit for the project named "Gigafitter: a processor for ultrafast reconstruction of complex events in Experimental Physics detectors", within the PRIN-2005 "Study and development of new modular techniques for the selection and the acquisition of events in Particle and Astroparticle Physics" coordinated by L. Peruzzo.
2006-2009: Contributions to the SLIM5 R&D experiment, funded by INFN; development of silicon detectors with low material interaction and integrated systems for on-line track reconstruction, suited for B-factories ,
2010-today: Construction of FTK, a processor for the on-line track reconstruction at ATLAS (with P. Giannetti, Y.K. Kim, M. Shochet).
More coordination activities:
1992-94: Member of the National Committee for Computing of the Istituto Nazionale di Fisica Nucleare (INFN).
2000-06: Member of the National Scientific Committee for Particle Physics of the INFN and local Coordinator of the Group I experiments of the INFN-Pisa (ALEPH, ATLAS, BABAR, CDF, CMS, NA48, KLOE, MU->E+GAMMA).
2009-today: Member of the European Committee for Future Accelerators (ECFA).
2011-today: Chair of the Physics degree courses at the University of Pisa.
2013-2016 Coordinator of the FP7-People-2012-IAPP 324318 FTK project funded by the European Community.

Both Mauro Dell'Orso and Paola Giannetti have been CDF members from the beginning, participating mainly on trigger and physics studies. They were leading actors in the SVT project and its upgrade. The particle physics returns of their work include the top quark discovery and an accurate measurement of its mass, precision measurement of the W boson mass, Bs mixing frequency measurement, precision measurement of many b hadron lifetimes, and many of the most stringent limits on nonstandard processes. The complete CDF RUN physics archive is a collection of published papers ranging over the full state of the art in hadron collider physics. Now they are in ATLAS with a key role in the FTK project.

More than 50 students got their Master/Laurea and PHD working on our real time tracking projects and related physics, under the supervision of the SVT/FTK Pisa group, finding after that interesting positions in european-USA institutions or industries. We report here few examples: (1) A.Annovi (physicist), Laurea&PHD with Pisa 2004 "Hadron collider physics with real time trajectory reconstruction" now staff at Frascati Laboratory (Italy), was "project leader" of the SVT upgrade and is now responsible of the integration of FTK in the ATLAS TDAQ. (2) A. Cerri(physicist), Laurea&phd "Study of trigger with secondary vertexes at CDF"- now Lecturer at the

University of Sussex (UK), working on hardware online tracker for the ATLAS Level 1 trigger. (3) M.D'Onofrio (physicist), Laurea 1999,"The Higgs in hadronic events Htt" – now staff at the University of Liverpool.(UK), (4) Francesco Crescioli (physicist), Laurea&PHD with Pisa 2004 "GigaFitter at CDF: Offline-Quality Track Fitting in a Nanosecond for Hadron Collider Triggers" now staff at LPNHE, Paris (France). (5) P. Giovacchini, (engineer), Laurea 2005 "Design & test of a standard cell associative memory for the Silicon Vertex Tracker of the CDF experiment" – now at STMicroelectronics Srl, Milan. (6) One more engineer (Michele Lamalfa) and physicist (Barbara Simoni) working with us have found a permanent position at STMicroelectronics, Milan .

B2 Training (maximum 2 pages)

- **Clarity and quality of the research training objectives for the researcher**

Training objectives of the proposal

I expect to realize a list of important goals in my training at INFN. I expect to learn:

- Very advanced use of programmable logic (FPGAs). High level firmware development (VHDL and Verilog description language), simulation & test capabilities, timing & implementation optimization.
- "Cost versus performance" evaluation and comparison of different technologies: VLSI devices, FPGAs, commercial CPUs.
- Familiarization with the latest generation of FPGA devices (e.g. Xilinx 7th generation FPGAs).
- Grand scale parallelization techniques on chip level, board level, system level.
- Understanding of the ATLAS online/offline tracking system problems, relative solutions and standardization of the system to be able to transfer the best of this technology to the future. Capability to improve flexibility and ease of use for the trigger devices, to allow application to different experiments with minimum tailoring and minimum engineering effort.
- Familiarization with the Experimental High Energy Physics involved in the ATLAS trigger.
- Capability to realize new triggers exploiting the hardware upgrades.
- Knowledge of trigger selections and study of their dependence on the accelerator luminosity. Understanding of bandwidth and processing problems. Optimization of efficiency and rejection power of the selection.
- Realization of simple expert systems to monitor and find problems in the system.
- Exercise automation of technological follow-up of digital electronics developments, producing clean project descriptions by high level languages and automatic compilation into the most advanced devices at time of construction. This will simplify further developments and applications to future experiments.
- Participation to the commissioning of the FTK in ATLAS
- Capability to adapt the experience gained on "supercomputers" developed for HEP to pattern recognition problems outside HEP, such as medical imaging.
- Representing the collaboration in meetings, workshops and conferences.
- Supervising graduate student theses and participating as an instructor in FTK collaboration schools.

As has been described in section B1 the Pisa group, which I will be able to join with the IEF fellowship, developed a vast experience in all the areas where I expect to learn and exercise my trainings. Not only the Pisa group built and used SVT at CDF, but also was the main proposer and pusher for the FTK use at ATLAS. Pisa is the ideal place to learn all what I list above.

Objectives beneficial for the development of an independent research career

This above training will allow me to acquire expertises that will make me important inside the FTK project and all the new future applications of the AM technology. As an expert I will be able to manage research groups working on the future development of the FTK system not only in the University of Thessaloniki, where I come from, but also in other collaboration partner's groups. I will be able to reinforce the FTK activity: with my own group I will organize developing, testing and operation monitoring of new evolutions of the AM system.

- **Relevance and quality of additional research training as well as of transferable skills offered with special attention to exposure to industry sector**

INFN and especially the Pisa Section is a great intellectual community, enormously stimulating in many different fields. It's close connection with the University of Pisa, Scuola Normale and Scuola Superiore Sant' Anna means that it is very easy to attend at seminars and classes of extremely high interest and quality. As my current background is in electronics, not mainly in HEP, I will be able to take courses in both the University and Scuola Normale to enhance my Experimental High Energy Physics knowledge. Training and courses are also offered for

computing, electronics and other skills, including management.

I will be able to exercise my teaching/mentoring capabilities participating to the management of young people in the FTK group, in particular students performing their thesis, and participating as organizer to the outreach activities of the IAPP project (schools, workshop and IAPP days, trainings offered by Pisa and CAEN partners).

There are international advanced courses in Scuola Superiore Sant' Anna in the field of ICT and embedded systems which I will be able to follow to enhance my already good knowledge of embedded systems.

A large number of experiments (CDF, Babar, Atlas, CMS, LHCb, Epsi, Kloe, MEG, TOTEM….) are present in Pisa and share experiences and structures. In Pisa there is a very large clean room where important components for detectors for HEP and astrophysics where made.

The University of Pisa was founded in 1343 and has had significant historic figures for physics as students and professors, from the historical figure of Galileo Galilei to Nobel Prize winners Enrico Fermi and Carlo Rubbia. It has 20 departments, 71 graduate programmes, 19 doctoral programmes and 68 third cycle specialisation programmes. More than 1500 people work in teaching and research and about the same as technical and administrative staff. The university branches from basic research to technical branches and classical studies, historical, philosophic and economic-juridical subjects, from sociology to psychology, from communication sciences to medicine. The university supports a number of spin-off companies in multiple disciplines such as IT, materials, communications etc. The Department of Physics has strong research groups in nanomaterials, non-linear phenomena, laser cooling and matter waves, metrology, spectroscopy, astronomy and astrophysics and applied physics. It strongly supports collaboration by organizing workshops where all members of the department present their work to their associates, the students and the community. The Department of Physics in Pisa currently ranks 42nd in the QS World University Rankings by Subject and the highest ranked Physics Department in Italy.

The FTK group in INFN Pisa has strong collaborations with the electronics industry. Two companies participate to the FTK tests, production and commissioning: the Italian CAEN and the Greek PRISMA Electronics. Both these companies had a wide experience in developing instruments and electronics devices for high energy physics. They had an important role in the development of the readout and power supplies for the LHC detectors. The researcher will have the occasion during his fellowship to collaborate with them as most boards will be designed, tested in Pisa, and learning about the companies' organization and working style.

Pisa will also be ideal to participate to FTK outreach activities since Pisa is the coordinator of the IAPP FTK project, that has industry partners, outreach and dissemination clear duties.

- **Measures taken by the host for providing quantitative and qualitative mentoring/tutoring**

I had the occasion to work in Pisa as seconded researcher in the IAPP FTK project. The work style in INFN is wonderful. Organization and continuous scientific discussions are the bases of the high research productivity of the relatively small, but excellent research groups. Each member has individual responsibilities and is required to discuss her/his work weekly with the rest of the group. Seminars in front of the whole scientific community of the institute are periodically required. This style is a strong stimulus to acquire clarity, independence, management capability, and presentation skills. The strong communication/discussion between all group members, provides a continuous stimulus to improve "leadership capability".

The FTK group is very well organized even if spread in the world. The tasks are clear and assigned to each separate researcher. There are weekly meetings for each assigned task where all participating researchers are included from all the involved institutes with remote access if required. In these weekly meetings the progress of each researcher's work is reported and the work assignment is adjusted accordingly. There is strong support when a problem appears within the project and assistance is available by the whole group if required. The support derives from the deep theoretical background of the group as well as the strong technical competence of its participants. The researchers are strongly encouraged to promote their work by participating in conferences and writing papers for internationally accredited journals. Mobility is available when required by the researcher and the project within all member institutes of the collaboration

B3 Researcher (maximum 7 pages which includes a CV and a list of main achievements)

- **Research experience**

My research field is development of high performance FPGA implementations, specializing on multiprocessing systems and parallel implementations. My experience covers a variety of fields: from development high resolution real-time image processing implementations to the development of integer linear processing models for design space exploration of multiprocessing implementation targeting but not restricted to FPGA systems.

A) As a PhD candidate and researcher in the Aristotle University of Thessaloniki I participated in the Marie Curie IAPP project: "Fast Tracker for Hadron Collider Experiments". As part of this project I was seconded for four months to CAEN SpA in Viareggio, Italy. There I was trained on the FastTrack Processor System and I was assigned the task of designing the firmware for the 2D-clustering algorithm for the FTK Input Mezzanine board. During my secondment I had close cooperation with researchers from INFN, University of Pisa and CERN and successfully completed the design of a complicated clustering module and its decoding step.

B) I also participated in the "Corallia: Lab-On-Chip" Nationally Funded Project. The Corallia Clusters Initiative is the first organization established in Greece for the development and systematic management of innovation clusters and collaboration between industry and academia. The "Corallia: Lab-On-Chip" project was an industry-academia cooperation aimed to develop a system prototype for a molecular analysis instrument using microfluidic Lab-on-Chips. During this collaboration our team worked hand in hand with Micro2Gen Ltd. in order to successfully adapt a patented machine vision algorithm and implement it with real-time specifications on a Xilinx FPGA. The Machine Vision system was designed to identify and follow microfluidic flows on Lab-On-Chips of maximum size 12.7cm x 8.5cm with a maximum speed of 20 mm/sec in circular channels of a diameter of 200μm.

C) As part of my PhD research I did extensive design space exploration for multiprocessing systems specializing on FPGA implementations. I used a combination of General Processing Elements (Microblaze Soft Processors) and application specific hardware accelerators, experimented using local memory (on device block-RAMs) as well as external memory (on board DDR) and experimented with different interconnections between the processing elements: buses (such as PLB), and FIFOs. This exploration led to the development of an Integer Linear Processing model for the optimal resources allocation and application partitioning on FPGA-based hybrid multiprocessing systems.

D) I participated as a primary researcher in the European Funded project "Jewel: Jordan Europe Wide Enhanced research Links in ICT". The project aimed at the improvement of research in Jordan in the area of ICT with twinning activities between Aristotle University of Thessaloniki and Jordan University of Science and Technology. My role was to propose and supervise research assignments to post-graduate and undergraduate students and also participate in workshops as an instructor.

E) Before my PhD as a post-graduate student I was included in the latest stage of the ARISE project (as part of the Doctorate Thesis of Dr. N. Vassiliadis). The ARISE framework (Aristotle Reconfigurable Instruction Set Extension) introduced a systematic approach for extending once a processor to support thereafter an arbitrary number of hardware accelerators. These accelerators can be coupled following a co-processing computational model or extending the processor's data path as functional units and can follow a hybrid (both loose and tight) computational model. The framework extends one-time the Instruction Set Architecture (ISA) of the processor with eight new instructions to control the introduced Custom Computing Units (CCUs). The ARISE framework was prototyped on a XILINX FPGA using a MIPS processor as a GPP. My role was to profile the extensively used MiBench embedded benchmark suite on the MIPS processor in order to identify the computationally intensive functions and possible targets for CCU development. After choosing the JPEG benchmark as a target for my thesis, I developed an ARISE specific hardware accelerator for the IDCT function of the JPEG algorithm, integrated it in the framework and verified it by using software with the ARISE extensions and on the FPGA implementation.

Scientific/professional CV: - academic achievements – list of other professional activities – any other relevant information

Education:

- Bachelor Degree in Physics, Aristotle University of Thessaloniki (1999-2005) with a CGPA8.88/10 (Excellent) Honors Thesis: "Digital Adder Design with a Reconfigurable Clock", supervisor Prof. S. Nikolaidis

Scholarship from the Greek State Scholarship Foundation for excellence in the National Exams for Entrance in the Higher Education

- Masters Degree in Electronics, Aristotle University of Thessaloniki (2005-2008) with a CGPA: 9.08/10 (Excellent)
  Thesis: "Application Analysis for the Design of Specific Processors", supervisor Prof. S. Nikolaidis
  Distinction for achieving best evaluation in the accepted students for the post graduate programme

Other work experience:

- Teaching Assistant – to Associate Professor S. Nikolaidis (2010-2013):
  Electronics Lab, Department of Physics
  "Digital Systems Laboratory – Elements of Reconfigurable Logic" in the 3rd Semester of the M.Sc. in Electronic Physics
  Description: Programmable logic - FPGA structure, architecture, methodology of design, simulation and programming
  "Embedded Systems" in the 2nd Semester of the M.Sc. in Electronic Physics
  Description: Development of Embedded Systems using Xilinx FPGAs, EDK and SDK, Microblaze programming
- Sales Manager – Kinetix Tele.com (2006), wholesale trading of VoIP telecommunications to retailers in Europe and the Middle East
- Computer Instructor – Data Station (1999-2001)
  Instructor of computer programming (Pascal and Delphi) in closed groups of high-school and university students

Personal Skills and Competences:

- Scientific Workshop, "4th International School of Trigger and Data Acquisition," Thessaloniki, Greece, Aristotle University of Thessaloniki, February 1-8, 2013
- Microelectronics Support Centre Training Course on, "Digital IC Implementation and Sign-off (Using Cadence Tools)," Rutherford Appleton Laboratory, Harwell Campus, November 19-23, 2012
- Workshop on, "Organizing and Writing Research Proposals," Research Committee of Aristotle University of Thessaloniki, October 1-5, 2012
- IDESA Digital - Advanced Digital Physical implementation flow Seminar, Aristotle University of Thessaloniki, February 2009

Hardware Description Languages: VHDL

Computer Programming Languages: C/C++, Pascal/Delphi, Assembly

FPGA Experience: Spartan-3E, Virtex-5 (lx110t), Spartan-6

Electronic Design Automation Tools: Xilinx ISE Development Suite, Modelsim, Aldec Active-HDL, SPICE (H-P), Matlab, Cadence for Digital IC Design, NI LabVIEW

Systems: GNU/Linux, Windows from 3.1x onwards

- **Research results including patents, publications, teaching etc., taking into account the level of experience**

In the following I describe my specific activity during my PhD and the research projects I participated in:

A) During my secondment in CAEN SpA for the Marie Curie IAPP in the Fast Tracker for Hadron Collider Experiments project I developed the firmware for a 2D clusteringalgorithm to be executed on the data received from the pixel detector modules by the FTK Input Mezzanine board. This module is essential for the FastTracker as:
   a. it achieves a substantial data reduction for the input of the system, which is critical for the timing performance required for the ATLAS experiment.
   b. it improves the measurement of the position where the particle has crossed the pixel module.

   The clustering module takes input for the ATLAS detector pixel modules and uses a moving window technique to identify the clusters. The size of the window is 8x21 pixels (21 for the r-phi direction and 8 for the z or eta direction). When implementing a window size of 8x21 pixels a 1% FPGA area was used (slice registers usage) on a Spartan 6 lx150t FPGA device. For the same device and a realistic hit occupancy an average of roughly 8 clock cycles per hit computation time was estimated, using a post-place and route

simulation with a 12ns clock. As an input step for the clustering module I also designed a decoder module. The decoder realigns the received hits from each pixel module, because half of the front end chips of the ATLAS pixel modules are read out in the reversed order, detects and compensates for possible errors in the control word sequence and also generates separate streams of pixel module data so that more than one clustering modules can operate in parallel. The results of this work have been accepted for publication in a, b and c.

B) In the "Corallia: Lab-On-Chip" project I participated in the design of a Machine Vision system for flow detection in microfluidic Lab-on-Chips. The system was designed for a real-time response to a 1Mpixel camera with 60fps rate. For this project I worked on the adaptation of the patented machine vision algorithm (provided by Micro2gen), the production of the equivalent C source code for the verification, the development of a Canny Edge Detection implementation, the Flow Detection components (including the center of mass calculation, the median filters and a flow proximity detector) and the verification of the complete system. The system prototype was successfully demonstrated in the project final audit. The results of this work were published in d, e, f, h and j and presented by me in conferences 2, 5 and 6.

C) During my PhD my research also included the development of an ILP model for the optimal resources allocation and application partitioning on FPGA-based hybrid multiprocessing systems. The ILP model uses as an input the application modeled as a directed acyclic graph where the nodes are application tasks and the edges are data transfers between tasks. The designer can set constraints such as maximum area, maximum number of processing elements, maximum execution time, maximum number of BRAMs and find the task allocation for one or a combination of optimization parameters (area, time, memory usage). This was the first ever proposed ILP model for MPSoC implementations that can combine these three optimization parameters. Since the modeling of the architecture and behavior of the processing elements and buses is not FPGA specific the model can easily be adapted to generic digital MPSoC applications, from ASICs to many core. The results of this work were published in g and i and presented by me in conferences 3, 4 and 6.

D) My participation in "Jewel: Jordan Europe Wide Enhanced research Links in ICT" project is described in the following Teaching Experience part.

Teaching Experience: I have extensive teaching experience from an early age. As an undergraduate I worked for two years for the private computer programming school Data Station where I taught computer programming languages (Pascal and Delphi) to classes of high school and university students. As a PhD candidate and teaching assistant I have assisted in the supervision of two post-graduate theses in embedded systems and one undergraduate thesis in FPGA design. I am currently assisting in the supervision of two more post-graduate theses on FPGA implementations. I have been a teaching assistant from the start of my PhD and have been teaching the FPGA part of the Digital Systems Laboratory on the 3rd semester of the M.Sc. in Electronic Physics, as well as part of the "Embedded Systems" course on the 2nd semester of the same Master's programme and the laboratory exercises which support it. During my secondment in CAEN SpA for the Marie Curie IAPP: Fast Tracker for Hadron Collider Experiments project I was the main VHDL instructor for the four day long "FTK Summer School for Training on VHDL and FPGA Implementations" held in the University of Pisa. The students of the school were under-graduate and post-graduate students, professional engineers with an interest in VHDL and researchers participating in the IAPP project who needed VHDL training for their future work.

I also acquired extensive teaching experience from my participation in the "Jewel: Jordan Europe Wide Enhanced research Links in ICT" project. For this project I was assigned the task of training the Jordanian students on FPGAs and Embedded systems. This included interaction through internet to give ideas for new projects and support the students when necessary. During the project I was an instructor for two workshops, one in Aristotle University of Thessaloniki and one in Jordan University of Science and Technology (5). During this workshops I taught an introductory course to semiconductors and one on FPGA design to a big university audience and supervised two laboratory exercises for FPGA and Embedded System Design in a laboratory class of more than 20 students.

I have been member of two workshop organizing committees (1, 3) and one National Conference of Electronics organized by my university (PACET 2012 - http://www.pacet.gr/). Twice I have been Session Chair (1, 3).

Publications:

a) **C.-L. Sotiropoulou**, A. Annovi, M. Beretta, P. Luciano and S. Nikolaidis, "A Multi-Core FPGA-based Clustering Algorithm for Real-Time Image Processing," to be published in the proceedings of IEEE-NSS 2013, COEX, Seoul, Korea

b) **C.-L. Sotiropoulou**, A. Annovi, M. Beretta, P. Luciano and S. Nikolaidis, "A Multi-Core FPGA-based 2D-Clustering Algorithm for High- Throughput Data Intensive Applications," to be published in the proceedings of ICATPP 2013, Como, Italy

c) G. Volpi, **C.-L. Sotiropoulou**, et al. "Design of a Hardware Track Finder (Fast Tracker) for the ATLAS Trigger," to be published in the Proceedings of TWEPP 2013, Perugia, Italy

d) **C.-L. Sotiropoulou**, L. Voudouris, C. Gentsos, A. Demiris, N. Vassiliadis and S. Nikolaidis, "Real-Time Machine Vision FPGA Implementation for Microfluidic Monitoring on Lab-on-Chips," in IEEE Trans. on *Biomedical Circuits and Systems,* IEEE Early Access, doi: 10.1109/TBCAS.2013.2260338.

e) L. Voudouris, **C.-L. Sotiropoulou**, N. Vassiliadis, A. Demiris, and S. Nikolaidis, "High-speed FPGA-based flow detection for microfluidic Lab-on-Chip," in *Proc. IEEE 20th Mediterranean Conf. Control & Automation (MED)*, pp. 1434-1439, Barcelona, 2012.

f) **C.-L. Sotiropoulou**, L. Voudouris, C. Gentsos, S. Nikolaidis, N. Vassiliadis, A. Demiris, and S. Blionas, "FPGA-based machine vision implementation for Lab-on-Chip flow detection," in *Proc. 2012 IEEE International Symp. Circuits and Systems*, pp. 2047–2050, 2012.

g) **Calliope-Louisa Sotiropoulou**, Spiridon Nikolaidis, "ILP formulation for hybrid FPGA MPSoCs optimizing performance, area and memory usage," *Electronics, Circuits and Systems (ICECS), 2011 18th IEEE International Conference on* , pp.748-751, 11-14 Dec. 2011

h) **Calliope-Louisa Sotiropoulou,** Christos Gentsos, Spiridon Nikolaidis, "FPGA-based Canny Edge Detection for Real-Time Applications," published at the 26th Conference on Design of Circuits and Integrated Systems (DCIS), Albufeira, Portugal, 2011.

i) **Calliope-Louisa Sotiropoulou**, Spiridon Nikolaidis, "Design space exploration for FPGA-based multiprocessing systems," *Electronics, Circuits, and Systems (ICECS), 2010 17th IEEE International Conference on* , pp.1164-1167, 12-15 Dec. 2010
(cited once – Scopus)

j) C. Gentsos, **C.-L. Sotiropoulou**, S. Nikolaidis, and N. Vassiliadis, "Real-time canny edge detection parallel implementation for FPGAs," in *Proc. 17th IEEE International Conf. Electronics, Circuits, and Systems*, pp. 499-502, 2010.
(cited five '7' times - Scopus)

k) **Calliope-Louisa Sotiropoulou**, Nikolaos Vassiliadis, George Theodoridis, Spiridon Nikolaidis, "JPEG Implementation Through Programming of an ARISE Machine," 1st Pan-Hellenic Conference in Electronics and Telecommunications (PACET 2009), Patras, March 2009.

Since July 2013 I am a member of the ATLAS-TDAQ collaboration author list.

Conferences-Seminars-Workshops

1) Scientific Workshop, "2nd Workshop on Modern Circuits and Systems Technologies," Thessaloniki, Greece, Aristotle University of Thessaloniki, February 1st, 2013
One oral presentation (substitute presenter) – Session Chair
2) 2012 IEEE International Symposium on Circuits and Systems (ISCAS), Seoul, Korea, May 20-23
Poster presentation
3) Scientific Workshop, "Modern Circuits and Systems Technologies," Thessaloniki, Greece, Aristotle University of Thessaloniki, March 16 2012
One oral presentation – Session Chair
4) 18th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2011, Beirut, Lebanon, December 11-14 2011
Poster presentation
5) Scientific Workshop, "Current Trends in Nanoscale VLSI Design," Irbid, Jordan, Jordan University of Science and Technology, October 24-27 2011
Instructor of 2 lectures and 2 labs, one paper presentation
6) 17th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2010, Athens, Greece, December 12-15, 2010
Two paper presentations
7) 1st Pan-Hellenic Conference in Electronics and Telecommunications 2009, PACET 2009, Patras, March 20-22 2009
Paper presentation

- **Independent thinking and leadership qualities**

Activities that reflect initiative, independent thinking, project management skills and leadership.- I always worked with a large degree of autonomy, from the beginning of my research activity.

During my thesis I worked on the ARISE framework with a great degree of independence. After doing an exploration and profiling of the available benchmark algorithms I chose the most suited to implement as an example, as well as the strategy and approach for the implementation.

As a PhD student, during my work on the Integer Linear Programming model I worked completely independently, choosing the algorithms of interest and the mathematic approach on the problem.

For my work on the "Corallia: Lab-On-Chip" project I was part of the Aristotle University Research group. The project was a wonderful opportunity to work on a grand scale industrial academic cooperation for a modern biomedical application. The project laid great challenges as it was important as an academic researcher to work closely with our industrial partner Micro2Gen, keeping in mind the different priorities of the private sector, without allowing them to hinder the academic research. During my work on the project I had to take initiative for changing specifications to better suit the hardware design and to coordinate the writing of deliverables, conference and journal papers. In certain occasions I represented my research group in collaboration meetings.

With my participation in the Marie Curie IAPP: Fast Tracker for Hadron Collider Experiments I participated in the FTK collaboration which is a very dynamic collaboration that strongly favours independence. In the FTK collaboration I was offered the opportunity to work on a very demanding clustering module and managed to complete the first version of the design in a very short period of time. I then proceeded to design the input step for the module proposing methods of parallelising each output, in order to facilitate future parallelization of the modules.

I have assisted in the supervision of post graduate students for their theses and several projects working independently with them in the followed design approach. I have designed training courses (on embedded systems, FPGA design etc.). I have participated in the organization of international scientific workshops and one national conference. I have chaired sessions of international scientific workshops. I have worked as a sales manager for a local telecommunications company where I was responsible for the sales of VoIP telecommunication products in Europe and the Middle East.

The potential for future development of the applicant – I will be able to extend my strong hardware design background with newly gained knowledge of experimental high energy physics. Even though my bachelor is in physics I never had to apply my physics background on electronic design. This will be an excellent opportunity to refresh my skills and use them to get a new approach for the hardware needed as I will be able to understand more thoroughly the physics behind the specifications. INFN Pisa, with its close connections to University of Pisa, Scuola Superiore Normale and Scuola Superiore Sant' Anna is the perfect place to do that. This ability will be extremely important as the HEP community looks at the SLHC phase II upgrade, where even more demanding hardware will be needed and people who can comprehend both aspects of the problem (physics, performance) will have an advantage.

As the project also includes exploring the associative memory architecture for more industrial applications (image processing etc.) INFN Pisa is also ideal since it has strong connections to industrial partners where the feasibility and usefulness of the approach can be explored. This interaction with industry will also put me in touch with board production and assembly management processes which will help my profile as a hardware designer.

Also with this project my managerial skill will have to be improved as I will have to request, manage and report on project funds.

- **Match between the *fellow*'s profile and project**

The applicant's skills and experience in relation with the proposed project.- The match is impressive and has already been proved by my participation in the Marie Curie IAPP: Fast Tracker for Hadron Collider Experiments project.

My background experience can be divided in three main descriptions: a) extensive experience of development of high performance FPGA implementations, b) exploration and modelling of multiprocessing systems, c) great experience in image processing implementations. My participation in the current project and the FTK collaboration is very well coupled with all the above qualities.

The L2 trigger performance requirements call for high performance hardware implementations combining both ASICs (the associative memory chips) and FPGAs for the data management, data reduction (clustering), data formatting, track fitting etc. These designs call for competent designer who can take the challenge from the hardware specifications to the final design verification. I already have a clear view of the complete FTK system,

as part of my training for the IAPP Fast Tracker for Hadron Colliders Project. My background in other demanding in performance designs is extremely well suited as it has already been proven by my ability to complete a demanding module for FTK in a couple of months.

The need for high performance and extreme data throughput for the FTK system can only call for high parallelism in all design levels and this is why the Associative Memory system is inherently parallel in nature, from hardware design level (RTL) to system level (boards and controls). As I have a background in design space exploration and modelling I can use my experience to seek for the most appropriate forms of parallelism for performance gain.

It is a goal of the collaboration to seek new applications for the associative memory systems, such as in image processing for implementations that require high resolution imagine (biomedical, security, astrophysics). My image processing background (algorithms, machine vision) will help me take this challenge. I worked on a edge detection algorithm and in APIMAP I should test the quality of the AM as edge detection device. I would need to use a 2D clustering algorithm to identify spots made of contiguous pixels above threshold and I am the person that developed the firmware for the FTK 2D clustering, and I have experience for the the center of mass calculation and algorithms for the definition of parameters related to the spots.

- **Potential for reaching or reinforcing a position of professional maturity**

The INFN organization is such that I will be strongly pushed to discuss/plan before and defend my work after. I will learn about management: supervision, organization of a team, presentation of the work in conferences. I will be part of a great collaboration with many years of experience and industrial connections. The goal coming back is that I participate in new proposals and work as referee for other group proposals. After the fellowship, I will have the competencies to attain such a position. These items will be part of my work: writing documentation, negotiations with industrial firms, financial planning and resource management. I will also participate in the effort to broaden the collaboration for new projects. The activity in the FTK collaboration will allow me to improve my capability for independent thinking and my managerial skills. As due to the current political situation Greek universities are severely underfinanced the only true source for research funding is through participation in international projects with strong international collaborations. My participation in such a collaboration and my ability to write project proposals and manage a project will strengthen my curriculum so that I am a strong contender for an academic position not only in my university but in all Greek institutes with interest in electronics and embedded systems.

Additionally, the collaborations strong international and industrial connections will give me the opportunity to pursue a possible position in these institutes as I will be an experienced researcher in the collaboration or in the collaboration's industrial partners.

- **Potential to acquire new knowledge**

My past experience in research is mostly on multimedia related FPGA implementations. My international experience is limited to four months secondment in CAEN SpA. The FTK group in Pisa would be a wonderful environment to move my career ahead and to give an international dimension to my knowledge. Dr. Paola Giannetti is a Director of Research at INFN Pisa and has been part of the Associative Memory research group from its beginning. INFN Pisa in conjunction with the University of Pisa has a very strong Physics group and a very strong electronics group. The experienced researchers from the FTK group in Pisa have been part of the team which developed and commissioned the SVT in CDF, so their experience will be an invaluable asset for my research.

The FTK group currently is working full time for commissioning the FTK vertical slice for the ATLAS TDAQ system in 2015. The ATLAS experiment would be a wonderful environment to move my career ahead and to increase the international dimension of my knowledge. The ATLAS collaboration is much larger than the FTK one. The ATLAS TDAQ system is a very complex architecture based on several different technologies where I could easily acquire new knowledge. The Associative Memory device is probably the most powerful but least flexible computing component of the system. It's integration in the TDAQ system requires powerful reconfigurable integration solutions. This is a high-level and creative work that starts from an understanding of the physics problems and goes all the way to the development of hardware-firmware solutions.

Additionally I will reinforce my physics background by acquiring experience in the physics behind the ATLAS trigger systems. A creative area for me would be understanding the ATLAS trigger selection criteria and analyzing their dependence on the accelerator luminosity, in order to find firmware/software optimizations. This is high-level work that starts from an understanding of the physics problems and goes all the way to the development of hardware-firmware-software solutions. My current background in firmware development will help my integration in the project and I will gain substantial background in particle physics in order to understand the specifications of

the ATLAS TDAQ system.
I can apply all what I learn also outside of HEP, in any field where computing power is a real issue. I will have the possibility, as described in my work-plan, to learn about totally new fields of application like medical imaging and brain studies, which is a really important target as the FTK collaboration looks to expand the application fields of the Associative Memory chips. For this part of the research project I will work closely with the experienced group in the University of Florence and also with the groups industrial partners.

B4 Implementation (maximum 6 pages)

- **Quality of infrastructures/facilities and international collaborations of host**

Of INFN countless international activities, some of the most important research is conducted at CERN in Geneva. Italy was one of the European laboratory's founding Member States and, through the INFN, it continues to be one of its most active members. Around 1,000 scientists from the INFN work in research groups at CERN, taking part in all experiments with the LHC particle accelerator (CMS, ATLAS, ALICE, LHCb, LHCf, Totem) and the SPS accelerator (COMPASS).

The INFN is also a major contributor to experiments at other leading foreign laboratories including FERMILAB, SLAC, BNL, and JLAB (United States); PNPI, BINP and JINR (Russian Federation); CIAE and IHEP (China); RIKEN and KEK (Japan); BARC (India), DESY and GSI (Germany), ESRF (France), PSI (Switzerland) etc.

In Italy, international collaboration is mainly concentrated at the INFN's four national laboratories, where major experimental facilities are available for use by the scientific community. One example is the VIRGO, interferometric antenna at Cascina, near Pisa, a joint-venture with the French CNRS IN2P3. The INFN also takes part in European scientific computing and nuclear physics projects. Together with numerous other research agencies from leading European countries, it founded the ApPEC (Astroparticle Physics European Coordination); it is a founding member of the French-Italian European Gravitational Observatory (EGO) Consortium (Cascina-Pisa); it is a member of the European Science Foundation (ESF) based in Strasbourg; it coordinates the EU-IndiaGRID2 project to improve grid technology in India. It has representatives on the NuPECC (Nuclear Physics European Collaboration Committee), on the PESC (Physical and Engineering Sciences) of the ESF, on the ICFA (International Committee Future Accelerators), on the ECFA (European Committee Future Accelerators) and on the FALC (Funding Agencies for Large Colliders). It is a member of the European Association for the Promotion of Science and Technology (EUROSCIENCE) in Strasbourg; it is a founding member of Science Europe based in Brussels; it holds a stake, with the CNR, in the European Synchrotron Radiation Facility (ESRF) in Grenoble.

Fundamental research in these areas requires the use of cutting-edge technologies and instrumentation, which the INFN develops both in its own laboratories and in collaboration with the world of industry. These activities are conducted in close collaboration with the academic world.

The INFN has a significant impact on Italian society. The technology and expertise developed by the INFN in conducting its experiments has major implications for the medical and healthcare industry and for the technology sector in general. Of the numerous examples, the development of a technique that uses carbon ions and protons to treat tumours (hadron therapy) stands out as particularly significant. The INFN has over a decade of experience in this field, gained directly at its laboratories in Catania. It built the hadron therapy machine installed at the CNAO in Pavia. The INFN is also a leading national and international player in the GRID, supercomputing network project and in expanding its use to applications in other scientific fields, e-commerce and culture. The INFN also uses its own analysis and research instruments and facilities to addresses issues regarding the cultural and environmental heritage.

Finally, the INFN is fully committed to promoting scientific culture. It takes part in all the main dissemination activities in Italy and each year it organises various exhibitions and events throughout the country, some of which are broadcast on TV.

The Pisa section is one of the most important inside INFN. It had leading roles in a large number of experiments. In CDF 4 spokespersons are Pisa researchers: prof. G. Bellettini, F. Bedeschi, L. Ristori and G. Punzi. Important leadership has been provided to the Higgs sector at CERN from Pisa: Prof. L. Foa' has been leader of the LEP physics in Aleph, and after that he had a leading role in the CMS experiment. G. Tonelli has recently been spokesperson of CMS.

The Heavy Flavour experiments were strongly represented both in the K and B sectors by prof. I. Mannelli and prof. M. Giorgi; the neutrino sector by Porf. Bemporad with the Chooz collaborations, the rare decay experiments by prof. A. Baldini with the MEG experiment, and the gravitational wave physics by prof. Fidecaro with the VIRGO

laboratory, astroparticle physics is present with the experiments Glast, AMS, Cream, Magic and Nemo, applied physics with advanced detector R&D, nano-technology is strongly represented at SNS, robotics at S. Anna, medical physics at INFN and CNR. All these activities are strongly supported by (a) a strong theoretical team, in particular a phenomenological school with Barbieri at SNS; (b) high-level educational capacities: the universities are reinforced by the schools SNS and S. Anna in Pisa and Santa Chiara infrastructures in Siena; (c) strong INFN administration teams; (d) large laboratory space; (e) high-level infrastructures for electronics service (board/chip design/production/test), mechanics service (detectors and large structures design/development/integration), high-technology (silicon detectors clean-rooms), computing (GRID at Pisa INFN and SNS). (e) high-level infrastructures for electronics and mechanics services, high-technology (silicon detectors clean-rooms), computing (GRID at Pisa, and SNS).

- **Practical arrangements for the implementation and management of the research project**

Implementation and management of the fellowship at host institution - practical arrangements that can have an impact on the feasibility and credibility of the project. – I know well the INFN structure in Pisa since I have been there few months during my IAPP secondment. In Pisa I will be able to access the FTK laboratory and I will have an office with computing capability to use all the necessary CAD software for my research. I will be allowed to use CADs for FPGA design (Altera and Xilinx software), for electronic board design and ASIC chip design (Mentor Graphics software and Cadence). Experienced technical staff will help me with the installation process and licences when necessary. FPGA test boards and prototype boards are already available in the laboratory and new will be acquired for the new devices which will be used in the project. I will use the laboratory for electronic tests, provided of racks with independent test stands, oscilloscopes, digital analyzer, and computers and terminals for access, control, monitoring of the available test stands. We will use standard 9U VME crates for board housing and the VME protocol for CPU-crate communication. A laptop will be available with CAD software to download new firmware directly through Boundary Scan.

At CERN, for parasitic tests in the vertical slice first and the FTK Demonstrator commissioning after, we will profit of the ATLAS and CERN famous organization. However the work will be more complex because of the interaction with the experiment. In the control room the shift team, helped by others experts, has the responsibility for the data taking or for tests of the whole TDAQ system during the shutdown. All the actions there have to be proposed and accepted by the TDAQ running coordinators before being executed. For this reason it is not possible to predict exactly now when and how we will operate, since our tests have to be coordinated with the tests from all the other groups. This part of the program to be executed at CERN is presently the less defined. However the activity performed with the Vertical Slice on the experiment during 2012 allowed us to know the TDAQ people and let them to know us. This will certainly help the long activity needed to test new prototypes on real data in the Vertical Slice and finally to install the Demonstrator.

My main collaboration will be with the researchers from INFN Pisa, but for different stages of the project I will have to interact strongly with FTK researchers from other Institutions spread around the world (USA, Japan, Europe, Australia). In particular researchers from Chicago and Fermilab that are developing the Data Formatter, Italian institutes such as INFN Frascati (Alberto Annovi, Guido Volpi, Naoki Yorita), and CERN (Andrea Negri, Jinlong Zhan, Viviana Cavaliere, John Bains, Walter Vandelli) for the FTK development stage, and University of Florence (Michela Del Viva) for the image processing exploration stage. I will have strong sharing of efforts with the companies that will participate to the FTK production, in particular CAEN in Viareggio, Italy and Prisma Electronics in Greece, since they are partners of the IAPP project.

The close connection of INFN with the University of Pisa, Scuola Superiore Normale and Scuola Superiore Sant'Anna allows researchers to follow organized seminars and courses to expand their knowledge. I am very interested to profit of them (see Section B2).

- **Feasibility and credibility of the project, including work plan**

Work plan that includes the goals that can help assess the progress of the project. - The FTK TDR has now been approved, the construction and design phase has started and will last for at least 4 years. It will be characterized by (a) a hardware design phase, during which the final optimization will be done, especially to reduce execution time as much as possible while maintaining processor performance (2014) (b) testing new prototypes and new firmware (2014) (c) the use of the Vertical Slice in the experiment to test the new prototypes collecting data in parasitic mode & learn with real data about FTK timing performance, to develop the control and monitoring software inside TDAQ, to implement the first track-based Level-2 selection algorithms and see their impact on important Higgs data samples (1 year activity between 2014 and 2015), (d) commissioning of the

Demonstrator (first half of 2015); (e) analysis of the ATLAS data to verify the FTK physics improvement.

I was included in the research of the FTK project during my secondment in CAEN SpA for the IAPP FTK project. I was trained in the FTK architecture and I have a complete and clear view of the system, which will help me start my research work as soon as the fellowship starts. My work, starting from the current system, will focus in architecture optimization through simulation and data analysis, and will be completed with strong participation in the construction, installation, and testing of the hardware that will be built in Frascati (the production of mezzanines for the 2-D clustering in the ATLAS pixel detectors).
The goals in Pisa are:

1. Apply my large experience on the use of FPGAs and test procedures to develop important modules for the FTK system's operation. This means:
    a. First year: to complete the implementation and parallelization of the 2-D clustering firmware in the FTK Input Mezzanine board. Complete the design and participate in the tests. Evaluate the relative costs of the FPGA solution and a small standard cell device. This work would be for the FTK Demonstrator to be installed for 2015 data taking.
    b. Second year: to develop and implement the design of the new version Track-Fitter to be placed in direct contact with one new Associative Memory chip. This design is not exploited for the standard FTK but it is the first step toward the design of the miniaturized elementary unit, the FTK SIP, that will be the fundamental block for future developments.
    c. Develop the necessary monitoring modules for the 2-D clustering and the new Track-Fitter. Assist in the development of the necessary software to execute monitoring and tests.
2. Interact with the ATLAS group at Argonne that will work on the Data Formatter mother board where the Frascati mezzanine will be placed and participate to tests of the integrated system.
3. Try to use the developed processor to analyze 2D images in other applications outside HEP. The goal of this demonstration is to use the AM-chip for simulation of the initial stages of the brain visual processing, such as the identification of object contours (edge detection). Data reduction of external stimuli before higher level processing is essential in (high rate) background filtering and during extraction of salient information from complex colored and highly textured natural images with multiple luminosity levels varying over time due to changes in illumination or motion of objects. Simulations of such visual analysis are onerous to implement, if at all, in usual supercomputers. Once assembled and suitably adapted and interfaced for the specific purpose, the prototype would be used to execute detailed and thorough simulations.
   I have experience from the past on "edge detection" algorithms, so it will be very interesting for me to test the AM capability to solve in real time this important task. In addition of that I worked for the pixel 2-D clustering algorithm inside FTK, an algorithm that is perfect for real time reconstruction of the shapes filtered by the AM. Let's call these two steps "AM edge detection" and "2-D shapes reconstruction". I will run them in pipeline.
   Let's start with the "AM edge detection". For the demonstration I will use an old AM system, a 9U VME board where input data are received on 6 parallel buses by a large Virtex II FPGA and loaded on CDF AM chips whose patterns are made of 6 15-bits independent words.
   Two computing phases will be necessary, first the training then the image processing.
   During the training phase, different steps will be taken into account:
   - The AM system has a large FPGA that will receive the image bit-streams (could come from a video-camera) through large FIFOs loaded by VME.
   - The FPGA will partition the input into small patterns (3x3 contiguous bit patches for static images, 3x3x3 for movies) and then will compute the frequencies of all possible patterns (512 for static images and 128 millions for movies) in a large set of natural images,
   - Then the FPGA will select the relevant patterns to be downloaded in the LAMB using the right range of frequency.

   During the image processing phase different steps will be taken into account:
   - A new set of independent images will be partitioned into 3x3 or 3x3x3 bit patterns by the FPGA and sent to the AM chips that will send back only the matching patterns.
   - The "filtered patterns" will be reorganized by the FPGA to produce the "filtered image".
   - During the image processing phase, the FPGA will continuously monitor the frequencies of salient patterns and, if the patterns downloaded in the AMchips will result outside the correct frequency range (i.e. predictive of their saliency), image processing will stop and a new set of updated salient patterns will be substituted in the filtering engine.

I will run in pipeline the **"2-D shapes reconstruction"** step to reconstruct the shapes filtered by the AM.

- The filtered image will be further processed by finding shapes in sets of contiguous bits over threshold, as done by FTK for clusters in the pixel detector. The FPGA proposed algorithms to be developed is highly parallelized and will achieve a processing time linear with respect to the number of pixels to be processed. This means that clustering can be performed in pipeline with the image acquisition, without suffering from combinatorial delays due to looping multiple times through the whole amount of data. For this reason, it is intrinsically stable with respect to the image occupancy and size. It is a fast general-purpose algorithm for high-throughput clustering of data "with a two dimensional organization". The two-dimensional problem is well processed by FPGAs since their available logic is naturally organized into a 2-dimensional array. The algorithm proposed is designed to be implemented with FPGAs but it can also profit of cheaper custom electronics.
- The reconstructed shape can be analysed further by the FPGA to measure quantities like the size. It can also be organized by the FPGA in the right resolution to be compared with high level templates of searched of particular wanted shapes downloaded again in the AM, trying to recognize wanted objects.

This projected route opens up the capabilities of the AM-chip combined with FPGA in the field of Medical Imaging as well ("A fast FPGA-based clustering algorithm for real time image processing"; NSS Conference Record, 2009 IEEE, Page(s): 4138 - 4141, 2009). The AM-chip filtering function, combined with the computing power of parallel arrays of FPGAs applied to image reconstruction could reduce the execution time of image processing. One potential application area is in the realm of automated medical diagnoses by imaging. The target focuses on the possibility of analysing time-changing images.

In conclusion, my work plan is complex and very ambitious, but I will be in the center where all these ideas are born and I will be working with a large group of very motivated people that will be of great help for the realization of this plan. Things external to my fellow will contribute to push me for a quick advancement:

- The FTK schedule in the ATLAS experiment and the milestones defined there. They require the FTK Demonstrator to take its own first data in the detector barrel in the second half of 2015 and a complete FTK detector coverage in 2016.
- The fact that application to imaging outside HEP would open the possibility of an important spin-off able to produce an interesting output on society and on the market. This is one of the goal of the FTK IAPP project that has Pisa as coordinator and the CAEN industry, very near to Pisa, involved as a partner. I will profit of the collaboration of all IAPP participants.

Work on FTK allows qualification for ATLAS membership. After one year I will be allowed to enter the ATLAS default author list and sign the full ATLAS physics output.
The work plan includes participation in conferences and related paper production. I plan at least two technological conference contributions (IEEE or similar) in 2 years and more than two technological papers.
The work plan also includes frequent presentations of the work inside the TDAQ/Physics group and seminars to the ATLAS collaboration of Pisa high energy community. It will include also supervision/tutoring of students working in ATLAS TDAQ.

- ***Where appropriate, describe the approach to be taken regarding the intellectual property that may arise from the research project.***

Inside INFN, publication on international journal is the standard way for communicating, research results. The usual targets for technological publications relating to the HEP experiments are JINST, IEEE TNS and NIM, while for the AM application exploration stage of the project we intend to target IEEE TVLSI or similar ACM journals.

- **Practical and administrative arrangements, and support for the hosting of the *fellow***

The University of Pisa is the biggest employer in the area. While the majority of the students are from Italy it has a strong multi-ethnic community from different European countries and many others such as Japan and China, due also to the attraction due to Scuola Normale and Sant'Anna. INFN is also a host for multinational researchers and has many international collaborations. The FTK group in Pisa has hosted many international researchers in the past from USA, Japan, Switzerland and currently also from Greece. They can profit of University structures in the center of Pisa (http://www.dsu.toscana.it/it/contatti/servizi.html) or private arrangements at very good prizes. Pisa

as a whole can be considered a campus, since the main resource is the very large University.
INFN offers full social security benefits. It provides a high speed internet connection cable and wireless for all the affiliated researchers. A security badge is offered for each affiliated member which allows access to the university campus, the INFN offices and laboratories. The badge allows access even in weekends if necessary. The campus offers a free parking space for employees and researchers.
The University of Pisa has an International Office to assist international students in Pisa. Visa and Registration assistance if offered for EU and Non-EU citizens. Assistance is also offered for obtaining the Italian tax code (Codice fiscale). There is also an accommodation office to assist students and researchers to find a suitable house or apartment. Accommodation can also be offered in one of the 1200 student accommodation places. The university's Interdepartmental Language Centre (CLI) offers Italian language courses for international students during the year for different proficiency levels. Many sports and leisure activities are offered. The university has a Sports Centre where university members are not required to pay a fee. Numerous university libraries and museums are spread throughout the city of Pisa. The position inside Tuscany and centrality in Italy allow very easy communication with the most important towns. It is also easy to move to CERN, also for short periods.
Since I have worked in the Pisa area for four months during my secondment in CAEN SpA for the IAPP FTK project I am already familiar with most of the bureaucratic processes necessary for both social security and taxation in Italy, I am familiar with the bureaucratic processes in the University of Pisa and INFN, as well as finding an accommodation in the area. I also speak elementary Italian, but when help was necessary it was always offered by the group to deal with administrative processes.
I also plan to follow Italian courses to improve my Italian.

B5 **Impact** (maximum 4 pages)

- **Impact of competencies acquired during the fellowship on the future career prospects of the researcher, in particular through exposure to transferrable skills training with special attention to exposure to the industry sector, where appropriate**

The fellow's potential of acquiring (complementary) competencies and skills during the fellowship…..

This project will allow me to increase my experience in electronics from design level to a grand scale system level. As my first degree is in Physics an important aspect is that I will additionally get experience in high energy physics experiments and this will make my professional curriculum more complete. As a physicist with a specialization in electronic design, in fact, it is important to be able to combine the my electronics background with newly acquired knowledge of physics analysis techniques and the capability of finding the most appropriate technical instruments to perform a physics measurement. This ability can be applied in a variety of different research fields (biomedical, imaging etc) as I will be particularly helpful choosing the right technology for online algorithm implementation. Moreover I will gain knowledge of hadron collider physics processes and the best strategies for online selection of such events. I will learn about monitoring/diagnostic/standardization problems for very complex electronic systems.
In addition to the solid electronics background I will gain with the fellowship, the experience acquired developing tools for online and offline data processing will be very useful at LHC for early data studies and for long range, efficient data taking planning.
I will complete my goals working in a totally new environment. I will know many LHC scientists, not only in Italy, but also at CERN, working in direct contact with the TDAQ group. I will learn from their experience, specifically developed on the ATLAS architecture.

…their impact on the prospects of reaching and/or reinforcing a position of professional maturity, diversity and independence

If the FTK demonstrator will be successful, FTK will be enabled for a large production and will be a trigger upgrade for the LHC Phase1. The success will push further this research, involve new Institution and Companies in an area that is in quick expansion, where new management and organization capabilities are strongly needed.
A new R&D is planned for the FTK evolution (FTK SIP) necessary for the many new foreseen applications, like online tracking at L1 for LHC Phase II and use of the AM for image processing. Time for FTK production after the TDR approval will be quite long, because of the LHC schedule, so even the FTK final production could profit of the electronic and algorithm advancement we plan to pursue in the next years. While the demonstrator will

convince the collaborations of the FTK capabilities, we will provide modern, much more powerful prototypes. The Associative Memory technology possible applications are many and increasingly complex.
I will become expert of these technologies and the necessity of expertise in these field will favour my professional position and my chance to build a group working with me. I will be able to propose new research fields and to provide a strong case to support them, and build a group to participate to a strong collaboration.
My curriculum will be general enough (electronics, advanced analysis techniques) to fit also on other spin-off projects, such as medical applications and brain simulation studies. I hope to become able to propose a project based on the experience acquired into our Super-Computer HEP activity, spreading our knowledge in new areas where computing power is a real issue.
I've already worked in Pisa and collaborated closely with INFN, University of Pisa and the FTK group for a brief period of four months. The period I will spend in Pisa will allow me to learn a different working style from a very good group, staying closely and continuously in contact with them. I hope to improve my communication skills and also my use of the Italian language.

- **exposure to the industry sector**

Working on the construction of so much hardware it is easy to have contacts with industries. We collaborate with

1. CAEN in Viareggio, very near Pisa. It offered space and expertise to allow the system integration before going to CERN and to perform cooling tests including power supplies that they will produce for us and will dissipate up to 5 kW in a single VME crate. CAEN could be also the company that will manage maintenance of FTK.
2. Prisma Electronics at Alexandroupoulis,Greece. It should assembly and tests the produced boards with our help. We have installed an FTK test stand at the company, to be able to run a first test before sending them to CAEN
3. Cistelaier, Modena, in Italy to produce the PCB of our prototypes.
4. IMEC, Belgium, Europractice. It is the interface towards TSMC and ASE for producing and packaging the AM chips.
5. Microtest, Altopascio, near Pisa. It is the company that perform the AMchip tests on large scale.

FTK community has very good relations with all these companies, considering that we have already built many prototypes together, most of them have participated to the SVT production and also we applied more than once to funds together. For me it will be a good occasion to learn about industry organization and also an important opportunity if I would decide to leave HEP research.

- **Contribution to career development or re-establishment where relevant**

The fellowship will develop characteristics that will aid the fellow in finding a professional position in either her home country (Greece) or other European countries with research background in experimental HEP and long-term participation in HEP research programs, such as CERN. Also, the acquired skills described previously apply to many different fields outside HEP providing thus flexibility to the fellow to establish a professional career in areas not directly related to HEP, but where high performance computing and analysis is necessary such as astrophysics, nuclear physics, biology/genetics, robotics, neuroscience, accelerator physics and medical physics. The high level of technology involved in the realization of the program provides the fellow the ability to develop a professional career in industry. For example, the fellow will be able to work in areas which demand high performance electronic design skills such as multimedia, security applications, communications etc. As the fellow's curriculum lacks extended international experience, the fellowship is fundamental to complete her curriculum. One important point is that the FTK group in Pisa pushes for publications and dissemination of its work in conferences which will be very important to increase the chances of the fellow's future in academia.
In the case of a fellow returning to research, how will his/her re-establishment be helped by the fellowship? – As already mentioned, the fellowship is expected to provide the fellow managerial and independent thinking skills that not only will improve the probability of obtaining a staff research position in a European institution, but also will broadly advance his career. This is also due to the specific nature of the project, which is totally innovative and involves high technology; it combines knowledge and capacities specialized in experimental HEP but enough general to be interesting for industry, at hardware and at software as well.

Benefit of the mobility to the European Research Area

Describe how the proposed mobility is genuine and therefore beneficial to the European Research Area. Genuine mobility is considered to allow the researcher to work in a significantly different geographical and working environment, different from the one in which he has already worked before – The proposed mobility can really improve Greek research organization. The Greek style is often too much against mobility. Each community wants to keep its researchers for ever. Often a person starts as student in an Institute and a particular

group, becomes phd-student and researcher there, after that takes a permanent position in the same institution/group. I am an example of this very case as I took my Bachelor's, my Master's and I am working toward a PhD in the same group of the same institution. Italy and CERN will be significantly different from my past experience. This mechanism creates in Greece local dependency mechanisms that can interfere with pure meritocratic criteria during recruitment. In Italy the mobility is practically forced on young researchers because even during their 3 year compulsory PhD duration they have to spend a year working on an institution abroad, which has an extremely beneficial impact on the Italian system. Italian researchers have a strong international presence. The mobility from a young age has helped in a way that Italian scientists work in all major research institutes of Europe and abroad, and in this way the mobility of young scientists is promoted even further.
In Italy young researches that have worked abroad, have developed a different thinking and they exit out of the most rigid Italian mechanisms, creating a new Italian research style. Additionally, the Italian research groups' international connections and cooperations assist them to form strong collaborations for research projects of cutting edge science, which makes them very likely candidates for international and European funding. This knowledge should be transported back in Greece where especially in the current political situation research is seriously underfunded.

- **Development of lasting cooperation and collaboration with other countries**

What is the likelihood of creating collaboration between the host country and other countries after the end of the fellowship? - The FTK collaboration is born as an international collaboration, including USA, Japanese, Italian and German institutions. It is grown recently, with the inclusion of France, Switzerland, Melbourne and Greek Institutions. We are looking to strengthen this connection and make Greek universities long term partner of the collaboration. The University of Thessaloniki is applying to national funds for infrastructure for super-computing development. Moreover, supercomputers can have wide applications even outside HEP. For this reason, my activity in the proposed APIMAP research project not only will reinforce the collaboration inside the HEP community, but also has a strong potentiality to favour the enlargement of the collaboration behind the development of the trigger technology in HEP.

- **Contribution to European excellence and European competitiveness regarding the expected research results**

How will the fellowship contribute to the European excellence and European competitiveness?
Our main goal is the use of our supercomputers (upgraded with the latest available technologies) in the baseline ATLAS configuration and future more complex applications. Our asymptotic, very challenging goal is to standardize a single processor that can work on both L1 and L2 applications at future high energy physics experiments and to explore its possible applications outside HEP.
Interest is growing around this project: the FTK collaboration does exist for the L2 application, but the FTK project popularity is quickly increasing in Europe and its influence on L1 tracking ideas is strong, both for the physics case and the technological developments. The interest for similar technology applied at L1 has been shown by the Italian SLIM5 collaboration first ["The associative memory for the self-triggered SLIM5 silicon telescope", the Slim5 collaboration, Nuclear Science Symposium Conference Record, 2008. NSS '08. IEEE19-25 Oct. 2008 Page(s):2765 – 2769] and is growing quickly at LHC. We think that our influence is going to increase resulting in improved physics capability of the LHC experiments.
A large collaboration from the FTK community has also participated to the 7th RTD Framework Programme - Specific Programme Cooperation Theme 3 "Information and Communication Technologies" Call identifier: FP7-ICT-2013-call 10, with a proposal of dedicated hardware highly parallelized that brings together embedded computing and high-performance computing teams jointly addressing challenges common in these two areas. The proposal was presented as the intention to face the need of future growth in computing performance exploiting parallelism. The explosion of data (the "Data Deluge") and the increase in natural (unstructured) data from the real world (i.e. "cyber-physical systems") is increasing computation requirements, and demanding new processing and computing methods and storage faster than technology can keep up. Increasingly complex algorithms, faster devices and systems are required to efficiently handle this new era of data to tackle the increasing gap between the growth of data and processing power. We were not funded because we were not enough convincing to be able to go to the market and really provide socially interesting applications. My fellowship would allow to have enough manpower to get some interesting results on medical applications, or movement reconstruction, so that we could be more convincing with important companies of these sectors and apply again. We think we can have an important impact on European competitiveness also for social applications,

but we need visibility in these new areas of research.

- Impact of the proposed outreach activities

Describe the outreach activities of the proposal to be implemented by the researches during the project duration – Significant outreach activity took place in the past to convince the LHC community that a hardware tracker is a fundamental tool for triggering at hadron colliders, especially for high-demanding collision environments. This was devoted mainly to the HEP community but allowed to develop web sites that could help to enlarge the knowledge of Super Computers outside HEP. The FTK project is now approved by the ATLAS Collaboration therefore the outreach work can now be reinforced by results on LHC data. In fact, up to now the FTK project was based on performances measured on simulation results or extrapolated from the successful performance of the SVT tracker. In the next years, the FTK demonstrator will offer the opportunity to give the first examples of the FTK potentialities on data acquired in the real experimental environment. In parallel, the first real prototypes promising the capability to exploit best of the available technology will be produced and tested, giving a concrete proof of the computing capability that the project can provide.

We believe that the technique can be used not only in HEP but is matured enough to be exported outwards, such as in medical science. Another aim of the FTK project is to convince the medical community about the impact of Super Computing can have in many aspects of medicine. At the moment, the possibility that image reconstruction can perform also at very high rates and in real time is not well-distributed in medical science. We think that the success of applying this technique in HEP will also be a boost to grasp the attention of other scientific communities as well. We consider very important the approach of the medical community. This could be done through presentation of the power of the Associative Memory chip systems in combined conferences such as NSS-MIC where both the Nuclear and Medical Imaging communities participate.

However outreach has first of all to be extended to the general public. I will participate and favour all the outreach already planned by FTK IAPP project. One annual occasion for each of the listed corresponding deliveries is expected in the collaboration:

IAPP project open day: the FTK labs will be open to the public to show the racks, crates, boards and chips developed by the collaboration. Teachers (the fellows in particular) in front of posters in the lab will describe the importance of the real time analysis performed on FPGAs (a new type of computing) to make sophisticated decisions in few microseconds, for HEP experiment triggers as well as for other applications outside HEP. The programmable logic power based on real time parallel computing will be described with examples. The importance of "pipelining" and "parallelism" will be described in detail with examples as being the key features of our computing model. Simple CAD stations (Xilinx and Altera systems) will be provided to visitors to develop their own simple logic. Logic examples already done will be provided for people interested only in the implementation inside the chip, not in the logic development. The goal is to let them understand how easy and powerful the use of these tools is.

FTK Workshop day: a set of seminars and lectures will be provided to university students on trigger for HEP experiments and FPGA applications outside HEP. This will be also the occasion to announce the Summer school week plan for the year. Few students will be allowed to spend a week during summer in one of the partner laboratory.

In addition I plan to work on dedicated web sites, participate to shows like the European initiative "Night of the Research" with posters, samples of hardware material and discussing directly with visitors. I propose myself also to participate as **Marie Curie Ambassadors,** that is I would like to visit schools to speak to young students, in particular girls to promote their interest for the research or assist teachers in preparing and delivering teaching materials.

The *Outreach plan* is very important in our project for many reasons: (a) to promote communication between the scientific community and the general public and to increase awareness of science. These will be occasions to show how important the HEP experiments are not only for the advancement of the nature knowledge, but also for the technological advancement. (b) to allow clever students to come in contact with the "big science" and let them know LHC and the experiments that they could join for their own future research activity. (c) to spread the use of programmable electronics (FPGAs) has new computing facilities.

B6 Ethical Issues (no maximum pages)

MAIN ETHICAL ISSUES THAT MUST BE ADDRESSED

- Human embryonic stem cells
- Informed consent
- Privacy and data protection
- Use of human biological samples and data
- Research on animals
- Research in developing countries
- Dual use

AREAS EXCLUDED FROM FUNDING

- Research activity aiming at human cloning for reproductive purposes.
- Research activity intended to modify the genetic heritage of human beings which could make such changes heritable (Research related to cancer treatment of the gonads can be financed).
- Research activities intended to create human embryos solely for the purpose of research or for the purpose of stem cell procurement, including by means of somatic cell nuclear transfer.

Include the Ethical issues table below. If you indicate YES to any issue, please identify the pages in the proposal where this ethical issue is described. Answering 'YES' to some of these boxes does not automatically lead to an ethical review. It enables the independent experts to decide if an ethical review is required. If you are sure that none of the issues apply to your proposal, simply tick the YES box in the last row.

ETHICAL ISSUES TABLE

Guidance notes on informed consent, dual use, animal welfare, data protection and cooperation with non-EU countries are available at:
http://cordis.europa.eu/fp7/ethics_en.html#ethics_sd

	Research on Human Embryo/ Foetus	YES	Page
	Does the proposed research involve human Embryos?		
	Does the proposed research involve human Foetal Tissues/ Cells?		
	Does the proposed research involve human Embryonic Stem Cells (hESCs)?		
	Does the proposed research on human Embryonic Stem Cells involve cells in culture?		
	Does the proposed research on Human Embryonic Stem Cells involve the derivation of cells from Embryos?		
	I CONFIRM THAT NONE OF THE ABOVE ISSUES APPLY TO MY PROPOSAL	X	

	Research on Humans	YES	Page
	Does the proposed research involve children?		
	Does the proposed research involve patients?		
	Does the proposed research involve persons not able to give consent?		
	Does the proposed research involve adult healthy volunteers?		

	Does the proposed research involve Human genetic material?		
	Does the proposed research involve Human biological samples?		
	Does the proposed research involve Human data collection?		
	I CONFIRM THAT NONE OF THE ABOVE ISSUES APPLY TO MY PROPOSAL	X	

	Privacy	**YES**	**Page**
	Does the proposed research involve processing of genetic information or personal data (e.g. health, sexual lifestyle, ethnicity, political opinion, religious or philosophical conviction)?		
	Does the proposed research involve tracking the location or observation of people?		
	I CONFIRM THAT NONE OF THE ABOVE ISSUES APPLY TO MY PROPOSAL	X	

	Research on Animals	**YES**	**Page**
	Does the proposed research involve research on animals?		
	Are those animals transgenic small laboratory animals?		
	Are those animals transgenic farm animals?		
	Are those animals non-human primates?		
	Are those animals cloned farm animals?		
	I CONFIRM THAT NONE OF THE ABOVE ISSUES APPLY TO MY PROPOSAL	X	

	Research Involving non-EU Countries (ICPC Countries	**YES**	**Page**
	Is any material used in the research (e.g. personal data, animal and/or human tissue samples, genetic material, live animals, etc) : a) Collected and processed in any of the ICPC countries?		
	b) Exported to any other country (including ICPC and EU Member States)?		
	I CONFIRM THAT NONE OF THE ABOVE ISSUES APPLY TO MY PROPOSAL	X	

	Dual Use	**YES**	**Page**
	Research having direct military use		
	Research having the potential for terrorist abuse		
	I CONFIRM THAT NONE OF THE ABOVE ISSUES APPLY TO MY PROPOSAL	X	

ENDPAGE

PEOPLE
MARIE CURIE ACTIONS

Marie Curie Intra-European Fellowships (IEF)
Call: FP7-PEOPLE-2013-IEF

PART B

“APIMAP”
Advanced Parallel Implementations for associative Memory APplications