STARTPAGE

HUMAN RESOURCES AND MOBILITY (HRM)
ACTIVITY

MARIE CURIE ACTIONS
Marie Curie Outgoing International Fellowships (OIF)

PART B Section 1

"POT"

B1.1 SCIENTIFIC QUALITY OF THE PROJECT *(MAXIMUM 4 PAGES)*

This project is a "second generation" high precision real time tracking system for the CDF experiment. Our group developed the "first generation" Silicon Vertex Tracker (SVT) and is now working on the upgrade to the original system. Our project encompasses the exploitation and optimization of the upgrade to improve as much as possible the CDF physics program. The CDF experiment is located at the Tevatron hadron collider at Fermilab, a USA national laboratory near Chicago. At present, the Tevatron is the particle accelerator providing the highest center-of-mass energy collisions in the world. It accelerates protons and antiprotons, and then makes them collide head-on inside the CDF detector. The CDF detector is used to study the products of these collisions. For a short description of the detector, please refer to section B2.2. Real time event reconstruction is a critical component for any detector at a hadron collider. The rate of collisions at CDF is a few million per second. Since it is impossible to readout and store data from all detector components at this rate, a realtime event reconstruction is made in the trigger to select the most interesting events for storage and later analysis.

The beginning of the XXI century appears to be very exciting for high energy physics: the Tevatron at Fermilab and later on the new powerful hadron collider, the LHC at CERN (the European laboratory located near Geneva), may give conclusive answers in many sectors of fundamental physics, e.g. supersymmetry, Higgs boson, and CP-symmetry violation. This project will have an important impact on this high energy physics program.

The experiments at these machines provide a large coverage of tracking detectors with very high spatial resolution (10-100 μm) around the primary interaction point. These detectors are very well suited for the study of physics channels containing the top and bottom heavy quarks, thanks to the possibility of measuring particle momenta (tracking inside a magnetic field) and identifying the b-quark decay vertices. Before decaying, B hadrons travel hundreds of microns and originate a decay vertex (secondary), which is spatially distinguishable from the production vertex (primary), provided adequate space resolution is available in the detector. Therefore, identification of a secondary vertex close to the primary vertex strongly suggests the presence of a b quark.

Past experience has shown that the identification of b quarks is extremely important in analyses at hadron collider experiments, not only for b quark studies per se but also for top quark and Higgs boson searches and for studies of processes beyond the standard model since the primary decay modes often contain b quarks. The silicon detector (SVX) of the CDF experiment, with a spatial resolution of the order of 10 μm, played a key role in many physics results coming from CDF, first of all the discovery of the top quark in 1995, as shown by an abundant scientific production.

Originality and innovative nature of the project – relationship to the state of the art in the research field. - These very precise silicon detectors, which contain hundreds of thousands or millions of channels, raise the problem of the complete tracking of large numbers of high multiplicity events. With tens or hundreds of particles produced by multiple primary collisions and traversing several detector layers in all directions, this is a formidable challenge even for the off-line analysis. The feasibility of a complete high-quality tracking for real time event selection has been considered impossible in large experiments at very high rates. In the past, real-time tracking was performed in a limited detector region or on a small subset of events, selected previously using other detectors.

The interest for the high event rate real time tracking at hadron colliders is mostly based on the possibility of the selection of events with b quarks in the trigger. Historically, events with b quarks were selected based on lepton identification. Trigger selection based on the secondary decay vertex increases the b-jet identification efficiency and opens up the possibility of studying the hadronic decay channels of the b quark, inaccessible to lepton methods. In particular, CDF has demonstrated the possibility of successfully using purely hadronic channels in the study of the top quark, in Higgs searches, and even in the reconstruction of the Z0 boson, thanks to the secondary vertex b tagging.

Electronics is becoming so powerful that the difference between the real-time and offline algorithm performances can be significantly reduced, even in hadron collider experiments producing

complex events at very high rates. We have already built a real-time pattern recognition system at CDF that approaches the performance level of off-line systems. The CDF online tracking system is a unique example of online b-quark selection in high energy physics. It attains supercomputer-class performance using a mixture of technologies, applied to the different parts of the tracking algorithm. High performance of dedicated hardware and flexibility of general purpose CPUs are obtained through the use of programmable devices. Three key features allow the SVT to carry out its job in few tens of microsecs: a highly parallel and pipelined architecture, custom VLSI pattern recognition, and a linear track fitter implemented with FPGA technology. We want to improve the functionality of the online tracking to match the Tevatron luminosity increase and to foster the use of these powerful online processors to more complex applications in the future.

Timeliness and relevance of the project - This is an important time to demonstrate to the high energy community the capability of the CDF online tracker. Many physicists dismiss the possibility of complete on-line tracking at hadron colliders because they see the problem as too formidable. Typically, online event reconstruction is subject to strong restrictions, such as tracking in a limited detector region or in a small subset of events. The goal of this research is to overturn this dominant opinion by demonstrating that up-to-date technology, exploited with suitable organisation and algorithms, permits the development of high-performance tracking triggers sensitive to secondary vertices.

Interdisciplinary and multidisciplinary aspects of the proposal- Generality and programmability allow the application of these ideas to other fields such as physics of accelerators with fixed target, or medical physics. For instance, the use of similar architectures for 4-momentum reconstruction of photons measured by liquid scintillator calorimeters with many phototubes has recently been studied. In this project the primary focus is on an architecture structured and dimensioned for CDF and even more complex future experiments. However, a very simplified version could be used in other applications such as for tracking in experiments on board of satellites (AMS, AGILE, GLAST) or by trackers for diagnostic imaging.

At a more general level, high performance computing architectures synergistically using CPU's and FPGA elements have been recently introduced. Experience gained in optimally partitioning a very complex algorithm on a variety of computing technologies will be an important asset for the efficient exploitation of these new computing structures.

Scientific/Technological Quality The trigger selection system at CDF is organised into a multi level architecture. This system selects the most interesting event signatures to reduce the high event production rate (bunches collide at 1.7 MHz) to a rate which can be stored on tape for further analysis. The level-1 (LVL1) and level-2 (LVL2) triggers are based on dedicated custom designed processors and reduce the rate to ~20-30 kHz and ~300 Hz respectively. Level-3 selection is performed by a CPU farm, outputting 50-100 events per second, which are written on tape.

The CDF trigger track processor architecture has a multi-stage structure, which solves the track reconstruction problem by successive approximations. At each stage the event is analyzed with increasing spatial resolution. The eXtremely Fast Track (XFT) processor finds tracks (P_t>1.5 GeV/c) in two dimensions (r-ϕ) at LVL1 in the large Central Outer drift Chamber (COT) with 96% efficiency, transverse momentum resolution σ (1/P_t) = 1.7 % and angular resolution σ (ϕ_0)=5 mrad in the transverse plane (ϕ). The XFT algorithm divides the pattern recognition into two steps: first track segments are found in each COT superlayer (12 wires) and then these segments are linked together to form tracks. In addition to being used in the LVL1 trigger decision, the XFT tracks are passed to the SVT processor for subsequent use at LVL2. In the SVT, five layers from the silicon vertex detector can be linked to the XFT tracks. The complex pattern recognition algorithm is again subdivided into two simpler sequential steps of increasing resolution. The first step associates fired silicon detector channels, called hits, and XFT tracks with low spatial resolution track candidates, called roads. This first step is performed by a dedicated device called Associative Memory (AM). In the second step, the real tracks are searched inside roads and fitted to determine their parameters (transverse impact

parameter resolution 35 μm, $\sigma(1/P_t)$ = 0.3 % and $\sigma(\phi_0)$=1 mrad). Tracks with a large impact parameter (distance larger than 100 μm from the center of the detector) are finally selected to indicate a secondary vertex.

The installation of the XFT and SVT processors at LVL1 and LVL2 respectively in the CDF experiment for the RUN II has been a great success. We have demonstrated that up-to-date technology allows high-performance tracking triggers sensitive to secondary vertices, at low cost and using design techniques and technologies, that although state-of-the-art are easily controlled within the physics community. SVT considerably enriches the b-quark event samples and, thanks to the improved threshold sharpness, it also results in better momentum selections at very high event rates.

These algorithms can be implemented using different technologies. Commercial CPUs offer flexibility, standardization and ease of upgrade but they are slow. The CPU flexibility is a great advantage for the full resolution tracking, because it must handle many variables and specific situations such as local corrections, alignment effects, exceptions etc. However programmable logic available today is flexible enough to successfully replace the CPUs even in high resolution computations.

Coarse resolution pattern recognition, however, does not profit very much from CPU flexibility. A large fraction of the CPU time needed to reconstruct high energy physics events is wasted in data sorting with a lot of random accesses to a large storage that contains all the tracker data. By contrast, the XFT processor and the AM perform the most CPU intensive part of the pattern recognition, consisting of a very large number of regular and highly structured loops of simple logical operations, always identical, with dedicated highly parallel structures.

Both XFT and the AM exploit the idea of a pattern matching algorithm based on precalculated and stored track candidates, which are compared in parallel with the actual event. The AM has to solve a more difficult problem since the silicon detector has about a factor of 10 more channels than the COT. For this reason a high density dedicated chip has been developed for the AM, while for the XFT commercially available programmable logic has been used. The first SVT associative memory chip was developed several years ago using VLSI full-custom technology and is specific for CDF. Because of the nature of a full-custom chip, it is not easily tailored to other experiments. Any redesign requires a large investment of time, personnel, and money. For simple applications, we designed a low density AM chip based on the essential characteristics of the programmable devices on the market such as Field Programmable Gate Array (FPGA). The use of commercial FPGA devices allows easy development and an easy update of the project. Technology improvements can be followed simply by replacing an old device with a pin-compatible newer version, which is usually faster and denser. Final production can use up-to-date technology. It is also easy to test and debug the prototype. Programmable chips are 100% tested at the factory. System performance can be studied and predicted with the full device simulator provided by the manufacturer. Boundary-scan, supported by last generation FPGAs, allows full test of printed board connections.

The only aspect for which programmable devices are inferior to a full custom ASIC is the achievable logic density. In some cases, such as the AM chip, ASICs can still be the better technology. For those applications requiring an extremely high pattern density, the use of a standard-cell ASIC can be a very good compromise between the design ease of an FPGA and logic density of a full custom ASIC. To minimize the human and monetary investment required, the circuit description must make use of high level languages, which are independent of the hardware substrate, allowing easy and automatic recompilation into standard-cell chips. We followed this strategy developing the new associative memory as a standard cell chip. The new standard cell AM chip has a key role in the SVT upgrade.

Upgrades to the CDF trigger are necessary as the Tevatron instantaneous luminosity increases. The increasing luminosity results in more complex events since the rate of interactions is greater than the rate of beam crossings resulting in multiple interactions in most events. The more complex events require more trigger processing time, in particular the track trigger, reducing the amount of data CDF

can record. A large upgrade program is under development at CDF to maintain the original CDF DAQ capability at the maximum expected Tevatron luminosity ($3x10^{32}$ cm^{-2} sec^{-1}). In this program, the XFT and SVT upgrades play a central role. Our project is a significant part of these track processor upgrades.

SVT includes important functions, complementary to the AM job, in particular the Track Fitting function that produces the list of tracks found at the maximum detector resolution. The SVT Track Fitter makes use of methods based on local linear function approximation (by exploiting the starting point provided by the associative memory "roads") and learn-from-data techniques for online correction of misalignments. The experience in SVT has been that the approximations introduced for speed do not significantly affect fit performance. These higher level functions necessary inside SVT have been implemented using a general purpose board designed for the upgrade of other parts of the CDF Level 2 trigger. , The PULSer And Recorder (PULSAR) is a general purpose 9U VME interface board. The general design philosophy of Pulsar is to use one type of motherboard (with a few powerful modern FPGAs and SRAMs) to interface any user data with any industrial standard link (eg CERN S-LINK or Gigabit Ethernet) through the use of custom mezzanine cards. The design is such that users can choose which standard link to interface with via simple custom transition module or mezzanine card. The design is general enough that it can be used in many applications, within CDF or outside CDF. It can be a general purpose interface board, a standalone DAQ system (eg test beam environment) or software based trigger system when combined with modern CPUs, or even as a general purpose diagnostic test tool. Pulsar design is powerful, modular, universal and self-testable. One of the main goals of our project is to extend this flexible standard board philosophy as much as possible.

In comparison, the XFT processor has a lower degree of standardization. Dedicated boards have been produced for the different functions (although mezzanine and transition card interfaces are common with the PULSAR). Our goal for future applications is a standard system working both at LVL1 and LVL2. Standardization will reduce costs and manpower needed to develop and maintain the system.

Research Methodology – The activity of our project is organized in two different areas. The main activity is on the CDF experiment at Fermilab, where two fellow years would be spent. It includes: (a) the XFT upgrade has to be installed and optimized (b) the SVT upgrade installation has to be completed and optimized (c) the LVL1/LVL2 physics selection has to be studied and improved as a function of luminosity increase. This last point, in particular, is the most creative and difficult to be predicted. In fact the LVL1/LVL2 optimization work that follows the accelerator luminosity increase requires the definition of increasingly exclusive triggers. The work will start from (a) the study of the selected samples, understanding why the background is growing, will continue (b) defining new trigger strategies using more exclusive criteria needed to bring back the purity of the sample, (c) implementing new firmware or CPU code to implement the new trigger and (d) tests of the new conditions. This work will probably require the use of additional Pulsar boards to provide a path for the data from one processor to another. Firmware will have to be developed for these new functions. Firmware optimizations will be required to save time or to improve rejection. More complex algorithms in the LVL2 final CPUs will be necessary to increase the quality of the final selection.

The secondary activity is R&D work at Pisa (INFN) devoted to extending the use of silicon detector tracking to the level 1 trigger selection. This is an already approved INFN R&D project, named SLIM5 that could find future applications for level 1 triggering at SLHC or at a Super B factory. We plan to use the standard cell AM chip produced for CDF for a preliminary study of tracking at LVL1 and produce a faster and denser version of associative memory that could be used at LVL1 and LVL2 in future applications. We plan to use or develop general purpose FPGA-based boards, extending the Pulsar philosophy, to implement all necessary functions around the associative memory. We plan to use as much as possible hardware that can be common to both LVL1 and LVL2 in the future.

B1.2 QUALITY OF THE RESEARCHER (*Maximum 6 Pages***)**

===== Summary of Laura Sartori research activity=========

Grant Student, Ferrara University, Department of Physics (1999)

- Ferrara University, Department of Physics, Italy, March 1999. - Graduated in physics (110/110 cum laude). Title of Thesis: *A VLSI low noise front-end circuit for microstrip silicon detectors for medical imaging application*.
- Medical project: Integrated SPECT-TAC system for breast cancer research Physics: characterization of silicon detector prototypes.
- Teaching Assistant, Ferrara University, Department of Engineer (1999) - Physics Course, I Level.

Grant PhD Student, Pisa University, Department of Physics (January 2000-December 2002)

- Development of a massively parallel processor (apeNEXT) dedicated to physics simulations, in standard-cell VLSI technology, in collaboration with INFN (National Institute of Nuclear Research) electronic group.
- Development of the fast communication links used to exchange data among the apeNEXT processors.
- Development of a slow control interface, based on standard protocol, for apeNEXT processors.
- Pisa University, Department of Physics, Italy, October 2004 - Ph.D. in Applied Physics. Title of the Thesis: *The apeNEXT project: development of architectural design of a massively parallel processor optimized for numerical simulations of LQCD*

Post-PhD Position, Ferrara University Department of Physics (January 2003– June 2004)

- Development of a VLSI standard-cell based Content Addressable Memory system for pattern recognition used for track finding in High Energy Experiments.
- Architectural development, hardware description, functional simulation, physical synthesis, placement and routing and static timing analysis.
- Teaching Assistant, Ferrara University. Department of Computer Science (2003). – Computer Architecture Course.

Design Engineer, STMicroelectronics Srl, Milano, Italy (July 2004 –present)

- Development and testing of the digital part of Flash-Nand Memory devices.
- Development of a serial interface for Flash-Nand Memory device.
- Hardware description, functional simulation and verification, placement and routing of memory device and improvement of the IC design flow.

Courses

- Chip Architecture Training, Synopsys, Milano (December 2000)
- Circuit Design for Digital Communications, Ecole Polytechnique Federale de Lausanne, Lausanne (September 2000)
- Electronic of digital system: II level, University of Pisa, Department of Electronic Engineer. Final mark: 30/30 (2000)
- Introduction to analogue signal processing and Op-amp design, University of Brunel, Uxbridge, GB (September 1998)

Potential of the researcher to meet the objectives of the proposed project

I have extensive experience in VLSI design. I worked on three important research projects, all of them providing important skills in areas related to our research project:

- I designed front end electronics for silicon detectors, getting knowledge on detector readout. This is an interesting item for the CDF experiment, that uses silicon detectors in its tracking system.

- I worked on the development of a key electronic device for the *apeNEXT supercomputer*, gaining knowledge on parallel and complex computer architectures and on standard cell technologies. My expertise in this field is particularly interesting for application to the CDF online trigger processors. In the framework of the apeNEXT project I also obtained basic knowledge on programmable logic by collaborating on the design of the control board of the processor.
- The most important experience for the online tracking at CDF is my activity as post-doc in Ferrara, Italy. I was responsible for designing the standard-cell associative memory chip(AM) for the SVT processor. I worked directly on all steps of the project and managed the work of collaborators to satisfy the needs of the experiments very tight schedule. Under my supervision, a student and a technician developed the Boundary Scan functions of the device and a physicist performed the extensive simulation tests to guarantee that all parts of the chip functioned perfectly before the prototype production.
- I also have experience in an international silicon company (STMicrolectronics) as design engineer. After less than one year I proposed a patent, concerning the architecture of Flash-Nand memories, and made strong contributions to improving the standard design flow of my team.

Since the first activity performed as a student in Ferrara during 1999, I demonstrated the capability to take responsibility for a design and to bring it to successful completion. My thesis was developed in the framework of a medical project: the realization of a digital imaging system based on silicon detector. My main contribution was the development of a Front End analog VLSI circuit design (0.8 um CMOS process) starting from the constraints imposed by the medical application: low noise and good time resolution, which are common requirements in experiments involving silicon detector.
I presented my results at the "1st International Workshop on Radiation Imaging Detectors" (Sweden, 1998) The work was also reported in the paper "Low-noise front-end amplifier and channel encoder for a 2-D X-ray digital imaging system with single photon counting capability", Nuclear Instruments and Methods in Physics Research, 2001, A460, 213-220.

During my PhD studies (January 2000-December 2003, Pisa University) I demonstrated the same independent thinking and initiative applied to a much larger and more complex project. I worked on a very important device for a massively parallel processor, optimized for numerical simulations of Lattice QCD (apeNEXT project). My contribution centered on the architectural design of the processor, in collaboration with members of the APE group at DESY, Ferrara and Pisa. I was involved in all phases of the back-end design of the processor. The term back-end refers to all the activities associated to the actual floorplanning, placement and routing of the electronics device of the processor, in the verification that the electrical and timing properties are as expected and the simulation of the final system, prior to manufacturing.

I presented the results in a seminar at Columbia University (August 2003). The title of the seminar is: The apeNEXT project". The papers "The apeNEXT project", Nucl.Phys.B (Proc Suppl) 140 (2005), 176-182 and "APE computer – Past, Present and Future". Computer Physics Communications, 147, (2002), 402-409 describe this work.

I also collaborated in the development of the slow control interface between the host PC and the processors, based on the standard protocol called I2C. The result is a system in which a single PCI board could control up to 64 processors. I presented the preliminary results to the "International Conference on Computer Communication and Control Technologies" 2003 Orlando.

As a post-doc I clearly showed my capability to manage a group and to realize in a short period (less than one year) a working complex device (10x10 mm die, full of logic at 95%).

All the steps of the design were under my supervision or directly done by me. I defined the chip architecture and wrote the chip specifications, I coordinated the VHDL logic description. Since the pattern array for 5000 patterns is very regular, like a memory, I manually optimized the placement. The pattern bank occupies most of the chip area and it is important to exploit the array regularity as much as possible. Only a manual study of the structure could guarantee this result. The remaining logic was handled by automatic tools for placing and routing. The 5000/pattern chip was extensively simulated with random-generated test vectors that exercised all possible configuration conditions, generated random patterns and random inputs. Timing information was extracted and checked. A few paths were optimized. Finally, standard scripts and procedures were provided to obtain in a short time a chip with modifications.

I submitted the project to UMC through IMEC for the MPW run and after that I submitted the same project for a pilot run. The chosen technology in 2003 (UMC 0.18 micron) was not the most powerful (0.13 micron was the best at that time), but the most convenient (92000 euros for 50 prototype chips). The final device was produced with a yield of approximately 70%, as expected given the die size.

The results were presented at the IEEE Nuclear Science Symposium & Medical Imaging Conference, October 23-29 2005, Puerto Rico and the following papers were submitted: "Vertexing at CDF" (to Elsevier Science) "The AM++ Board for the Silicon Vertex Tracker upgrade at CDF", "A VLSI Processor for Fast Track Finding Based on Content Addressable Memories" (to IEEE Transaction Nuclear Science).

After just a few months as design engineer at STMicroelectronics, I demonstrated the capability to propose new solutions to technical and planning problems. I developed a serial interface for memory devices. This work is now described in detail in an European patent application ("Memory architecture with serial peripheral interface"). I have introduced improvements and changes in the traditional design flow adopted by my team (Designer group), by using new and modern tools (physical synthesis tool, static timing analysis tool, reduction of simulation time) demonstrating team skill for interacting with CAD group.

In conclusion I already have extensive knowledge of the project that would be the field of application of my fellowship. I have technological skills very relevant for our proposal and I have demonstrated organization and managerial capabilities that will allow me to play an important role in the CDF trigger group.

Potential to acquire new knowledge

My experience is limited to chip design and my activity has been limited to Italy. The Fermilab laboratory and the CDF experiment would be a wonderful environment to move my career ahead and to give an international dimension to my knowledge. The CDF collaboration consists of 58 institutions from around the world. Moreover, the CDF Level 2 trigger system is a very complex architecture based on several different technologies where I could easily acquire new knowledge. The VLSI device I designed is the most powerful but least flexible computing component of the system. I can learn the use of programmable logic and the use of level 2 processors to be able to compare the potentialities of different technologies.

A totally new field for me would be associated with understanding the CDF trigger selection criteria and analyzing their dependence on the accelerator luminosity, in order to find firmware optimizations. This is a high-level and creative work that starts from an understanding of the physics problems and goes all the way to the development of hardware-firmware solutions. A clear example is the b-quark selection at LVL2. The impact parameter resolution of tracks found by the SVT decreases as the luminosity increases. This is probably due to the fact that the larger hit occupancy favors the increase of fake tracks with large

impact parameter. As a consequence, the purity of the LVL2 selected samples decreases and more selective criteria may be required to control trigger rates.

My final goal (and for our group more generally) is to learn as much as possible about problems of the CDF online tracking system so we can leverage future technological developments in microelectronics to suitable solutions for high energy physics. In this sense, I should understand how to improve flexibility and ease of use for the trigger system as a whole, to allow migration to different experiments with tailoring efforts.

I will be able to learn which diagnostic tools should be developed during these years of data taking. All the chips we have in SVT have boundary scan capabilities and we can access information through the VME interface. We have standalone programs that check the connectivity on the boards. The acquired experience on monitoring and maintaining the system will be of great importance for more complex future applications.

We should exercise automation of technological follow-up of digital electronics developments, producing clean project descriptions using high level languages and automatic compilation into the most advanced devices at time of construction. This approach has already been adopted during the SVT upgrade to exploit to the best and for a long interval of time the initial designing efforts, simplifying further developments and applications to future generation experiments.

The experience I can collect working for two years on the CDF trigger will be very important for the work I can do when I will return to INFN Pisa. I will be able to evaluate the best technology to implement an algorithm or different parts of it comparing costs and performances of dedicated VLSI devices, programmable logic or CPUs. Some mixture of these technologies may be the best choice as it is now the case for tracking triggers at CDF. This experience is of particular value if we consider that this kind of knowledge is substantially missing in Italy. We are experiencing an backward situation, in which electronics is so powerful that high energy experiments could easily implement real time selections at very high rates (very fast algorithms) with offline precisions, but very little is done in this direction, possibly because the community is not aware of the potentiality of the available electronics.

I will be able to disseminate to the Italian high energy physics community my experience, will be able to exploit my research outcomes and I will be able to contribute to future funding provision on this field.

The scientist in charge is Paola Giannetti from Istituto Nazionale di Fisica Nucleare – Sezione di Pisa. Mauro Dell'Orso will cooperate with Paola Giannetti as co-supervisor.

Peter Wilson will be my supervisor in Fermilab.

I will collaborate at the level of 10% of my time, also with Professor Melvyn J. Shochet from the Enrico Fermi Institute at the University of Chicago. The Enrico Fermi Institute is located near Fermilab (one hour by car) and is a wonderful opportunity for my work. Professor Melvyn J. Shochet and the Enrico Fermi Institute have been in CDF and have been a very important part of the SVT and Pulsar projects since the beginning. The Enrico Fermi Institute is very attractive for its courses, seminars. The Enrico Fermi Institute has also a very good electrical engineering group. It has extensive experience in electronics design. Engineers in these groups have extensive experience on projects with CDF, in particular with SVT and the Pulsar project for the Level 2 trigger selection.

Main Publication

- Patent proposal: Memory architecture with serial peripheral interface (European patent application)

- L.Sartori et al. “Low noise front-end Amplifier and channel encoder for a 2-D X-ray digital imaging system with single photon counting capability”. Nucl.Instr. and Meth. 2001, A460,213-220. **Abstract**: *We describe two VLSI CMOS ICs for 2-D X-ray digital imaging system with single photon counting capability: a low front-end analog amplifier and an 80 MHz synchronous digital encoder. Our VLSI system will be optimized to perform X-Y coincidences with double-sided microstrip digital detector. The main application we are investigating is stereotaxic mammography, because of low X-ray energy used and the small area involved.*
- N.Belcari et al. “Measurement of photoelectron yield from scintillating fibers coupled to a YAP:Ce matrix”, Nucl.Instr and Meth. 2001, A461, 413-415.
- A.Del Guerra et all. “An integrated PET-SPECT small animal imager: preliminary results”, IEEE Trans.Nucl.Sci. 2000,NSS47,1537-1540.
- M.Gambaccini et all. “Development of a small field quasi-monochromatic computer tomography system”, Physica Medica 2000, XVI(3), 161-164.
- The APE Collaboration. “The apeNEXT project” Nucl.Phys.B (proc.Suppl.)140, (2005),176-182. **Abstract**: *We present the current status of the apeNEXT project. Aim of this project is the development of a next generation of APE machines, which will provide multi-teraflop computing power. Like previous machine, apeNEXT is based on a custom designed processor, which is specifically optimized for simulating QCD. We discuss the machine design, report on benchmarks, and give an overview on the status of the software development.*
- F.Bodin et al. “APE computer – Past, Present and Future”. Computer physics Communications, 147, (2002), 402-409.
- R.Ammendola et al. “Status of the ApeNext project”. Nucl.phys.B (Proc.Suppl.) 119, (2003), 1038-1040.
- F.Bodin et al. “The APENEXT project” Nucl.Phys.B (Proc.Suppl) 106, (2002),173-176.
- A.Bartolini et al. “Status of APE1000”. Nucl.Phys.B (Proc.Suppl.) 106, (2002), 1043-1045.
- F.Bodin et al. “The apeNEXT project” Talk from 2003 Computing in High Energy and Nuclear Physics (CHEP03), Jun 2003, La Jolla, CA,USA. Published in eConf C0303241:THIT005,2003.
  F.Bodin et al “apeNEXT:A multi-Tflops Computer for simulations in Lattice Gauge Theory. Poster at the XXIII Physics in collisions conference (PIC03), Zeuthen, Germany, June 2003.

ENDPAGE

HUMAN RESOURCES AND MOBILITY (HRM)
ACTIVITY

MARIE CURIE ACTIONS
Marie Curie Outgoing International Fellowships (OIF)

PART B Section 1

"POT"