EUROPEAN COMMISSION

7th Framework Programme for
Research, technological
Development and Demonstration

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A1: Content

Proposal Number	609765	Proposal Acronym	NEURONS
Project Type	CP-FP-INFSO		

General Information

Proposal Title	advaNced associativE memory architectUres for massive data pROcessiNg parallelism).

Duration in months	36	Call (part) Identifier	FP7-ICT-2013-10

Activity code(s) most relevant to your topic	ICT-2013.3.4	ICT-2013.3.4	

Abstract (max. 2000 chars)

The NEURONS project brings together embedded computing and high-performance computing teams jointly addressing challenges common in these two areas and magnified by the ubiquity of many-cores and heterogeneity across the whole computing spectrum by:
• Designing and fabricating innovative cost effective and low energy data-intensive parallel computing platforms to provide high levels of reliability, efficiency, availability, and scalability.
• Developing of innovative approaches and algorithms to parallel programming to address the processing of data on data-intensive systems.
• Demonstrating the system capability in applications that can exploit new computing paradigms and determining how they should evolve to support emerging data-intensive applications.

The main technological objectives of NEURONS are:
• Development of a novel multicore “Associative Memory for Multi-Applications” chip (AMMA-chip) in aggressive technology nodes (65 nm).
• Complement the AMMA functionality with Field Programmable Gate Arrays (FPGA) highly parallelized algorithms.
• Demonstration of the AMMA in case scenarios requiring massive data paralleled processing such as Computer Vision, Medical Imaging, High Energy Physics and Nuclear Fusion.
• Development of software algorithms for the foreseen demonstration scenarios requiring high parallelism data intensive processing.
• Design of novel computing architectures in the 3D domain.

The NEURONS project will pave the way towards new breakthroughs in the design, operations, and control of embedded computing systems requiring the control of mixed criticalities (i.e. Systems of Systems) opening multifaceted applications in industry (i.e. control of industrial processes), engineering (i.e. real-time context aware vehicles), healthcare (i.e. dynamic diagnostics), etc. The technology developed by the NEURONS project also steps ahead in materializing the ultimate computing paradigms such as cognitive computation and brain-like computing systems.

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Free keywords

embedded computing, high-performance computing, associative memory, many-cores, parallelization, system of systems, big data, data-intensive systems, mixed criticalities

a) Has this proposal (or a very similar one) been previously submitted to a call for proposals of the 7th EU RTD Framework Programme ? ○ Yes ◉ No

b) Is this proposal (or a similar one) currently being submitted to another call under FP7 ? ○ Yes ◉ No

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A2.1 Participant #1

INFN

If your organisation has already registered for FP7, enter your Participant Identity Code ***999992789***

Legal Name ***ISTITUTO NAZIONALE DI FISICA NUCLEARE***

Organisation short name ***INFN***

Administrative data (legal address)

Street name ***Via Enrico Fermi*** Number ***40***

Town ***FRASCATI***

Postal Code / Cedex ***00044***

Country ***IT***

Internet homepage ***www.infn.it***

Status of your organisation

Certain types of organisations benefit from special conditions under the FP7 participant rules. The Commission also collects data for statistical purposes.

The guidance notes will help you complete this section.

Please 'tick' the relevant box(es) if your organisation falls into one ore more of the following categories.

Non-profit organisation	(•) Yes	( ) No
Public body	(•) Yes	( ) No
Research organisation	(•) Yes	( ) No
Higher or secondary education establishment	( ) Yes	(•) No

Main area of activity (NACE code) 73.1

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1. Is your number of employees smaller than 250? (full time equivalent)	○ Yes	○ No
2. Is your annual turnover smaller than € 50 million?	○ Yes	○ No
3. Is your annual balance sheet total smaller than € 43 million?	○ Yes	○ No
4. Are you an autonomous legal entity?	○ Yes	○ No

You are NOT an SME if your answer to question 1 is "NO" and/or your answer to both questions 2 and 3 is "NO".

In all other cases, you might conform to the Commission's definition of an SME.

Please check the additional conditions given in the guidance notes to the forms.

Following this check, do you conform to the Commission's definition of an SME? ○ Yes ◉ No

Dependencies with (an)other participant(s)

Are there dependencies between your organisation and (an)other participant(s) in this proposal? ○ Yes ◉ No

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Contact point - Person in charge for participant #1

For the co-ordinator (Participant #1) this person is the one who the Commission will contact in the first instance.

Family name* ***Giannetti*** First name(s)* ***Paola***

Title Dr.

○ Male ◉ Female

Position in the organisation Researcher director

Department/Faculty/Institute/Laboratory name/... INFN-Pisa

Address ☐ Same as legal address

Street name Edificio C - Polo Fibonacci, Largo B. Pontecorvo Number 3

Town Pisa Postal Code/Cedex 56127

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Phone1* + ***39*** ***0502214393*** Phone2 + 39 0502214593

Fax + 39 0502214317 E-mail* ***paola.giannetti@pi.infn.it***

** Contact details can only be changed by the Proposal Coordinator via the "Step 4 – Manage Your Related Parties" screen.*

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A2.2 Participant #2

CNRS

If your organisation has already registered for FP7, enter your Participant Identity Code ***999997930***

Legal Name ***CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE***

Organisation short name ***CNRS***

Administrative data (legal address)

Street name ***Rue Michel -Ange*** Number ***3***

Town ***PARIS***

Postal Code / Cedex ***75794***

Country ***FR***

Internet homepage ***www.cnrs.fr***

Status of your organisation

Certain types of organisations benefit from special conditions under the FP7 participant rules. The Commission also collects data for statistical purposes.

The guidance notes will help you complete this section.

Please 'tick' the relevant box(es) if your organisation falls into one ore more of the following categories.

Non-profit organisation	(•) Yes	( ) No
Public body	(•) Yes	( ) No
Research organisation	(•) Yes	( ) No
Higher or secondary education establishment	( ) Yes	(•) No

Main area of activity (NACE code) 73.1

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1. Is your number of employees smaller than 250? (full time equivalent)	○ Yes	○ No
2. Is your annual turnover smaller than € 50 million?	○ Yes	○ No
3. Is your annual balance sheet total smaller than € 43 million?	○ Yes	○ No
4. Are you an autonomous legal entity?	○ Yes	○ No

You are NOT an SME if your answer to question 1 is "NO" and/or your answer to both questions 2 and 3 is "NO".

In all other cases, you might conform to the Commission's definition of an SME.

Please check the additional conditions given in the guidance notes to the forms.

Following this check, do you conform to the Commission's definition of an SME? ○ Yes ◉ No

Dependencies with (an)other participant(s)

Are there dependencies between your organisation and (an)other participant(s) in this proposal? ○ Yes ◉ No

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Contact point - Person in charge for participant #2

For the co-ordinator (Participant #1) this person is the one who the Commission will contact in the first instance.

Family name* ***Calderini*** First name(s)* ***Giovanni***

Title Dr.

(•) Male ( ) Female

Position in the organisation Director of Research

Department/Faculty/Institute/Laboratory name/... LPNHE

Address ☐ Same as legal address

Street name Place Jussieu Number 4

Town Paris Postal Code/Cedex 75252

Country FR

Phone1* + ***33*** ***144272325*** Phone2 +

Fax +

E-mail* ***giovanni.calderini@lpnhe.in2p3.fr***

** Contact details can only be changed by the Proposal Coordinator via the "Step 4 – Manage Your Related Parties" screen.*

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A2.3 Participant #3

Microtest

If your organisation has already registered for FP7, enter your Participant Identity Code ***986573518***

Legal Name ***Microtest S.r.l.***

Organisation short name ***Microtest***

Administrative data (legal address)

Street name ***via Galeotta*** Number ***9/A***

Town ***Altopascio (LU)***

Postal Code / Cedex ***55011***

Country ***IT***

Internet homepage ***www.microtest.net***

Status of your organisation

Certain types of organisations benefit from special conditions under the FP7 participant rules. The Commission also collects data for statistical purposes.

The guidance notes will help you complete this section.

Please 'tick' the relevant box(es) if your organisation falls into one ore more of the following categories.

Non-profit organisation	○ Yes	◉ No
Public body	○ Yes	◉ No
Research organisation	○ Yes	◉ No
Higher or secondary education establishment	○ Yes	◉ No

Main area of activity (NACE code) DL

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1. Is your number of employees smaller than 250? (full time equivalent)	(•) Yes	( ) No
2. Is your annual turnover smaller than € 50 million?	(•) Yes	( ) No
3. Is your annual balance sheet total smaller than € 43 million?	(•) Yes	( ) No
4. Are you an autonomous legal entity?	(•) Yes	( ) No

You are NOT an SME if your answer to question 1 is "NO" and/or your answer to both questions 2 and 3 is "NO".

In all other cases, you might conform to the Commission's definition of an SME.

Please check the additional conditions given in the guidance notes to the forms.

Following this check, do you conform to the Commission's definition of an SME? (•) Yes ( ) No

Dependencies with (an)other participant(s)

Are there dependencies between your organisation and (an)other participant(s) in this proposal? ( ) Yes (•) No

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Contact point - Person in charge for participant #3

For the co-ordinator (Participant #1) this person is the one who the Commission will contact in the first instance.

Family name* ***Lupi*** First name(s)* ***Moreno***

Title Mr.

(•) Male ( ) Female

Position in the organisation Technical manager

Department/Faculty/Institute/Laboratory name/... CAEN

Address ☒ Same as legal address

Street name via Galeotta Number 9/A

Town Altopascio (LU) Postal Code/Cedex 55011

Country IT

Phone1* + ***39*** ***0583269651*** Phone2 +

Fax + 39 0583269631 E-mail* ***moreno.lupi@microtest.net***

** Contact details can only be changed by the Proposal Coordinator via the "Step 4 – Manage Your Related Parties" screen.*

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A2.4 Participant #4

AUTH

If your organisation has already registered for FP7, enter your Participant Identity Code	***999895692***
Legal Name	***ARISTOTELIO PANEPISTIMIO THESSALONIKIS***
Organisation short name	***AUTH***

Administrative data (legal address)

Street name	***Administration Building, University Campus***	Number	
Town	***THESSALONIKI***		
Postal Code / Cedex	***54124***		
Country	***EL***		
Internet homepage	***www.auth.gr***		

Status of your organisation

Certain types of organisations benefit from special conditions under the FP7 participant rules. The Commission also collects data for statistical purposes.

The guidance notes will help you complete this section.

Please 'tick' the relevant box(es) if your organisation falls into one ore more of the following categories.

Non-profit organisation	(•) Yes	( ) No
Public body	(•) Yes	( ) No
Research organisation	(•) Yes	( ) No
Higher or secondary education establishment	(•) Yes	( ) No

Main area of activity (NACE code)	80.3

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1. Is your number of employees smaller than 250? (full time equivalent)	○ Yes	○ No
2. Is your annual turnover smaller than € 50 million?	○ Yes	○ No
3. Is your annual balance sheet total smaller than € 43 million?	○ Yes	○ No
4. Are you an autonomous legal entity?	○ Yes	○ No

You are NOT an SME if your answer to question 1 is "NO" and/or your answer to both questions 2 and 3 is "NO".

In all other cases, you might conform to the Commission's definition of an SME.

Please check the additional conditions given in the guidance notes to the forms.

Following this check, do you conform to the Commission's definition of an SME? ○ Yes ◉ No

Dependencies with (an)other participant(s)

Are there dependencies between your organisation and (an)other participant(s) in this proposal? ○ Yes ◉ No

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Contact point - Person in charge for participant #4

For the co-ordinator (Participant #1) this person is the one who the Commission will contact in the first instance.

Family name* ***Kordas*** First name(s)* ***Konstantinos***

Title Dr.

(•) Male ( ) Female

Position in the organisation Lecturer

Department/Faculty/Institute/Laboratory name/... Division of Nuclear and Particle Physics, Dept. Physics

Address ☐ Same as legal address

Street name Faculty of Sciences Building, University Campus Number 1

Town Thessaloniki Postal Code/Cedex 54124

Country EL

Phone1* + ***30*** ***2310994121*** Phone2 +

Fax + 30 2310998209 E-mail* ***kordas@physics.auth.gr***

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A2.5 Participant #5

UNIGE

If your organisation has already registered for FP7, enter your Participant Identity Code ***999974650***

Legal Name ***UNIVERSITE DE GENEVE***

Organisation short name ***UNIGE***

Administrative data (legal address)

Street name ***Rue du General Dufour*** Number ***24***

Town ***GENEVE***

Postal Code / Cedex ***1211***

Country ***CH***

Internet homepage ***www.unige.ch***

Status of your organisation

Certain types of organisations benefit from special conditions under the FP7 participant rules. The Commission also collects data for statistical purposes.

The guidance notes will help you complete this section.

Please 'tick' the relevant box(es) if your organisation falls into one ore more of the following categories.

Non-profit organisation	(•) Yes	( ) No
Public body	(•) Yes	( ) No
Research organisation	(•) Yes	( ) No
Higher or secondary education establishment	(•) Yes	( ) No

Main area of activity (NACE code) 80.3

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1. Is your number of employees smaller than 250? (full time equivalent)	○ Yes	○ No
2. Is your annual turnover smaller than € 50 million?	○ Yes	○ No
3. Is your annual balance sheet total smaller than € 43 million?	○ Yes	○ No
4. Are you an autonomous legal entity?	○ Yes	○ No

You are NOT an SME if your answer to question 1 is "NO" and/or your answer to both questions 2 and 3 is "NO".

In all other cases, you might conform to the Commission's definition of an SME.

Please check the additional conditions given in the guidance notes to the forms.

Following this check, do you conform to the Commission's definition of an SME? ○ Yes ◉ No

Dependencies with (an)other participant(s)

Are there dependencies between your organisation and (an)other participant(s) in this proposal? ○ Yes ◉ No

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Contact point - Person in charge for participant #5

For the co-ordinator (Participant #1) this person is the one who the Commission will contact in the first instance.

Family name* ***Wu*** First name(s)* ***Xin***

Title Prof.

(•) Male ( ) Female

Position in the organisation Associate professor

Department/Faculty/Institute/Laboratory name/... Département de physique nucléaire et corpusculaire (DPNC)

Address ☐ Same as legal address

Street name Quai Ernest-Anserme Number 4

Town Geneva Postal Code/Cedex 1211

Country CH

Phone1* + ***41*** ***223796272*** Phone2 +

Fax +

E-mail* ***xin.wu@cern.ch***

** Contact details can only be changed by the Proposal Coordinator via the "Step 4 – Manage Your Related Parties" screen.*

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A2.6 Participant #6

UNIFI

If your organisation has already registered for FP7, enter your Participant Identity Code	***999895789***
Legal Name	***UNIVERSITA DEGLI STUDI DI FIRENZE***
Organisation short name	***UNIFI***

Administrative data (legal address)

Street name	***Piazza San Marco***	Number	***4***
Town	***Florence***		
Postal Code / Cedex	***50121***		
Country	***IT***		
Internet homepage	***http://www.unifi.it***		

Status of your organisation

Certain types of organisations benefit from special conditions under the FP7 participant rules. The Commission also collects data for statistical purposes.

The guidance notes will help you complete this section.

Please 'tick' the relevant box(es) if your organisation falls into one ore more of the following categories.

Non-profit organisation	(•) Yes	( ) No
Public body	(•) Yes	( ) No
Research organisation	(•) Yes	( ) No
Higher or secondary education establishment	(•) Yes	( ) No

Main area of activity (NACE code)	80.3

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1. Is your number of employees smaller than 250? (full time equivalent)	○ Yes	○ No
2. Is your annual turnover smaller than € 50 million?	○ Yes	○ No
3. Is your annual balance sheet total smaller than € 43 million?	○ Yes	○ No
4. Are you an autonomous legal entity?	○ Yes	○ No

You are NOT an SME if your answer to question 1 is "NO" and/or your answer to both questions 2 and 3 is "NO".

In all other cases, you might conform to the Commission's definition of an SME.

Please check the additional conditions given in the guidance notes to the forms.

Following this check, do you conform to the Commission's definition of an SME? ○ Yes ◉ No

Dependencies with (an)other participant(s)

Are there dependencies between your organisation and (an)other participant(s) in this proposal? ○ Yes ◉ No

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Contact point - Person in charge for participant #6

For the co-ordinator (Participant #1) this person is the one who the Commission will contact in the first instance.

Family name* ***Del Viva*** First name(s)* ***Michela***

Title Dr.

○ Male ◉ Female

Position in the organisation Assistant Professor

Department/Faculty/Institute/Laboratory name/... Department of Psychology

Address ☐ Same as legal address

Street name Via di San Salvi, Complesso di San Salvi, Padiglione 26 Number 12

Town Firenze Postal Code/Cedex 50135

Country IT

Phone1* + ***39*** ***3277052969*** Phone2 +

Fax + E-mail* ***michela@in.cnr.it***

** Contact details can only be changed by the Proposal Coordinator via the "Step 4 – Manage Your Related Parties" screen.*

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A2.7 Participant #7

PRIELE

If your organisation has already registered for FP7, enter your Participant Identity Code ***984440488***

Legal Name ***Prisma Electronics ABEE***

Organisation short name ***PRIELE***

Administrative data (legal address)

Street name ***Dimokratias Avenue*** Number ***87***

Town ***ALEXANDROUPOLIS***

Postal Code / Cedex ***68100***

Country ***EL***

Internet homepage ***www.prisma.gr***

Status of your organisation

Certain types of organisations benefit from special conditions under the FP7 participant rules. The Commission also collects data for statistical purposes.

The guidance notes will help you complete this section.

Please 'tick' the relevant box(es) if your organisation falls into one ore more of the following categories.

Non-profit organisation	○ Yes	◉ No
Public body	○ Yes	◉ No
Research organisation	○ Yes	◉ No
Higher or secondary education establishment	○ Yes	◉ No

Main area of activity (NACE code) DL

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1. Is your number of employees smaller than 250? (full time equivalent)	(•) Yes	( ) No
2. Is your annual turnover smaller than € 50 million?	(•) Yes	( ) No
3. Is your annual balance sheet total smaller than € 43 million?	(•) Yes	( ) No
4. Are you an autonomous legal entity?	(•) Yes	( ) No

You are NOT an SME if your answer to question 1 is "NO" and/or your answer to both questions 2 and 3 is "NO".

In all other cases, you might conform to the Commission's definition of an SME.

Please check the additional conditions given in the guidance notes to the forms.

Following this check, do you conform to the Commission's definition of an SME? (•) Yes ( ) No

Dependencies with (an)other participant(s)

Are there dependencies between your organisation and (an)other participant(s) in this proposal? ( ) Yes (•) No

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Contact point - Person in charge for participant #7

For the co-ordinator (Participant #1) this person is the one who the Commission will contact in the first instance.

Family name* ***Mermigli*** First name(s)* ***Konstantina***

Title Mrs ○ Male ◉ Female

Position in the organisation R&D projects manager

Department/Faculty/Institute/Laboratory name/... PRISMA

Address ☐ Same as legal address

Street name El Venizelou, Nea Smirni Number 126

Town Athens Postal Code/Cedex

Country EL

Phone1* + ***30*** ***2109313110*** Phone2 +

Fax + E-mail* ***kmerm@prisma.gr***

** Contact details can only be changed by the Proposal Coordinator via the "Step 4 – Manage Your Related Parties" screen.*

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A2.8 Participant #8

UHEI

If your organisation has already registered for FP7, enter your Participant Identity Code ***999987648***

Legal Name ***RUPRECHT-KARLS-UNIVERSITAET HEIDELBERG***

Organisation short name ***UHEI***

Administrative data (legal address)

Street name ***SEMINARSTRASSE*** Number ***2***

Town ***HEIDELBERG***

Postal Code / Cedex ***69117***

Country ***DE***

Internet homepage ***www.uni-heidelberg.de***

Status of your organisation

Certain types of organisations benefit from special conditions under the FP7 participant rules. The Commission also collects data for statistical purposes.

The guidance notes will help you complete this section.

Please 'tick' the relevant box(es) if your organisation falls into one ore more of the following categories.

Non-profit organisation	(•) Yes	( ) No
Public body	(•) Yes	( ) No
Research organisation	(•) Yes	( ) No
Higher or secondary education establishment	(•) Yes	( ) No

Main area of activity (NACE code) 80.3

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1. Is your number of employees smaller than 250? (full time equivalent)	○ Yes	○ No
2. Is your annual turnover smaller than € 50 million?	○ Yes	○ No
3. Is your annual balance sheet total smaller than € 43 million?	○ Yes	○ No
4. Are you an autonomous legal entity?	○ Yes	○ No

You are NOT an SME if your answer to question 1 is "NO" and/or your answer to both questions 2 and 3 is "NO".

In all other cases, you might conform to the Commission's definition of an SME.

Please check the additional conditions given in the guidance notes to the forms.

Following this check, do you conform to the Commission's definition of an SME? ○ Yes ◉ No

Dependencies with (an)other participant(s)

Are there dependencies between your organisation and (an)other participant(s) in this proposal? ○ Yes ◉ No

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Contact point - Person in charge for participant #8

For the co-ordinator (Participant #1) this person is the one who the Commission will contact in the first instance.

Family name* ***Soltveit*** First name(s)* ***Hans Kristian***

Title Mr.

(•) Male ( ) Female

Position in the organisation Scientist

Department/Faculty/Institute/Laboratory name/... Physikalisches Institut der Universität Heidelberg

Address ☐ Same as legal address

Street name Im Neuenheimer Feld Number 226

Town Heidelberg Postal Code/Cedex 69120

Country DE

Phone1* + ***49*** ***622119409*** Phone2 + 49 6221 19409

Fax + E-mail* ***soltveit@physi.uni-heidelberg.de***

** Contact details can only be changed by the Proposal Coordinator via the "Step 4 – Manage Your Related Parties" screen.*

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A2.9 Participant #9

IMEC

If your organisation has already registered for FP7, enter your Participant Identity Code ***999981149***

Legal Name ***INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW***

Organisation short name ***IMEC***

Administrative data (legal address)

Street name ***Kapeldreef*** Number ***75***

Town ***LEUVEN***

Postal Code / Cedex ***3001***

Country ***BE***

Internet homepage ***www.imec.be***

Status of your organisation

Certain types of organisations benefit from special conditions under the FP7 participant rules. The Commission also collects data for statistical purposes.

The guidance notes will help you complete this section.

Please 'tick' the relevant box(es) if your organisation falls into one ore more of the following categories.

Non-profit organisation	(•) Yes	( ) No
Public body	( ) Yes	(•) No
Research organisation	(•) Yes	( ) No
Higher or secondary education establishment	( ) Yes	(•) No

Main area of activity (NACE code) 73.1

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1. Is your number of employees smaller than 250? (full time equivalent)	○ Yes	◉ No
2. Is your annual turnover smaller than € 50 million?	○ Yes	◉ No
3. Is your annual balance sheet total smaller than € 43 million?	○ Yes	◉ No
4. Are you an autonomous legal entity?	◉ Yes	○ No

You are NOT an SME if your answer to question 1 is "NO" and/or your answer to both questions 2 and 3 is "NO".

In all other cases, you might conform to the Commission's definition of an SME.

Please check the additional conditions given in the guidance notes to the forms.

Following this check, do you conform to the Commission's definition of an SME? ○ Yes ◉ No

Dependencies with (an)other participant(s)

Are there dependencies between your organisation and (an)other participant(s) in this proposal? ○ Yes ◉ No

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Contact point - Person in charge for participant #9

For the co-ordinator (Participant #1) this person is the one who the Commission will contact in the first instance.

Family name* ***Das*** First name(s)* ***Carl***

Title Dr.

(•) Male ( ) Female

Position in the organisation Director of the ASIC Services

Department/Faculty/Institute/Laboratory name/... INVOMEC

Address ☒ Same as legal address

Street name Kapeldreef Number 75

Town LEUVEN Postal Code/Cedex 3001

Country BE

Phone1* + ***32*** ***16281248*** Phone2 + 32 16281248

Fax + E-mail* ***carl.das@imec.be***

** Contact details can only be changed by the Proposal Coordinator via the "Step 4 – Manage Your Related Parties" screen.*

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A2.10 Participant #10

CAEN

If your organisation has already registered for FP7, enter your Participant Identity Code ***973290338***

Legal Name ***COSTRUZIONI APPARECCHIATURE ELETTRONICHE NUCLEARI C.A.E.N. SPA***

Organisation short name ***CAEN***

Administrative data (legal address)

Street name ***VIA VETRAIA*** Number ***11***

Town ***VIAREGGIO***

Postal Code / Cedex ***55049***

Country ***IT***

Internet homepage ***www.caen.it***

Status of your organisation

Certain types of organisations benefit from special conditions under the FP7 participant rules. The Commission also collects data for statistical purposes.

The guidance notes will help you complete this section.

Please 'tick' the relevant box(es) if your organisation falls into one ore more of the following categories.

Non-profit organisation	○ Yes	◉ No
Public body	○ Yes	◉ No
Research organisation	○ Yes	◉ No
Higher or secondary education establishment	○ Yes	◉ No

Main area of activity (NACE code) 33

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1. Is your number of employees smaller than 250? (full time equivalent)	(•) Yes	( ) No
2. Is your annual turnover smaller than € 50 million?	(•) Yes	( ) No
3. Is your annual balance sheet total smaller than € 43 million?	(•) Yes	( ) No
4. Are you an autonomous legal entity?	(•) Yes	( ) No

You are NOT an SME if your answer to question 1 is "NO" and/or your answer to both questions 2 and 3 is "NO".

In all other cases, you might conform to the Commission's definition of an SME.

Please check the additional conditions given in the guidance notes to the forms.

Following this check, do you conform to the Commission's definition of an SME? (•) Yes ( ) No

Dependencies with (an)other participant(s)

Are there dependencies between your organisation and (an)other participant(s) in this proposal? ( ) Yes (•) No

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Contact point - Person in charge for participant #10

For the co-ordinator (Participant #1) this person is the one who the Commission will contact in the first instance.

Family name* ***Petrucci*** First name(s)* ***Stefano***

Title Mr.

(•) Male ( ) Female

Position in the organisation Marketing manager

Department/Faculty/Institute/Laboratory name/... Marketing

Address ☒ Same as legal address

Street name VIA VETRAIA Number 11

Town VIAREGGIO Postal Code/Cedex 55049

Country IT

Phone1* + ***39*** ***3486001513*** Phone2 +

Fax + E-mail* ***s.petrucci@caen.it***

** Contact details can only be changed by the Proposal Coordinator via the "Step 4 – Manage Your Related Parties" screen.*

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A2.11 Participant #11

UCL

If your organisation has already registered for FP7, enter your Participant Identity Code ***999975620***

Legal Name ***UNIVERSITY COLLEGE LONDON***

Organisation short name ***UCL***

Administrative data (legal address)

Street name ***Gower Street*** Number ***1***

Town ***LONDON***

Postal Code / Cedex ***WC1E 6BT***

Country ***UK***

Internet homepage ***http://www.ucl.ac.uk***

Status of your organisation

Certain types of organisations benefit from special conditions under the FP7 participant rules. The Commission also collects data for statistical purposes.

The guidance notes will help you complete this section.

Please 'tick' the relevant box(es) if your organisation falls into one ore more of the following categories.

Non-profit organisation	(•) Yes	( ) No
Public body	(•) Yes	( ) No
Research organisation	(•) Yes	( ) No
Higher or secondary education establishment	(•) Yes	( ) No

Main area of activity (NACE code) 80.3

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1. Is your number of employees smaller than 250? (full time equivalent)	○ Yes	○ No
2. Is your annual turnover smaller than € 50 million?	○ Yes	○ No
3. Is your annual balance sheet total smaller than € 43 million?	○ Yes	○ No
4. Are you an autonomous legal entity?	○ Yes	○ No

You are NOT an SME if your answer to question 1 is "NO" and/or your answer to both questions 2 and 3 is "NO".

In all other cases, you might conform to the Commission's definition of an SME.

Please check the additional conditions given in the guidance notes to the forms.

Following this check, do you conform to the Commission's definition of an SME? ○ Yes ◉ No

Dependencies with (an)other participant(s)

Are there dependencies between your organisation and (an)other participant(s) in this proposal? ○ Yes ◉ No

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Development and Demonstration

Contact point - Person in charge for participant #11

For the co-ordinator (Participant #1) this person is the one who the Commission will contact in the first instance.

Family name* ***Konstantinidis*** First name(s)* ***Nikos***

Title Prof.

(•) Male ( ) Female

Position in the organisation Professor in particle physics

Department/Faculty/Institute/Laboratory name/... Department of Physics & Astronomy

Address ☒ Same as legal address

Street name Gower Street Number 1

Town LONDON Postal Code/Cedex WC1E 6BT

Country UK

Phone1* + ***44*** ***2076793411*** Phone2 +

Fax + E-mail* ***n.konstantinidis@ucl.ac.uk***

** Contact details can only be changed by the Proposal Coordinator via the "Step 4 – Manage Your Related Parties" screen.*

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A2.12 Participant #12

IST ID

If your organisation has already registered for FP7, enter your Participant Identity Code ***954983722***

Legal Name ***ASSOCIACAO DO INSTITUTO SUPERIOR TECNICO PARA A INVESTIGACAO E DESEN***

Organisation short name ***IST ID***

Administrative data (legal address)

Street name ***AVENIDA ROVISCO PAIS*** Number ***1***

Town ***LISBOA***

Postal Code / Cedex ***1049 001***

Country ***PT***

Internet homepage ***www.ist-id.pt***

Status of your organisation

Certain types of organisations benefit from special conditions under the FP7 participant rules. The Commission also collects data for statistical purposes.

The guidance notes will help you complete this section.

Please 'tick' the relevant box(es) if your organisation falls into one ore more of the following categories.

Non-profit organisation	(•) Yes	( ) No
Public body	( ) Yes	(•) No
Research organisation	(•) Yes	( ) No
Higher or secondary education establishment	( ) Yes	(•) No

Main area of activity (NACE code) 73.1

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1. Is your number of employees smaller than 250? (full time equivalent)	○ Yes	○ No
2. Is your annual turnover smaller than € 50 million?	○ Yes	○ No
3. Is your annual balance sheet total smaller than € 43 million?	○ Yes	○ No
4. Are you an autonomous legal entity?	○ Yes	○ No

You are NOT an SME if your answer to question 1 is "NO" and/or your answer to both questions 2 and 3 is "NO".

In all other cases, you might conform to the Commission's definition of an SME.

Please check the additional conditions given in the guidance notes to the forms.

Following this check, do you conform to the Commission's definition of an SME? ○ Yes ◉ No

Dependencies with (an)other participant(s)

Are there dependencies between your organisation and (an)other participant(s) in this proposal? ○ Yes ◉ No

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Contact point - Person in charge for participant #12

For the co-ordinator (Participant #1) this person is the one who the Commission will contact in the first instance.

Family name* ***Soares Gonçalves*** First name(s)* ***Bruno***

Title Dr.

(•) Male ( ) Female

Position in the organisation President of IPFN

Department/Faculty/Institute/Laboratory name/... Instituto de Plasmas e Fusão Nuclear (IPFN-IST)

Address ☒ Same as legal address

Street name AVENIDA ROVISCO PAIS Number 1

Town LISBOA Postal Code/Cedex 1049 001

Country PT

Phone1* + ***35*** ***1218417818*** Phone2 +

Fax + E-mail* ***bruno@ipfn.ist.utl.pt***

** Contact details can only be changed by the Proposal Coordinator via the "Step 4 – Manage Your Related Parties" screen.*

EUROPEAN COMMISSION

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A3.1.1 Budget #1

INFN

In FP7, there are different methods for calculating indirect costs. The various options are explained in the guidance notes. Please be aware that not all options are available to all types of organisations.

Method: Specific flat rate 60%

My legal entity is established in an ICPC and I shall use the lump sum funding method
(If yes, please fill below the lump sum row only. If no, please do not use the lump sum row)

○ Yes ◉ No

Type of Activity

	RTD up to 50 or 75% *	Demonstration up to 50%	Management up to 100%	Total
Personnel costs (in €)	183 018 €	116 466 €	127 558 €	427 042 €
Subcontracting (in €)	0 €	0 €	5 500 €	5 500 €
Other direct costs (in €)	153 000 €	0 €	10 000 €	163 000 €
Indirect costs (in €)	201 610 €	69 879 €	82 534 €	354 023 €
Lump sum, flat-rate or scale of unit (option only for ICPC) (in €)				
Total budget (in €)	537 628 €	186 345 €	225 592 €	949 565 €
Requested EC contribution (in €)	403 221 €	93 172 €	225 592 €	721 985 €
Total Receipts (in €)				0 €

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A3.1.2 Budget #2

CNRS

In FP7, there are different methods for calculating indirect costs. The various options are explained in the guidance notes. Please be aware that not all options are available to all types of organisations.

Method: Specific flat rate 60%

My legal entity is established in an ICPC and I shall use the lump sum funding method
(If yes, please fill below the lump sum row only. If no, please do not use the lump sum row)

○ Yes ◉ No

Type of Activity

	RTD up to 50 or 75% *	Demonstration up to 50%	Management up to 100%	Total
Personnel costs (in €)	127 224 €	0 €	13 392 €	140 616 €
Subcontracting (in €)	0 €	0 €	2 500 €	2 500 €
Other direct costs (in €)	258 000 €	0 €	10 000 €	268 000 €
Indirect costs (in €)	231 134 €	0 €	14 035 €	245 169 €
Lump sum, flat-rate or scale of unit (option only for ICPC) (in €)				
Total budget (in €)	616 358 €	0 €	39 927 €	656 285 €
Requested EC contribution (in €)	462 268 €	0 €	39 927 €	502 195 €
Total Receipts (in €)				0 €

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A3.1.3 Budget #3

Microtest

In FP7, there are different methods for calculating indirect costs. The various options are explained in the guidance notes. Please be aware that not all options are available to all types of organisations.

Method: Specific flat rate 60%

My legal entity is established in an ICPC and I shall use the lump sum funding method
(If yes, please fill below the lump sum row only. If no, please do not use the lump sum row)

○ Yes ◉ No

Type of Activity

	RTD up to 50 or 75% *	Demonstration up to 50%	Management up to 100%	Total
Personnel costs (in €)	173 760 €	0 €	57 920 €	231 680 €
Subcontracting (in €)	0 €		0 €	0 €
Other direct costs (in €)	29 000 €		10 000 €	39 000 €
Indirect costs (in €)	121 656 €	0 €	40 752 €	162 408 €
Lump sum, flat-rate or scale of unit (option only for ICPC) (in €)				
Total budget (in €)	324 416 €	0 €	108 672 €	433 088 €
Requested EC contribution (in €)	243 312 €	0 €	108 672 €	351 984 €
Total Receipts (in €)				0 €

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A3.1.4 Budget #4

AUTH

In FP7, there are different methods for calculating indirect costs. The various options are explained in the guidance notes. Please be aware that not all options are available to all types of organisations.

Method: Specific flat rate 60%

My legal entity is established in an ICPC and I shall use the lump sum funding method
(If yes, please fill below the lump sum row only. If no, please do not use the lump sum row)

○ Yes ◉ No

Type of Activity

	RTD up to 50 or 75% *	Demonstration up to 50%	Management up to 100%	Total
Personnel costs (in €)	42 855 €	42 855 €	8 571 €	94 281 €
Subcontracting (in €)	0 €	0 €	0 €	0 €
Other direct costs (in €)	48 000 €	0 €	10 000 €	58 000 €
Indirect costs (in €)	54 513 €	25 713 €	11 142 €	91 368 €
Lump sum, flat-rate or scale of unit (option only for ICPC) (in €)				
Total budget (in €)	145 368 €	68 568 €	29 713 €	243 649 €
Requested EC contribution (in €)	109 026 €	34 284 €	29 713 €	173 023 €
Total Receipts (in €)				0 €

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A3.1.5 Budget #5

UNIGE

In FP7, there are different methods for calculating indirect costs. The various options are explained in the guidance notes. Please be aware that not all options are available to all types of organisations.

Method: Specific flat rate 60%

My legal entity is established in an ICPC and I shall use the lump sum funding method
(If yes, please fill below the lump sum row only. If no, please do not use the lump sum row)

○ Yes ◉ No

Type of Activity

	RTD up to 50 or 75% *	Demonstration up to 50%	Management up to 100%	Total
Personnel costs (in €)	116 870 €	0 €	17 531 €	134 401 €
Subcontracting (in €)	0 €	0 €	0 €	0 €
Other direct costs (in €)	14 000 €	0 €	8 000 €	22 000 €
Indirect costs (in €)	78 522 €	0 €	15 318 €	93 840 €
Lump sum, flat-rate or scale of unit (option only for ICPC) (in €)				
Total budget (in €)	209 392 €	0 €	40 849 €	250 241 €
Requested EC contribution (in €)	157 044 €	0 €	40 849 €	197 893 €
Total Receipts (in €)				0 €

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A3.1.6 Budget #6

UNIFI

In FP7, there are different methods for calculating indirect costs. The various options are explained in the guidance notes. Please be aware that not all options are available to all types of organisations.

Method: Specific flat rate 60%

My legal entity is established in an ICPC and I shall use the lump sum funding method
(If yes, please fill below the lump sum row only. If no, please do not use the lump sum row)

○ Yes ◉ No

Type of Activity

	RTD up to 50 or 75% *	Demonstration up to 50%	Management up to 100%	Total
Personnel costs (in €)	0 €	167 656 €	8 824 €	176 480 €
Subcontracting (in €)	0 €	0 €	0 €	0 €
Other direct costs (in €)	0 €	8 000 €	8 000 €	16 000 €
Indirect costs (in €)	0 €	105 393 €	10 094 €	115 487 €
Lump sum, flat-rate or scale of unit (option only for ICPC) (in €)				
Total budget (in €)	0 €	281 049 €	26 918 €	307 967 €
Requested EC contribution (in €)	0 €	140 524 €	26 918 €	167 442 €
Total Receipts (in €)				0 €

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A3.1.7 Budget #7

PRIELE

In FP7, there are different methods for calculating indirect costs. The various options are explained in the guidance notes. Please be aware that not all options are available to all types of organisations.

Method: Specific flat rate 60%

My legal entity is established in an ICPC and I shall use the lump sum funding method
(If yes, please fill below the lump sum row only. If no, please do not use the lump sum row)

○ Yes ◉ No

Type of Activity

	RTD up to 50 or 75% *	Demonstration up to 50%	Management up to 100%	Total
Personnel costs (in €)	79 500 €	27 000 €	24 000 €	130 500 €
Subcontracting (in €)	0 €	0 €	0 €	0 €
Other direct costs (in €)	18 000 €	0 €	10 000 €	28 000 €
Indirect costs (in €)	58 500 €	16 200 €	20 400 €	95 100 €
Lump sum, flat-rate or scale of unit (option only for ICPC) (in €)				
Total budget (in €)	156 000 €	43 200 €	54 400 €	253 600 €
Requested EC contribution (in €)	117 000 €	21 600 €	54 400 €	193 000 €
Total Receipts (in €)				0 €

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A3.1.8 Budget #8

UHEI

In FP7, there are different methods for calculating indirect costs. The various options are explained in the guidance notes. Please be aware that not all options are available to all types of organisations.

Method: Actual indirect costs

My legal entity is established in an ICPC and I shall use the lump sum funding method
(If yes, please fill below the lump sum row only. If no, please do not use the lump sum row)

○ Yes ◉ No

Type of Activity

	RTD up to 50 or 75% *	Demonstration up to 50%	Management up to 100%	Total
Personnel costs (in €)	105 436 €	0 €	10 544 €	115 980 €
Subcontracting (in €)	0 €	0 €	0 €	0 €
Other direct costs (in €)	8 000 €	0 €	10 000 €	18 000 €
Indirect costs (in €)	106 491 €	0 €	8 962 €	115 453 €
Lump sum, flat-rate or scale of unit (option only for ICPC) (in €)				
Total budget (in €)	219 927 €	0 €	29 506 €	249 433 €
Requested EC contribution (in €)	164 945 €	0 €	29 506 €	194 451 €
Total Receipts (in €)				0 €

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A3.1.9 Budget #9

IMEC

In FP7, there are different methods for calculating indirect costs. The various options are explained in the guidance notes. Please be aware that not all options are available to all types of organisations.

Method: Actual indirect costs

My legal entity is established in an ICPC and I shall use the lump sum funding method
(If yes, please fill below the lump sum row only. If no, please do not use the lump sum row)

○ Yes ◉ No

Type of Activity

	RTD up to 50 or 75% *	Demonstration up to 50%	Management up to 100%	Total
Personnel costs (in €)	74 000 €	0 €	18 500 €	92 500 €
Subcontracting (in €)	0 €	0 €	0 €	0 €
Other direct costs (in €)	51 000 €	0 €	8 000 €	59 000 €
Indirect costs (in €)	62 900 €	0 €	15 725 €	78 625 €
Lump sum, flat-rate or scale of unit (option only for ICPC) (in €)				
Total budget (in €)	187 900 €	0 €	42 225 €	230 125 €
Requested EC contribution (in €)	140 925 €	0 €	42 225 €	183 150 €
Total Receipts (in €)				0 €

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A3.1.10 Budget #10

CAEN

In FP7, there are different methods for calculating indirect costs. The various options are explained in the guidance notes. Please be aware that not all options are available to all types of organisations.

Method: Specific flat rate 60%

My legal entity is established in an ICPC and I shall use the lump sum funding method
(If yes, please fill below the lump sum row only. If no, please do not use the lump sum row)

○ Yes ◉ No

Type of Activity

	RTD up to 50 or 75% *	Demonstration up to 50%	Management up to 100%	Total
Personnel costs (in €)	16 000 €	24 000 €	10 000 €	50 000 €
Subcontracting (in €)	0 €	0 €	0 €	0 €
Other direct costs (in €)	4 000 €	0 €	10 000 €	14 000 €
Indirect costs (in €)	12 000 €	14 400 €	12 000 €	38 400 €
Lump sum, flat-rate or scale of unit (option only for ICPC) (in €)				
Total budget (in €)	32 000 €	38 400 €	32 000 €	102 400 €
Requested EC contribution (in €)	24 000 €	19 200 €	32 000 €	75 200 €
Total Receipts (in €)				0 €

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A3.1.11 Budget #11

UCL

In FP7, there are different methods for calculating indirect costs. The various options are explained in the guidance notes. Please be aware that not all options are available to all types of organisations.

Method: Specific flat rate 60%

My legal entity is established in an ICPC and I shall use the lump sum funding method
(If yes, please fill below the lump sum row only. If no, please do not use the lump sum row)

○ Yes ◉ No

Type of Activity

	RTD up to 50 or 75% *	Demonstration up to 50%	Management up to 100%	Total
Personnel costs (in €)	0 €	175 100 €	7 725 €	182 825 €
Subcontracting (in €)	0 €	0 €	0 €	0 €
Other direct costs (in €)	0 €	4 000 €	8 000 €	12 000 €
Indirect costs (in €)	0 €	107 460 €	9 435 €	116 895 €
Lump sum, flat-rate or scale of unit (option only for ICPC) (in €)				
Total budget (in €)	0 €	286 560 €	25 160 €	311 720 €
Requested EC contribution (in €)	0 €	143 280 €	25 160 €	168 440 €
Total Receipts (in €)				0 €

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A3.1.12 Budget #12

IST ID

In FP7, there are different methods for calculating indirect costs. The various options are explained in the guidance notes. Please be aware that not all options are available to all types of organisations.

Method: Specific flat rate 60%

My legal entity is established in an ICPC and I shall use the lump sum funding method
(If yes, please fill below the lump sum row only. If no, please do not use the lump sum row)

○ Yes ◉ No

Type of Activity

	RTD up to 50 or 75% *	Demonstration up to 50%	Management up to 100%	Total
Personnel costs (in €)	65 070 €	72 300 €	5 423 €	142 793 €
Subcontracting (in €)	0 €	0 €	0 €	0 €
Other direct costs (in €)	4 000 €	0 €	8 000 €	12 000 €
Indirect costs (in €)	41 442 €	43 380 €	8 053 €	92 875 €
Lump sum, flat-rate or scale of unit (option only for ICPC) (in €)				
Total budget (in €)	110 512 €	115 680 €	21 476 €	247 668 €
Requested EC contribution (in €)	82 884 €	57 840 €	21 476 €	162 200 €
Total Receipts (in €)				0 €

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A3.2: Budget

Estimated budget in EUR (whole of the project)

Nr.	Organisation Short Name	Organisation country	RTD	Demonstration	Management	Total	Total receipts	Requested EU contributions
1	INFN	IT	537 628	186 345	225 592	949 565	0	721 985
2	CNRS	FR	616 358	0	39 927	656 285	0	502 195
3	Microtest	IT	324 416	0	108 672	433 088	0	351 984
4	AUTH	EL	145 368	68 568	29 713	243 649	0	173 023
5	UNIGE	CH	209 392	0	40 849	250 241	0	197 893
6	UNIFI	IT	0	281 049	26 918	307 967	0	167 442
7	PRIELE	EL	156 000	43 200	54 400	253 600	0	193 000
8	UHEI	DE	219 927	0	29 506	249 433	0	194 451
9	IMEC	BE	187 900	0	42 225	230 125	0	183 150
10	CAEN	IT	32 000	38 400	32 000	102 400	0	75 200

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11	UCL	UK	0	286 560	25 160	311 720	0	168 440
12	IST ID	PT	110 512	115 680	21 476	247 668	0	162 200
		Total	2 539 501	1 019 802	676 438	4 235 741	0	3 090 963

Small or medium-scale focused research project (STREP)

ICT Call 10
FP7-ICT-2013-10

advaNced associativE memory architectUres for massive data pROcessiNg paralleliSm

(NEURONS)

Type of project: **Small or medium scale focused research project (STREP)**
Date of preparation: 15/01/2013

Work programme objective addressed:
ICT-2013.3.4 Advanced computing, embedded and control systems
c) Exploiting synergies and strengths between computing segments

Name of the coordinating person: Dr. Paola Giannetti
e-mail: paola.giannetti@pi.infn.it
fax: +39 - 050 2214 317

PARTICIPANT NO. *	PARTICIPANT ORGANISATION NAME	PART. SHORT NAME	COUNTRY
1 (COORDINATOR)	ISTITUTO NAZIONALE DI FISICA NUCLEARE	INFN	I
2	CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE	CNRS	F
3	Microtest S.r.l.	Microtest	I
4	ARISTOTELIO PANEPISTIMIO THESSALONIKIS	AUTH	EL
5	UNIVERSITE DE GENEVE	UNIGE	CH
6	UNIVERSITA DEGLI STUDI DI FIRENZE	UNIFI	I
7	Prisma Electronics ABEE	PRIELE	EL
8	RUPRECHT-KARLS-UNIVERSITAET HEIDELBERG	UHEI	D
9	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	IMEC	B
10	COSTRUZIONI APPARECCHIATURE ELETTRONICHE NUCLEARI C.A.E.N. SPA	CAEN	I
11	UNIVERSITY COLLEGE LONDON	UCL	UK
12	ASSOCIACAO DO INSTITUTO SUPERIOR TECNICO PARA A INVESTIGACAO E DESENVOLVIMENTO	IST ID	P

Proposal abstract

The NEURONS project brings together embedded computing and high-performance computing teams jointly addressing challenges common in these two areas and magnified by the ubiquity of many-cores and heterogeneity across the whole computing spectrum by:

- Designing and fabricating innovative cost effective and low energy data-intensive parallel computing platforms to provide high levels of reliability, efficiency, availability, and scalability.
- Developing of innovative approaches and algorithms to parallel programming to address the processing of data on data-intensive systems.
- Demonstrating the system capability in applications that can exploit new computing paradigms and determining how they should evolve to support emerging data-intensive applications.

The main technological objectives of NEURONS are:

- Development of a novel multicore “Associative Memory for Multi-Applications” chip (AMMA-chip) in aggressive technology nodes (65 nm).
- Complement the AMMA functionality with Field Programmable Gate Arrays (FPGA) highly parallelized algorithms.
- Demonstration of the AMMA in case scenarios requiring massive data paralleled processing such as Computer Vision, Medical Imaging, High Energy Physics and Nuclear Fusion.
- Development of software algorithms for the foreseen demonstration scenarios requiring high parallelism data intensive processing.
- Design of novel computing architectures in the 3D domain.

The NEURONS project will pave the way towards new breakthroughs in the design, operations, and control of embedded computing systems requiring the control of mixed criticalities (i.e. Systems of Systems) opening multifaceted applications in industry (i.e. control of industrial processes), engineering (i.e. real-time context aware vehicles), healthcare (i.e. dynamic diagnostics), etc. The technology developed by the NEURONS project also steps ahead in materializing the ultimate computing paradigms such as cognitive computation and brain-like computing systems.

Contents

Section 1: Scientific and/or technical quality

1.1 Concept and objectives

1.1.1. NEURONS: overall project context

1.1.1.1. Computing: new paradigms

ICT (Information and Communication Technology) has transformed how we work and live—and has the potential to continue doing so. ICT helps bring distant people together, coordinate disaster response, enhance economic productivity, enable new medical diagnoses and treatments, add new efficiencies to our economy, improve weather prediction and climate modeling, broaden educational access, strengthen national defense, advance science, and produce and deliver content for education and entertainment. These transformations have been made possible by sustained improvements in computer performance (Fig. 1.1.1). We have been living in a world where information processing costs have been decreasing exponentially year after year. The performance achievements have driven an implicit, pervasive expectation that future ICT advances will occur as an inevitable continuation of the stunning advances ICT has experienced in the past half-century.

By the 2000s, however, it had become apparent that **processor performance growth faced two major constraints**:

- **First, the ability to increase clock speeds locked horns with power limits**. By 2004, the long-fruitful strategy of scaling down the size of CMOS circuits, reducing the supply voltage, and increasing the clock rate had become infeasible. Since a chip's power consumption is in proportion to the clock speed times the supply voltage squared, the inability to continue to lower the supply voltage halted developers' ability to increase the clock speed without increasing power dissipation. The ultimate consequence has been that growth in single-processor performance has stalled—or at best is being increased only marginally over time.

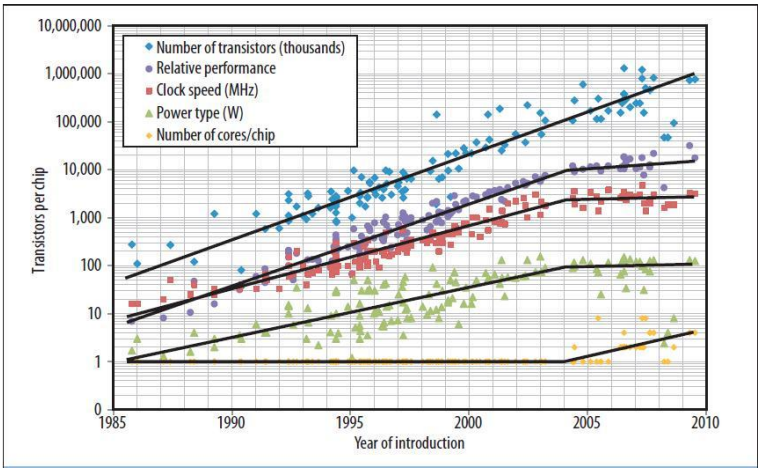

Fig. 1.1.1 Transistors, frequency, power, performance, and processor cores over time. The original Moore's law projection of increasing transistors per chip remains unabated even as performance has stalled (Source Ref: 1).

- **Second, efforts to improve individual processors' internal architecture have netted diminishing returns.** Many advances in the architecture of general-purpose sequential processors, such as deeper pipelines and speculative execution, have contributed to successful exploitation of increasing transistor densities. Today, however, there appears to be little opportunity to significantly increase performance by improving the internal structure of existing sequential processors.

Future growth in computing performance must come from parallelism[1]. The microprocessor industry has already begun to deliver parallel hardware in mainstream products with chip multiprocessors (CMPs), an approach that places new burdens on software developers to build applications that take advantage of multiple, distinct cores[2]. Although developers have found reasonable ways to use two or even four cores effectively by running independent tasks on each one, they have not, for the most part, parallelized individual tasks to make full use of the available computational capacity. Moreover, if industry continues to follow the same trends, they will soon be delivering chips with hundreds of cores. Harnessing these will require new hardware and software breakthroughs for parallel computing. **Nevertheless multicore systems and architectures and the vast increase in computing processing they promise must be ready to face the definite trends emerging from upcoming societal challenges and the evolution of computing systems[3].**

[1] David Geer, Industry Trends- Chip Makers Turn to Multicore Processors, IEEE Computer Society, 2005.
[2] P. Gepner et al., Multi-Core Processors: New Way to Achieve High System Performance, Proceedings of the International Symposium on Parallel Computing in Electrical Engineering (PARELEC'06), 2006, IEEE Computer Society
[3] S.H. Fuller, L.I. Millett, "The Future of Computing Performance: Game over or Next Level," Committee on Sustaining Growth in Computing Performance, National Research Council, National Academies Press, Sept, 2011.

From a technology point of view, the "Moore's law" of ever-increasing levels of integration fuelled computing performance over the past five decades. Each new technology generation doubled transistor density and increased frequency, while simultaneously reducing the power per transistor. Ever more demanding applications directly exploited these growing resources. However, a major paradigm shift is now taking place founded in recent trends and challenges[4]:

- **The *explosion of data*[5] (the "Data Deluge") and the increase in natural (unstructured) data from the real world (i.e. "cyber-physical systems") is increasing computation requirements, and demanding new processing and computing methods and storage faster than technology can keep up**. **Increasingly complex algorithms, faster devices and systems are required to efficiently handle this new era of data to tackle the increasing gap between the growth of data and processing power**. **Over 95% of the digital universe is "unstructured data"** – meaning its content can't be truly represented by its location in a computer record, such as name, address, or date of last transaction. Digital images, voice packets, and the musical notes in an MP3 file would be considered unstructured data. In organizations, unstructured data accounts for more than 80% of all information.
- Moore's law", while keeping pace in terms of transistor density, is now enabling only minor frequency increases and minor decreases in power dissipation per transistor. To keep increasing raw performance, the current approach is to add more processing units (multi-core processing). Unfortunately, this is far from transparent to most applications: **existing software and hardware now has to be re-engineered to execute efficiently on parallel architectures**. **The *complexity* of this task is one of today's main challenges**.
- **Another important limitation is *power efficiency***: even if more devices can be packed on a chip, the power used by each device is no longer dropping accordingly (end of Dennard scaling[6]). Since we are already at the power limit, **it will no longer be possible to use all devices on a chip simultaneously**. The resulting need to turn off functionality to meet power constraints results in "Dark Silicon".
- As devices become smaller with each generation, the variability between devices (in terms of performance and power) and their reliability decreases. To continue to leverage ever-smaller devices, **we must learn how to build reliable systems from unreliable, and highly variable, components**.
- **While connectivity during the last decade was mainly limited to wired computers and servers, we are now witnessing an *explosion in connectivity***. Critically, this connectivity now comprises a large variety of devices, ranging from warehouse-sized data centers for cloud and high performance computing, to mobile devices (phones, cars, planes, etc.), and all the way down to embedded sensors in the physical world and in the human body.
- **The computing domain is facing an increased *demand for dependability* and reliability across all fields**. Many emerging applications require high levels of safety and security (healthcare, automotive, etc.) and new technologies are introducing new challenges in reliability (ubiquitous connectivity, unreliable devices, etc).

1.1.1.2. The NEURONS project context: innovative ICT for the Big Data Challenge

In the coming sections more details of the general and scientific objectives of the project NEURONS will be described. Nevertheless and leveraging in the introductory sections before it will be useful to offer an preliminary section like this one framing the project NEURONS with respect to the challenges that computation will face in the coming decades as described before. Among the different trends and challenges faced by the ICT technologies summarized above, the NEURONS project focuses specially in developing innovative parallel hardware and novel software algorithms and solutions that will allow to use the advantages of specially considering one of the major challenges that computing power needs to face: Big Data processing. The NEURONS project will address and benefit from challenges that are common in embedded computing and high-performance computing and are magnified by the ubiquity of many-cores and heterogeneity across the whole computing spectrum with direct applicability to massive parallel data processing.

The NEURONS's parallel processing architecture stems from ones currently used in High Energy Physics (HEP) where complex images need to be reconstructed in few tens of microseconds and therefore extremely suitable to tackle the Big Data challenge. The key role in the novel technology that NEURONS will develop is played by a custom multicore Associative Memories (AM) that will intensively be used to filter out the relevant information of the data to be further processed by Field Programmable Gate Arrays (FPGAs) executing higher level algorithms. The AM implements the maximum parallelism and offers the best timing performances, since it solves its task in the time data are loaded on it. Additionally the NEURONS architecture benefits from the FPGA computing power to eliminate the main drawbacks of AMs. In fact the AM does not scale to large image sizes having high resolution, so the AM performs a first low resolution filtering

[4] R. Cavin, J. A. Hutchby, V. Zhirnov, J. E. Brewer, and G. Bourianoff, "Emerging Research Architectures", *Computer* vol. 41 (2008) 33-37.

[5] Data, data everywhere, *The Economist*. 25 February 2010

[6] R. Dennard, et al., "Design of ion-implanted MOSFETs with very small physical dimensions," IEEE Journal of Solid State Circuits, vol. SC-9, no. 5, pp. 256-268, Oct. 1974

function. The FPGA complements the AM task with its flexibility and configurability, adapting its logic to perform any necessary "refining processing" of the low resolution AM result. In addition the NEURONS's AM has a specific architecture that helps to identify not only perfect features, but also partial, or noisy versions of them. The figure 1.1.2 below shows the structure of one pattern, that is one location of the NEURONS AM.

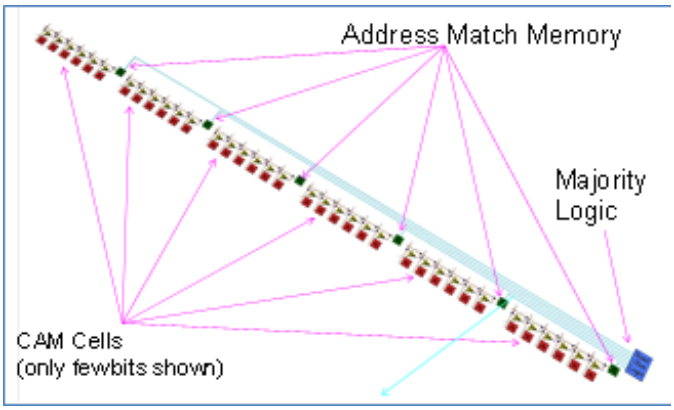

Fig. 1.1.2 Structure of one pattern AM for the NEURONS project.

Here is described the **key innovative conceptual and design difference between** the NEURONS project AM and commercially available AM[7]. In NEURONS'AM each pattern is stored in a single memory location like in the commercial AM, but it consists of N independent words of M bits each. Each word refers to a particular item to be identified in a flux of data that is private of the words that occupy that position in the pattern. In fact data are sent on N parallel buses, one for each word of the pattern. Each word is provided with reserved hardware comparators and a match flip-flop. All words in the AM can make independent and simultaneous comparisons with the data serially presented to its own bus. Any time a match is found, the match flip-flop is set. A pattern matches when a majority of its flip-flops are set. This is very promising for unstructured data processing which is, as mentioned before, perhaps one of the most daunting open issues to benefit from the Big Data challenge (see also further sections). In NEURONS the embedded system controls, configures and handles the AM providing the flexible computing power to process the shapes selected by the AM. The goals of this elementary unit are (a) maximum parallelism exploitation, (b) low power consumption, (c) execution times at least 1000 time shorter than the best commercial Control Processing Units (CPUs) performing the same task, distributed debugging and monitoring tools suited for a pipelined, highly parallelized structure, high degree of configurability to face with the best efficiency different applications.

In this context the key areas of focus of the project NEURONS are encompassing the needs required for present and future applications related to data intensive processing:

- Design and fabrication of innovative data-intensive parallel computing platforms to provide high levels of reliability, efficiency, availability, and scalability.
- Development of innovative approaches to parallel programming to address the parallel processing of data on data-intensive systems.
- Development of novel programming abstractions (i.e. algorithms) which allow a natural expression of parallel processing of data.
- Demonstrating applications that can exploit this computing paradigm and determining how it should evolve to support emerging data-intensive applications.

A more detailed description of the objectives as well as the innovative aspects of the NEURONS project is offered in subsequent section of the proposal. Nevertheless we judge necessary to emphasize in the coming sections the challenges that Big Data entail for the present and future developments of ICT Technologies and the huge benefits that innovative hardware and software computing paradigms will bring such as the ones the NEURONS project proposes[8] towards addressing and benefiting from the potential offered by extracting valuable information out of the so-called Big Data; that will pave the way towards European leadership in the newly emerging area of Big Data computing which will affect in an unprecedented manner the realization of science and businesses.

[7] Many of them classified as Content Addressable Memories (CAM).
[8] I. Gorton at al., Data Intensive Computing in the 21st Century, IEEE Computer, Vol. 41, No. 4, 2008, pp. 30-32V. Cerf, An Information Avalanche, IEEE Computer, vol. 40, no. 1 (2007), pp. 104-105.

1.1.1.3. Big-Data Technology Challenges: Collect, Store and Analyze

Advances in digital sensors, communications, computation, and storage have created huge collections of data, capturing information of value to business, science, government, and society. A pioneering study published in 2011 estimated the world's technological capacity to store, communicate, and compute information tracking 60 analog and digital technologies during the period from 1986 to 2007. It concluded that in 2007, humankind was able to store 2.9×10^{20} optimally compressed bytes, communicate almost 2×10^{21} bytes, and carry out 6.4×10^{18} instructions per second on general-purpose computers[9] (fig.1.1.3). General-purpose computing capacity grew at an annual rate of 58%. The world's capacity for bidirectional telecommunication grew at 28% per year, closely followed by the increase in globally stored information (23%). Humankind's capacity for unidirectional information diffusion through broadcasting channels has experienced comparatively modest annual growth (6%). Telecommunication has been dominated by digital technologies since 1990 (99.9% in digital format in 2007), and the majority of our technological memory has been in digital format since the early 2000s (94% digital in 2007).

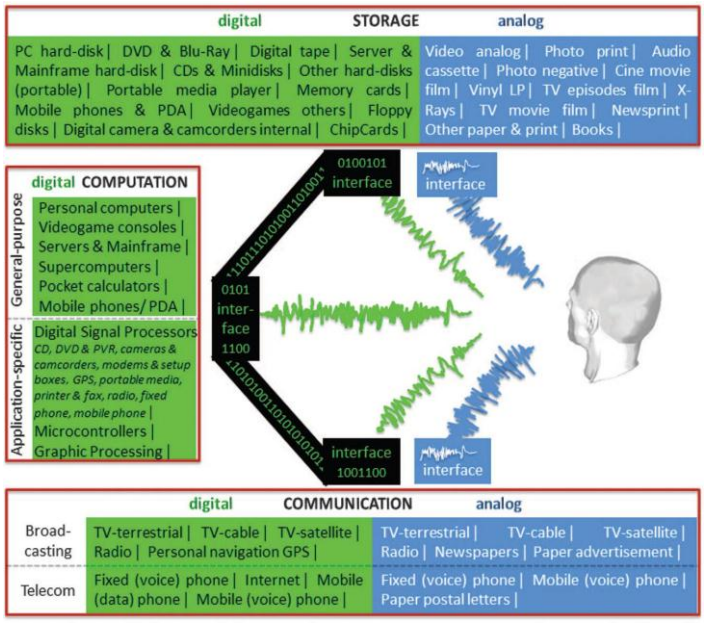

Fig. 1.1.3 The three basic information operations and their most prominent technologies (source: Ref. 9).

Data is rapidly increasing in quantity and becoming more diverse. In such a context there are growing demands from many different fields to analyze this data and utilize it to generate value (i.e. education, research, marketing, modeling of complex systems, etc). **Most of the data that has been subjected to analysis in the past has been of the structured type** that either has a defined format or consist of numerical values such as sales or inventory levels which are easy to process computationally. **However structured data makes only 20% of the total data held by corporations with text, images, voice and other unstructured data produced by people accounting for the reminder**. Whereas most previous data analysis hardware and software were designed to handle structured data, recent years have seen a growing need for the handling of text, images, video and other unstructured data created by people. **The problems with unstructured data are that its size and quantity have made its processing slow and that it is difficult to analyze because, unlike structured data, it could not be processed mechanically in its original format.**

It is therefore crucial to develop and implement novel hardware and software ICT paradigms and infrastructure technologies, such as storage systems, technologies for massive data processing, and media processing technologies for searching text, voice, image, and other media data[10].

Just as search engines have transformed how we access information, other forms of *big data computing* can and will transform the activities of companies, scientific researchers, medical practitioners, and defense and intelligence operations. Some examples illustrate:

- Some estimation indicates that **new data stored by enterprises exceeded 7 exabytes (exa = 10^{18}) of data globally in 2010 and that new data stored by consumers around the world that year exceeded an additional 6 exabytes**[11]. To put these very large numbers in context, the data that companies and individuals are producing and storing is equivalent to filling more than 60,000 US Libraries of Congress.
- Many scientific disciplines have become data-driven. For example, a modern telescope is really just a very large digital camera. The proposed **Large Synoptic Survey Telescope (LSST)** will scan the sky from a mountaintop in Chile, recording **30 trillion bytes of image data every day**. Astronomers will apply massive computing power to this data to probe the origins of our universe.

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[9] Martin Hilbert and Priscila López, *The World's Technological Capacity to Store, Communicate, and Compute Information*, Science 332, 60 (2011).

[10] AK. Asanovic et al., A view of the parallel computing landscape, Commun. ACM, Vol. 52, No. 10. (October 2009), pp. 56-67

[11] McKinsey Global Institute Report, Big data: The next frontier for innovation, competition, and productivity, 2011.

- **The Large Hadron Collider (LHC) at CERN**, a particle accelerator that will revolutionize our understanding of the workings of the Universe, will generate **60 terabytes of data per day** – 15 petabytes (15 million gigabytes) annually. Similar *eScience* projects are proposed or underway in a wide variety of other disciplines, from biology to environmental science to oceanography. These projects generate such enormous data sets that automated analysis is required. Additionally, it becomes impractical to replicate copies at the sites of individual research groups, so investigators pool their resources to construct a large data center that can run the analysis programs for all of the affiliated scientists.
- **Modern medicine** collects huge amounts of information about patients through imaging technology (**CAT scans, MRI**), genetic analysis (**DNA microarrays**), and other forms of diagnostic equipment. By applying ***data mining*** to data sets for large numbers of patients, medical researchers are gaining fundamental insights into the genetic and environmental causes of diseases, and creating more effective means of diagnosis. **Some estimations point that the global size of "Big Data" in Healthcare stands at roughly 150 Exabytes in 2011, increasing at a rate between 1.2 and 2.4 Exabytes per year**[12].
- **Understanding the environment** requires collecting and analyzing data from thousands of sensors monitoring air and water quality and meteorological conditions, another example of eScience. These measurements can then be used to **guide simulations of climate and groundwater models to create reliable methods to predict the effects of long-term trends, such as increased CO_2 emissions, the use of chemical fertilizers, etc**.
- **Intelligence agencies** are being overwhelmed by the vast amounts of data being collected through satellite imagery, signal intercepts, and even from publicly available sources such as the Internet and news media. Finding and evaluating possible threats from this data requires "connecting the dots" between multiple sources, e.g., to automatically match the voice in an intercepted cell phone call with one in a video posted on a terrorist website.
- The collection of **all documents on the World Wide Web** (**several hundred trillion bytes of text**) is proving to be a corpus that can be mined and processed in many different ways. For example, language translation programs can be guided by statistical language models generated by analyzing billions of documents in the source and target languages, as well as multilingual documents, such as the minutes of the United Nations. Specialized web crawlers scan for documents at different reading levels to aid English-language education for first graders to adults.
- "Big data" has increased the demand of information management specialists so that **companies such as Software AG, Oracle Corporation, IBM, Microsoft, SAP, and HP have spent more than $15 billion on technologies related to data management and analytics**. Big Data industry on its own is worth more than $100 billion and growing at almost 10% a year which is roughly twice as fast as the software business as a whole[13] .

These are but a small sample of the ways that all facets of commerce, science, society, and national security are being generating huge amounts of data and the necessity and opportunity that will entail to extract new forms of understanding from this data (Fig 1.1.4). The rising importance of big-data computing stems from advances in many different technologies:

Fig. 1.1.4 Explosion of Data: some examples (Units equivalence P(Peta)= 10^{15} ,T(Tera)= 10^{12}, G (Giga)= 10^{9}).

- **Sensors:** Digital data are being generated by many different sources, including digital imagers (telescopes, video cameras, MRI machines), chemical and biological sensors (microarrays, environmental monitors), and even the millions of individuals and organizations generating web pages.
- **Computer networks:** Data from the many different sources can be collected into massive data sets via localized sensor networks, as well as the Internet.
- **Data storage:** Advances in magnetic disk technology have dramatically decreased the cost of storing data. For example, a one-terabyte disk drive, holding one trillion bytes of data, costs around 100 Euros. As a reference, it is estimated that if all of the text in all of the books in the Library of Congress could be converted to digital form, it would add up to only around 20 terabytes.
- **Cluster computer systems:** A new form of computer systems, consisting of thousands of "nodes," each having several processors and disks, connected by high-speed local-area networks, has become the chosen hardware

[12] How big is 'big data' in healthcare?, available at: http://blogs.sas.com/content/hls/2011/10/21/how-big-is-big-data-in-healthcare/ SAS Health and Life Sciences blog.

[13] Data, data everywhere, The Economist. 25 February 2010

configuration for data-intensive computing systems. These clusters provide both the storage capacity for large data sets, and the computing power to organize the data, to analyze it, and to respond to queries about the data from remote users.

- **Cloud computing facilities:** The rise of large data centers and cluster computers has created a new business model, where businesses and individuals can *rent* storage and computing capacity, rather than making the large capital investments needed to construct and provision large-scale computer installations.
- **Data processing devices, architectures and analysis algorithms: The enormous volumes of data require automated or semi-automated analysis – techniques to detect patterns, identify anomalies, and extract knowledge. The "trick" is in developing new forms of computation, combining hardware performance with statistical analysis, optimization, and artificial intelligence, so to be able to construct statistical models from large collections of data and to infer how the system should respond to new data.**

1.1.1.4. Data Processing: Technology and Application Challenges

Recent years have seen a growing demand from a range of sectors such as healthcare, finance, corporate information, government institutions, security, etc for analysis and repurposing of unstructured data that in the past was limited to collection, storage and viewing; repurposing means using data in other ways to generate added value such as academic and industrial research, marketing, etc.

The problem with unstructured data is that it has not been able to be put to use because the difficulty of subjecting it to computational processes. Compared to structured data, the typical example of which is a database, the problems with repurposing unstructured data are that factors such as its size and quantity make processing slow, and that it is difficult to use for statistical processing or other analysis because its format is not machine-understandable like numerical data.

For example, hardware and software technologies and architectures for massive data processing are required for tasks such as searching for similar images in large amounts of image data, using multiple computers to execute similarity calculations in parallel, or techniques for optimally positioning data on an HDD (hard disk drive). Also, tasks such as similar case searches of the scanned images of for example medical records on a paper medium and statistical and other analytical processing require technologies able to extract information in a form that can be processed on a computer and convert it to structured data. Examples of this information include named entities and their attributes, or numerical data and its meaning, taken from test results, for example, and obtained by searching scanned images.

Much of the technology required for big-data computing is developing at a satisfactory rate due to market forces and technological evolution. For example, disk drive capacity is increasing and prices are dropping due to the ongoing progress of magnetic storage technology and the large economies of scale provided by both personal computers and large data centers. Other aspects require more focused attention, including:

- **High-speed networking:** Although one terabyte can be stored on disk for approximately 100 Euros, transferring that much data requires an hour or more within a cluster and roughly a day over a typical “high-speed” Internet connection. These bandwidth limitations increase the challenge of making efficient use of the computing and storage resources in a cluster. They also limit the ability to link geographically dispersed clusters and to transfer data between a cluster and an end user.
- **Cluster computer programming:** Programming large-scale, distributed computer systems is a longstanding challenge that becomes essential to process very large data sets in reasonable amounts of time. The software must distribute the data and computation across the nodes in a cluster, and detect and remediate the inevitable hardware and software errors that occur in systems of this scale. Major innovations have been made in methods to organize and program such systems, including the MapReduce programming framework introduced by Google. Much more powerful and general techniques must be developed to fully realize the power of big-data computing across multiple domains.
- **Extending the reach of cloud computing:** Despite recent commercial developments (i.e. Amazon AWS), technological limitations, especially communication bandwidth, make unsuitable this solution for tasks that require extensive computation over large amounts of data. In addition, the bandwidth limitations of getting data in and out of a cloud facility incur considerable time and expense.
- **Machine learning and other data processing and analysis techniques:** As a scientific discipline, machine **learning is still in its early stages of development. Many algorithms do not scale beyond data sets of a few million elements or cannot tolerate the statistical noise and gaps found in real-world data. Further research is required to develop algorithms that apply in real-world situations and on data sets of trillions of elements. The automated or semi-automated analysis of enormous volumes of data lies at the heart of big-data computing for all application domains. Consumer-image databases are growing so dramatically they require automated**

search instead of manual labeling. Low error rates require processing very high dimensional feature spaces. Current image classifiers are too slow to deliver adequate response times.

- **Widespread deployment:** Until recently, the main innovators in this domain have been companies with Internet-enabled businesses, such as search engines, online retailers, and social networking sites. Only now are technologists in other organizations (including universities) becoming familiar with the capabilities and tools. Although many organizations are collecting large amounts of data, only a handful are making full use of the insights that this data can provide. We expect "big-data science" – often referred to as eScience – to be pervasive, with far broader reach and impact even than previous-generation computational, science.
- **Security and privacy:** Data sets consisting of so much, possibly sensitive data, and the tools to extract and make use of this information give rise to many possibilities for unauthorized access and use. Much of our preservation of privacy in society relies on current inefficiencies. For example, people are monitored by video cameras in many locations – ATMs, convenience stores, airport security lines, and urban intersections. Once these sources are networked together, and sophisticated computing technology makes it possible to correlate and analyze these data streams, the prospect for abuse becomes significant. In addition, cloud facilities become a cost-effective platform for malicious agents, e.g., to launch a botnet or to apply massive parallelism to break a cryptosystem. Along with developing this technology to enable useful capabilities, we must create safeguards to prevent abuse.

Big-data computing is perhaps the biggest innovation in computing in the last decade. We have only begun to see its potential to collect, organize, and process data in all walks of life. Investments in big-data computing will have extraordinary near-term and long-term benefits. The technology has already been proven in some industry sectors; the challenge is to extend the technology and to apply it more widely.

1.1.2. NEURONS project objectives: parallel computing architectures for the Big Data challenge

As stated before the **key areas of focus** of the project NEURONS are encompassing the needs required for present and future applications related to data intensive processing:

- Design and fabrication of innovative data-intensive parallel computing platforms to provide high levels of reliability, efficiency, availability, and scalability.
- Development of innovative approaches to parallel programming to address the parallel processing of data on data-intensive systems.
- Development of novel programming abstractions (i.e. algorithms) which allow a natural expression of parallel processing of data.
- Demonstrating applications that can exploit this computing paradigm and determining how it should evolve to support emerging data-intensive applications.

According to the above defined focus areas the **general objectives** of the NEURONS project are:

- **Development** of a novel multicore “Associative Memory for Multi-Applications” chip (AMMA-chip).
- **Complement** the AMMA functionality with FPGA highly parallelized algorithms.
- **Demonstration** of the AMMA in case scenarios requiring massive data paralleled processing.
- **Development of** software algorithms for the foreseen demonstration scenarios requiring high parallelism data intensive processing.

The above general objectives of the NEURONS project will be possible by the consecution of the following **scientific and technological objectives**:

1.1.2.1. Development of novel “Associative Memory for Multi-Applications” (AMMA) and AMMA Board

The **main objective** is to develop a novel “Associative Memory for Multi-Applications” (AMMA) chip. This objective will be achieved by fabricating ASIC prototypes in 65 nm VLSI-technologies (Very Large Scale Integrated Technologies). The AMMA will count with serial link buses for all data paths. The newly developed chip will allow the storage in the memory bank of 32 Kpatterns per die and multi-packaged chips to reach 64 Kpatterns capability per chip. The NEURONS project will develop an AMMA-Board containing the AMMA chips and an AMMA-Control-Board board to control and complete the functions of the custom-made mezzanine. The custom-made mezzanine, the AMMA-Board, is also called, for historical reasons, Local Associative Memory Board (LAMB) and contains 32 AMMA chips, 16 on the top and 16 on the bottom face.

The figure 1.1.5 shows on the top the state of the art of the online AM system[14] developed for the CDF experiment at Fermilab, a large 9U VME board provided of FPGAs on the motherboard and assembled with 4 LAMB mezzanines. On the bottom the LAMB is shown. One of the NEURONS's key goals is the miniaturization of the system in new modern standards with the objective to make it suitable for an open range of applications in which massive and parallel data processing is key.

The new Control Board will have the following characteristics:

- powerful FPGA (Field Programmable Gate Arrays) with embedded CPU and large on-board memory,
- communication via Ethernet & PCI Express with the external world,
- handling (distribution and collection) of all AMMA-Board serial links,
- configuration and control of the AMMA bank on the AMMA-Board,
- provision of extra functionality to complete the AMMA functions in real time.

While the AMMA chip needs challenging developments, one of the advantages that the newly developed technology in NEURONS will have is that boards already available on the market are powerful enough to cover the above listed requests. Availability and incorporation of commercial boards will allow early to the consortium partners involved in the demonstration WP4 to acquire experience (software development, communication with the external word, large file management…) in advance with respect the availability of the AMMA chip to be develop. In this sense the figure 1.1.6 shows a preliminary and already available to the consortium prototype sketch of the new NEURONS computing unit, based on a Xilinx Virtex™ 6 PCI Express Gen 2 / SFP+ / USB 3.0 Development Board. The new LAMB will be connected to the large connector on the top of the board.

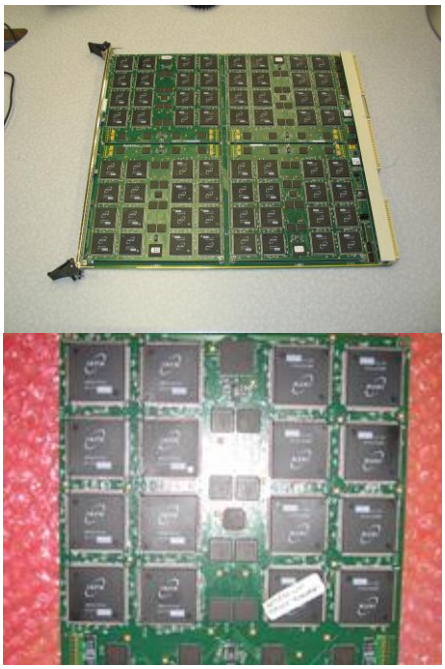


Fig. 1.1.5. Up - state of the art of the online AM system developed for the CDF experiment at Fermilab; down – LAMB. The NEURONS project will go beyond this state of the art as explained in detailed in the text.

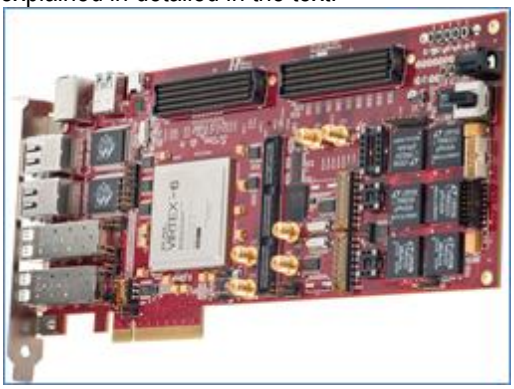


Fig. 1.1.6 Preliminary and already available to the consortium prototype sketch of the new NEURONS computing unit, based on a Xilinx Virtex™ 6 PCI Express Gen 2 / SFP+ / USB 3.0 Development Board. The NEURONS project will go beyond this state of the art as described in the text

1.1.2.2. Development of 3D integration architectures

The NEURONS project (with its WP5) will pursue the development of further integration concepts to increase the power and degree of parallelism of the system, without increasing the size and consumption, thanks to a miniaturization process that will increase the logic density. One important goal will be the increase of the FPGA parallelism. We will design a system where an FPGA will be associated to each AM chip. The first AMMA prototype, in fact, can suffer for bottlenecks in the FPGA for certain applications, in particular when the AM chip low resolution causes an high rate of fakes and an overload for the high resolution work of the FPGA. The best solution that we want to investigate today is the multi-packaging of the FPGA and the AMMA-chip in the same package. The figure 1.1.7 shows on the left the silicon interposer approach for Xilinx Virtex-7 FPGA as example.

The most important goal of WP5, however, will be the integration of larger banks inside the AMMA chip. This goal will be pursued working in different directions. First of all we will optimize the 2D design to occupy the maximum die size allowed by the package, keeping the power consumption at the minimum level to be able to package two AMMA chips one over the other (2.5 D). In this case communication between different chips is limited to contacts between peripheral pads.

[14] The AM++ board for the silicon vertex tracker upgrade at CDF" Annovi, A. et al., IEEE Transactions on Nuclear Science, Volume: 53, 2006 , Page(s): 1726

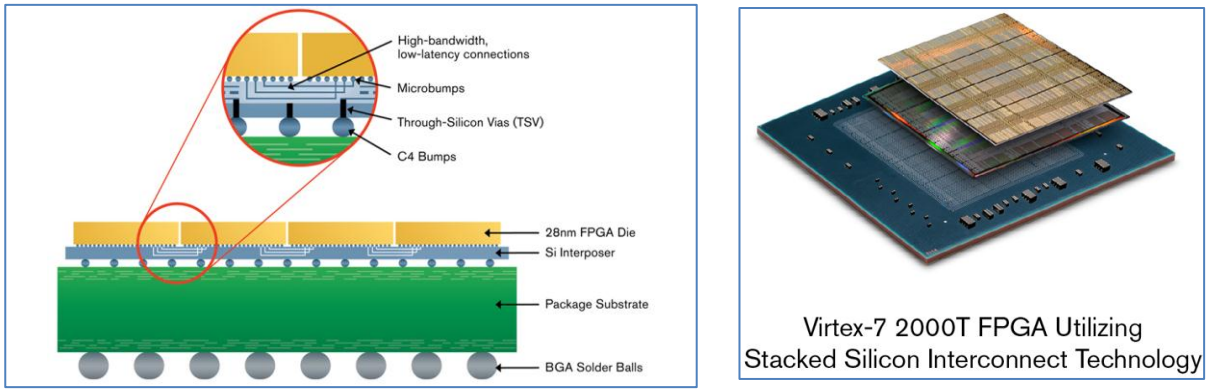


Fig. 1.1.7 Left and right - example of silicon interposer approach for Xilinx Virtex-7 FPGA; This approach will constitute the basis for the innovations that the NEURONS project will develop as described in the text.

Nevertheless although the NEURONS project will push 2D architectures to the maximum it will be extremely interesting to investigate and understand the potentiality for 3D. Future associative memory designs will require many more stored patterns per unit area at less power per pattern and at greater speed. This is by no means a simple task, but the three elements – pattern density, power and speed – are related to one another through geometry. Obviously, with smaller feature sizes, more associative memory cells can be made in the same area. Furthermore, both power and speed are directly connected to load capacitance which is itself related to feature size. Therefore, the logical approach to the requirements of future associative memory designs is to build them in smaller and smaller feature sizes. However, this approach eventually fails both economically and technically. Economically, each new process node is averaging a factor of 2.5 times in production cost over the preceding technology node. Technically, the scaling of VLSI circuits reduces gate delay, but increases interconnect delay. Then, the advantages of a 3D AMMA are increased pattern density at an increased speed with decreased power density. The improved pattern density comes from a reduction in the area required to build the AMMA through transistor reduction and vertical integration. The decreased power density comes from a reduction of transistors and a minimization of parasitic capacitance. The increased speed comes from architectural modifications.

The NEURON project will dedicate efforts for a highly innovative 3D design to solve the pattern density and performance limitation in 2D design by vertical integration. The 3D structure will be inherently open and flexible, and would facilitate design reuse, making possible the design of more general-purpose fast pattern recognition devices with potential applications far beyond the ones originally conceived by the 2D AMMA-chip. Associative Memory chips can be said to belong to the same class of integrated circuits as SRAM and DRAM chips. They are large arrays of smaller cells that are reproduced many times and are ordered in a fashion that is periodic in two dimensions. Moreover, these smaller cells are mainly connected to peripheral cells and do not interact much with one another. Consequently, this makes any 3D memory or associative memory design different than, for example, 3D microprocessor design. Intuitively, an appropriate rendering of the repeated cell in 3 dimensions can be expected to yield significant benefits to the overall design and therefore will deserve considerable attention in the NEURONS project. The NEURONS project will analyse the feasibility in 65 nm of use of potential suggested routes for more conservative technology nodes (130 nm) which propose Vertically Integrated Pattern Recognition Associative Memory (VIPRAM)

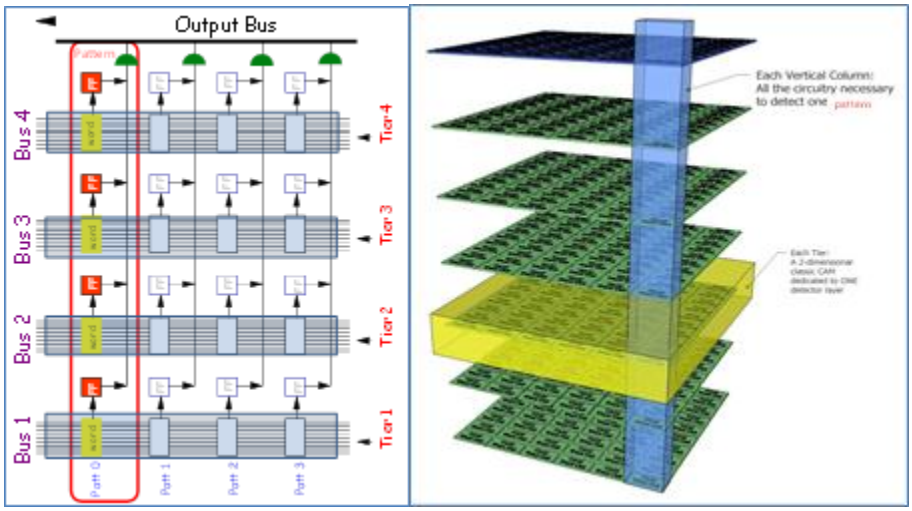


Fig. 1.1.8 VIPRAM 3D concept. The NEURONS project will explore and develop designs on similar architectures in a much more advanced technology nodes (65 nm).

architectures[15]. Nevertheless the challenges associated to the 65 nm node probably will represent one of the more ambitious goals the NEURON project will face.
The VIPRAM main idea is shown in the figure 1.1.8 below. The AMMA patterns, as described in figure 1.1.2 of section 1.1.2.2, would become vertical. Each word connected to the same input bus belongs to the same tier and each tier will receive and distribute a single bus. The last tier is logically different and contains the majority logic of each pattern and the readout logic.
In conclusion the WP5 investigation will provide necessary data (dimension and consumption of the final FPGA-AMMA-chip couple) to design the mechanics and power distribution for a system of AMMA-Elementary Units (AMMA-EUs). They could be joined by an Ethernet switch or, if small enough, inserted on a PCI express bus, or integrated in the very powerful ATCA technology.

1.1.2.3 AMMA chip demonstration for massive parallel data processing applications

The performance and capabilities of the newly developed AMMA chip will be demonstrated and evaluated in four application fields requiring massive data processing parallelism and that will constitute a solid test-bench for the evaluation of the AMMA-chip and will open up application paths towards commercially interesting and in many cases pioneering business markets. The NEURONS project foresees the following demonstration scenarios:

- **Computer Vision and Medical Imaging Applications**

The goal of this demonstration is to use the AMMA-chip for simulation of the initial stages of the brain visual processing, such as the identification of object contours. Convincing models about the brain functioning at this level are very similar to the internal AMMA architecture[16]. Therefore, the AMMA chip could implement fast pattern selection/filtering of the type studied in these models of human vision or other brain functions. In particular, strong data reduction of external stimuli before higher level processing is essential in (high rate) background filtering and during extraction of salient information from complex colored and highly textured natural images with multiple luminosity levels varying over time due changes in illumination or motion of objects. Simulations of such visual analysis are onerous to implement, if at all, in usual supercomputers. Once assembled and suitably adapted and interfaced for the specific purpose, the prototype would be used to execute detailed and thorough simulations. Two computing phases will be necessary, first the training then the image processing.
During the training phase, different steps will be taken into account:

- The embedded system will receive the image bit-streams (could come from a video-camera) through Ethernet or PCI Express,
- The FPGA will partition the input into small patterns (3x3 contiguous bit patches for static images, 3x3x3 for movies) and then will compute the frequencies of all possible patterns (512 for static images and 128 millions for movies) in a large set of natural images,
- Then the FPGA will select the relevant patterns to be downloaded in the LAMB.

During the image processing phase different steps will be taken into account:

- A new set of images will be partitioned into 3x3 or 3x3x3 bit patterns by the FPGA and sent to the LAMB that will send back only the matching patterns.
- The “filtered patterns” will be reorganized by the FPGA to produce the “filtered image”, further processed by finding shapes in sets of contiguous bits over threshold and producing templates of the shapes for higher level image processing.
- During the image processing phase, the FPGA will continuously monitor the frequencies of salient patterns and, if the patterns downloaded in the LAMB will result outside the correct frequency range (i.e. predictive of their saliency), image processing will stop and a new set of updated salient patterns will be substituted in the filtering engine.

This projected route opens up the capabilities of the AMMA-chip in the field of Medical Imaging as well. The AMMA-chip filtering function, combined with the computing power of parallel arrays of FPGAs. applied to image reconstruction could reduce the execution time of image processing. One potential application area is in the realm of automated medical diagnoses by imaging. The target focuses on the possibility of analysing time-changing images. The FPGA proposed algorithms to be developed in NEURONS for shape finding in the filtered image is highly parallelized and will achieve a processing time linear with respect to the number of pixels to be processed. For this reason, it is intrinsically stable with respect to the image occupancy and size. It is a fast general-purpose algorithm for high-throughput clustering of data "with a two dimensional organization". The two-dimensional problem is well processed by FPGAs since their available logic is naturally organized into a 2-dimensional array. The algorithm proposed is designed to be implemented with FPGAs but it

[15] Developement of 3D Vertically Integrated Pattern Recognition Associative Memory (VIPRAM). G. Deputch, et al., Apr, 2011 - FERMILAB-TM-2493-CMS-E-PPD-TD]
[16] Punzi & Del Viva (2006) Visual features and information theory JOV 6(6) 567. See also among others, Luciano Ristori, An artificial retina for fast track finding, Nuclear Instruments and Methods in Physics Research A 453 (2000) 425-429.

can also profit of cheaper custom electronics developed in the NEURONS project. The key feature is a very short processing time that scales linearly with the amount of data to be processed. This means that clustering can be performed in pipeline with the image acquisition, without suffering from combinatorial delays due to looping multiple times through the whole amount of data.

- **High Energy Physics and Nuclear Fusion Technology**.

Future high-energy particle physics experiments looking for rare processes constitute an excellent top demanding challenge for fast pattern recognition. The Large Hadron Collider (LHC) at CERN has planned a luminosity increase of a factor of ten over the original design as the goal for the upgrade in the coming years, which will result in a corresponding increase in fundamental particle interactions and track densities in different detectors (i.e. ATLAS, CMS, etc). Most of these interactions contain events that are of no significance and should not be recorded. Since the quantity of data that can be stored for later analysis is limited, real-time event selection is imperative to retain the interesting events while rejecting the background and the capability to perform fast pattern recognition and track reconstruction of particle trajectories will be crucial. The ultimate physics reach of the LHC experiments will crucially depend on the tracking trigger's ability to help discriminate between interesting rare events and the background. In order to give an idea of the magnitude of the challenge that the AMMA-chip will demonstrate in terms of intensive and parallel processing of data it is sufficient to consider that the ATLAS detector at CERN generates a data flow of about 600Gbits/s to be processed on line. This a factor 200 more than the 500MBps reported in current examples for challenges of "hardware technologies for High-Performances Data-Intensive computing"[17]. Similar numbers apply in the case of the CMS detector at CERN. Very powerful AMMA-chip-based processors will be used in the online data taking at both experiments. This strategy enriches a lot the acquired physics samples but also opens new large problems in the offline area. In fact to perform precise offline analysis of the different samples, the trigger efficiency has to be evaluated with accuracy for each channel. For this goal a lot of Monte Carlo events have to be simulated reproducing exactly the hardware functions. However, reproducing the functionality of 16400 AMMA-chips working in parallel (this is the AM computing power of the FTK (Fast Tracker) processor for example) with conventional CPUs is extremely difficult. The job to simulate one event reconstruction requires an extremely large memory that the GRID nodes do not have. For this reason the execution of one event simulation is split into 128 jobs working in parallel on GRID, whose outputs have to be merged together. It is easy to imagine that this system can be exploited for development studies, but cannot be used for massive event production as will be requested when the online super computers will participate to all trigger decisions, and each trigger decision will need thousands of simulated events. It is much more natural to use a battery of AMMA-chips in the simulation, instead of making efforts to simulate them in conventional CPUs. The NEURONS demonstrator will become a co-processor or an accelerator for offline trigger simulation. The NEURONS demonstration will consider the download of the ATLAS and CMS detectors' hits in a chaotic order and track seeds (i.e. groups of hits consistent with being produced by a real fundamental physics particle) will be identified by the AMMA-chip. The track seeds will be used by the FPGA algorithm to find all the full-resolution tracks searched by the trigger application.

A challenging field to demonstrate the high potential of the technology developed by the NEURONS project is the area of Nuclear Fusion. The NEURONS project foresees a highly demanding test for demonstrating the performance capacity of the technology developed. A unique feature in the operation of fusion energy experiments such as ITER (International Thermonuclear Experimental Reactor) is the requirement to access, analyze, visualize and assimilate data, between shots ("shots" are the basic units of fusion experiments) in near-real-time, to support decision making during operation[18].The quantity of data itself is estimated at 2 PB (peta bytes) per year. One of the critical issues that the capacity to process such amount of data will bring is the safe and optimal exploitation of nuclear fusion research experiments which requires a precise and accurate feed-back control of several plasma parameters. The inputs to such controllers are provided by a wide range of plasma diagnostics, which usually require data acquired both with high spatial and timing accuracy to be processed with very low latency. One of the most important aspects of the operation of a nuclear fusion experiment is the precise determination of the plasma boundary shape, as this is strongly correlated to the performance of the fusion experiment and ultimately to the amount of heat load that is transferred to the device first wall. The plasma shape is usually determined using as input large sets of magnetic probes. Although robust, this method is prone to fail when faults develop in any of the magnetic sensors and it can be severely degraded in the presence of plasma instabilities. Real-time tomography of plasma radiation provides an alternative method for the calculation of the plasma shape that can complement other diagnostics and be used to validate the plasma shape, serving as an alternative source in the case of

[17] M.Gokhale et al., Hardware Technologies for High-Performance Data-Intensive Computing, Computer, IEEE Computer Society, 41 , Issue: 4, 2008, 60-68. See also: I. Gorton et. Al, Data-Intensive Computing in the 21st Century Computer, IEEE Computer Society, 41 , Issue: 4, 2008, 30-32.

[18] "Visions for Data Management and Remote Collaboration on ITER", M. Greenwald, et al., Proceedings of the 10th International Conference on Accelerator and Large Experimental Physics Control Systems, 2005.

failure of other diagnostics. One of the major limitations of real-time tomography is that the algorithm results strongly depend on the selected initialization values, in particular when the lines of sight are sparse. The NEURONS project will overcome this limitation by using the newly developed AMMA-chip and exploiting its massive parallelism in data correlation searches by comparing the input data simultaneously to a list of pre-calculated expected tomographic reconstructions (pattern matching), so that a great increase in accuracy can be achieved without affecting real-time performance. Tomography algorithms are typically time-consuming. The higher the resolutions of the reconstruction mesh or the more input signals are available the more time they tend to take to provide a reconstruction. Neural Networks (NNs) encoded in the field programmable gate arrays (FPGAs) of the NEURONS project can provide the speed to obtain tomographic reconstructions in real time (RT). As mentioned in previous sections Associative Memories (AM) are a form of NN which stores patterns that can be retrieved at a later time by providing the expected input. The AM is trained to expect standard tomography signals as inputs and to provide the reconstruction as output. One drawback of AMs is that they only retrieve a pattern that was provided to them during training. It is then imperative that the AM is trained with as many relevant patterns as possible and as little irrelevant ones. This training is performed offline, so it has no impact on RT performance. The RT stage consists mainly of a matrix operation on the input vector of data. This task can be implemented on an FPGA, parallelizing all the vector operations and providing the result in very few processing cycles. Other more accurate real-time tomography reconstruction algorithms, such as first order regularization, required when the lines of sight are sparse as it is the case in several applications, will benefit from an insight as first guess of the reconstruction. The AMs may be used for this initialization improving the reconstruction accuracy, by avoiding local minima on the algorithm, while maintaining RT performance. The NEURONS project will develop the firmware for the AMMA Board to extend the existing algorithm for extraction of salient visual patterns (features) to nuclear fusion plasma experiments. Additionally, the necessary software to manage the readout system and image processing unit connected together will be developed. This software, used together with the AMMA board and the ATCA AMC Digitizer, will give the opportunity to explore the advantages of an AMMA-chip pattern based system for real-time control in nuclear fusion plasma experiments. The realization of this demonstration will certainly open up new avenues for achieving the new requirements and be capable of adapting towards the migration to new technologies and to new computing platforms that fusion technology will require.

1.1.2.4 Connection of the Objectives of NEURONS with the Work Programme

The NEURONS projects constitutes a joint effort of different expertise in the areas of embedded computing and high performance computing capable of delivering breakthrough technology and address the challenges that this goal implies. The following table 1.1.1. summarizes the close connections that the NEURONS project has with the objectives foreseen in the Work programme:

Work Programme	**NEURONS project**
Bringing together teams from embedded computing and high-performance computing to jointly address challenges that are common in these two areas and are magnified by the ubiquity of many-cores and heterogeneity across the whole computing spectrum.	The NEURONS project brings together different academic and industrial partners that are leading experts in embedded computing (i.e. PRIELE, Univ. Thessaloniki,) and high-performance computing (i.e. INFN, LPNHE, Univ. Heidelberg, IMEC, Microtest, Univ. Genova etc) complemented by partners specialised in demonstrating the capabilities of the newly developed technology in different fields (i.e. CAEN, UCL, Univ. Florence, etc). This join effort will allow building the new NEURONS's computing unit, based on many cores whose elementary unit is the AMMA-chip, and also achieving the final goal of coupling FPGA-AMMA-chip into a heterogeneous unit that combines embedded computing flexibility with high computing power.
Challenge: Low power & Energy Efficiency	Achieving the goal of increasing the AMMA-chip pattern densities (different strategies will be pursued and compared) while keeping the core and IO consumptions below 1 watt and half watt respectively. The NEURONS elementary unit will need ~60 Watt, a low consumption compared to what would be necessary to reach the same computing power with commercial CPUs.
Challenge: Performance Analysis	The complex computing system that the NEURONS project will develop requires a built in system to analyse the system performance. The expert partners on high-performance computing will define the necessary tools. Each stage of the pipeline will have de-randomizing First-in-first-out (FIFOs) at the input and a set of counters to monitor the event processing time in the stage to identify bottle-necks in the system. The teams from embedded computing will optimize the control of the pipelines and the input/output file management.
Challenge: Dependability	The system's availability, reliability, and its maintenance support is strongly related to the available expertise on the system. The low cost and the compact nature of the system favour

	the availability of spares and easiness of replacement and redundancy, however expertise to detect the problem and replace a piece requires additional competences compared to the standard system management work. For this reason it is very important to enlarge the knowledge and use of these hybrid systems and the dissemination activity has a very important role. The SME companies participating to the project could have a determinant role in this direction.
Challenge: Time-criticality	The NEURONS's elementary unit will be extremely efficient when optimized for a specific task. At the CERN ATLAS detector, it has been demonstrated via simulation to be ~1000 faster than an Atlas CPU performing the same physics task. The NEURONS consortium will work to demonstrate its capability in different applications. Cross fertilization with the embedded system experts will guarantee an efficient I/O with the external word. "Time criticality" will be maintained as a primary goal in the implementation of a good connection with the outside.
Challenge: Parallelisation	The NEURONS system will be data driven and made of many parallel pipelines. To have a sketch of how much it can grow we can compare to the online ATLAS detector Fast Tracking System (FTK) at CERN that will start to be active in 2015. FTK will have ~2000 FPGAs and 16500 AMMA-chips organized in 512 pipelines and connected by thousands of dedicated high frequency S-links. High parallelism is guaranteed by the high number of cores and the very powerful I/O structure.
Challenge: Debugging	Debugging for such large number of cores and links will constitute a challenged addressed by NEURONS. The project will propose to use its expertise on a circular memory buffer that records—as a logic state analyser—the last 10^5 words sent or received on a pipeline. Comparing a board's input and output with emulation software checks data processing. The memories also serve as sources and sinks of test patterns for testing single boards, a small chain of boards, a slice of the system. The buffers can be frozen and read by monitoring software parasitically during data-taking, when any board detects an error condition, such as invalid data. By polling the circular memories during running, large samples of data are sampled and statistically analysed to monitor data quality.
Challenge: Co-design, Compilation and Hybrid Programming	The NEURONS project counts with the expertise for designing and fabricating complex electronics components at the system level (dedicated AMMA chips and FPGAs, a wide range of high speed serial links). The design of these systems requires designers to be knowledgeable in both hardware and software domains to make good design trade-offs. Digital hardware design has increasingly more similarities to software design. Hardware circuits are often described using modelling or programming languages, and they are validated and implemented by executing software programs, which are sometimes conceived for the specific hardware design. These "systems on silicon" exhibit a sizable amount of embedded software, which provides flexibility for product evolution and differentiation purposes. Some of this hybrid experience will be necessary also at the user level. With the NEURONS project we plan to develop the hardware, but also the experience to handle efficiently this hybrid system. With a large demonstration program we plan to build an exploitation environment that will take into account and will face all these aspects before eventually going to the next step, the commercialization.
Challenge: Virtualisation	Certainly this computer is conceived for an application at a time, it looks based on the old model "one server, one application". However if a large number of AMMA-Boards will exist on the network, virtualization could centralize administrative tasks while improving scalability and overall hardware-resource utilization. Virtualization could better manage updates and rapid changes to the different applications improving the efficiency and availability of resources. Certainly it is an important challenge. We will face it after the acquisition of the NEURONS demonstrator experience.
Challenge: Customisation and Reconfigurability	Reconfigurability and customization are key aspects that can make powerful and multi-purpose the technology developed in NEURONS. The demonstration activities will have a determinant role to show the flexibility of the hardware facing the different applications as well as set the avenues for future ones as part of the project exploitation plan.
Real cross-fertilisation of expertise.	The NEURONS project certainly constitutes a true example of cross-fertilization expertise that can be highlighted in two aspects: • Cross-fertilization between experts teams of embedded computing and high performance computing. • Cross-fertilization between industrial technology designers and cutting edge research in the

	fields above. • Cross-fertilization in demonstration areas for the developed technology such as medical, high energy physics, computer vision, image processing, etc. This constitutes the NEURONS project as a landmark project in innovation.

Table 1.1.1 Objective foreseen in the Work programme addressed by the NEURONS project

1.2 Progress beyond the state-of-the-art

1.2.1. Associative Memories: state of the art and applications

Associative Memories devices (AMs)[19] exploit massive parallelism in data correlation searches by comparing the input data simultaneously to a list of pre-calculated "expectations" (pattern matching). These correlations (i.e. the matched patterns) are found by the time input data are loaded into the devices.

One of today's commercial applications of AMs is to classify and forward Internet Protocol (IP) packets in network switches and routers[20]. These two devices need to do a highly demanding job: faster routing or switching of packet based data through the network by performing table lookups. Traditional solutions have been based on software algorithms but the number of operations required exceeds performance limits. AMs hardware-based solutions allow for much greater speed and performance acting as a "co-processor" to the CPU by offloading the task of table lookup, providing multidimensional classification, lower latency and higher throughput therefore allowing for wire-speed packet processing. Another key application is signature recognition[21]. In this context one of the foremost demands that the Internet needs is data protection. With new ways coming in vogue to hack an end point, the need for protection from such attacks, be it through a virus or a spam, is extremely necessary. AMs help in such a cause by maintaining a signature data base in which an associate processor can scan the packets for such signatures and drop packets if necessary; such functionality adds immense value to the security regarding the content moved across the Internet. AMs are successfully implemented as well in the field of biometrics especially for handwritten signature recognition and verification[22] and face recognition[23]. In this task AMs offer the advantage of performing signature verification with lowest errors in least time due to the high parallelism in pattern recognition related task. The parallel implementation distributes the computation work to multiple processors and achieves the required results in a minimal CPU time. As mention before data stored in AMs are accessed by their contents allowing extreme parallelism. This is in contrast to random-access memory (RAM) in which data items are accessed according to their address. The ability to retrieve data by association is a very powerful technique required in many high-volume information processing applications. For example, AMs have been used to perform real-time radar tracking. They are also used in database applications, image processing, and computer vision. Further AM-based applications taken again advantage of the AM's massive parallelism contemplate areas such as image recognition in different Healthcare disciplines, prediction of complex systems dynamics (i.e. meteorology, climate models), processing of Big Data, brain-like computer architectures, etc. (table 1.2.1.)[24].

The major advantage that AMs offers over RAM regarding the capability of rapidly retrieving data through the use of parallel search and comparison operations makes them fundamental elements in the vast area of applications where Artificial Neural Networks (ANN) are used nowadays as well as envisioned for the coming decades. ANNs offer a computational approach that is quite different from conventional digital computation. Digital computers operate sequentially and can do arithmetic computation extremely fast. ANNs are a parallel, distributed information processing structure consisting of processing elements interconnected via unidirectional signal channels called connection weights. Some of the major attributes of ANNs are:

a) they can learn from examples and generalize well on unseen data, and
b) are able to deal with situations where the input data are erroneous, incomplete, or fuzzy.

Although developed as a model for mimicking human intelligence into machine, ANNs have excellent capability of learning the relationship between input-output mapping from a given dataset without any knowledge or assumptions about the statistical distribution of data. This capability of learning from data without any a priori knowledge makes neural networks and therefore AMs particularly suitable for classification and regression tasks in practical situations. In most financial and

[19] Kostas Pagiamtzis, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 3, MARCH 2006, 712-727.
[20] E. Jih, IIC-China ESC. China 2002. Conference Proceedings.
[21] P. Hans, Electronics Spectra, 2010, 18-20.
[22] T. Dash, International Journal of Advanced Research in Computer Engineering & Technology Volume 1, Issue 4, June 2012.
[23] See among others, Karm Veer Arya et al. Face Recognition using Parallel Associative Memory, IEEE International Conference on Systems, Man and Cybernetics (SMC 2008).
[24] B.D.C.N. Prasad et al. Study on Associative Neural Memories, (IJACSA) International Journal of Advanced Computer Science and Applications, Vol. 1, No. 6, December 2010A.

manufacturing applications, classification and regression constitute integral parts. Neural networks are also inherently nonlinear which makes them more practical and accurate in modelling complex data patterns as opposed to many traditional methods which are linear. In numerous real-world problems including those in the fields of finance and manufacturing, ANNs applications have been reported to outperform statistical classifiers or multiple-regression techniques in classification and data analysis tasks. Because of their ability to generalize well on unseen data, they are also suitable to deal with outlying, missing, and/or noisy data. Neural networks have also been paired with other techniques to harness the strengths and advantages of both techniques.

Area	Associative Memories Examples of Application Fields/data input to be processed
Human Resources Management	• Employee Selection and Hiring - predict on which job an applicant will achieve the best job performance. Input data: information about an applicant: personal information, previous jobs, educational levels, previous performance, etc.
Medical	• Medical Diagnosis - Assisting doctors with their diagnosis by analysing the reported symptoms. Input data: patient's personal information, patterns of symptoms, heart rate, blood pressure, temperature, laboratory results, medical images, etc. • Detection and Evaluation of Medical Phenomena - detect epileptic seizures, estimate tumour size, detects patient breathing abnormalities when a patient is under anaesthesia, etc. Input data: patient's personal information, breathing rate, heart rate, patterns of symptoms, blood pressure, temperature, etc. • Patient's Length of Stay Forecasts - forecast which patients remain for a specified number of days. Input data: personal information such as age and sex, level of physical activity, heart rate, blood pressure, temperature and laboratory results, treatment procedures, etc. • Treatment Cost Estimation Input data: personal information such as age and sex, physiological data, the use of drug or other therapies, treatment procedures, number of recurrences after first treatment, etc.
Financial	• Stock Market Prediction - predict the future movement of the security using the historical data of that security. Input data: Open, High, Low, Close, Volume, technical indicators, market indexes and prices of other securities. • Bankruptcy prediction - classify a company as potential bankruptcy. Input data: company characteristics and business ratios, such as working capital/total assets, retained earnings/total assets, earnings before interest and taxes/total assets, market value of equity/total debt, and sales/total assets. • Fraud Detection - detect and automatically decline fraudulent insurance claims, client transactions, and taxes. Input data: transaction parameters, applicant's information and other data of past incidents. • Economic Indicator Forecasts - forecast economic indicators for the next week, month, and quarter. Input data: social and economic indicators, time-series data of an indicator.
Sales and Marketing	• Sales Forecasting - predict future sales based on historical information about previous marketing and sales activities. Input data: historical data about marketing budget, number of ads, special offers and other factors affecting sales. • Targeted Marketing - reduce costs by targeting a particular marketing campaign to the group of people which have the highest response rate. Avoid wasting money on unlikely targets. Input data: information about customers and their response rate.
Industrial	• Process Control - determine the best control settings for a plant. Complex physical and chemical processes that may involve interaction of numerous (possibly unknown) mathematical formulas can be modelled heuristically using a neural network. • Quality Control - predict the quality of plastics, paper, and other raw materials; machinery defect diagnosis; diesel knock testing, tire testing, milk testing. Input data: product/part/machinery characteristics, quality factor. • Temperature and force prediction in mills and factories Input data: previous values of temperature, force and other characteristics of mills and factories.
Operational Analysis	• Retail Inventories Optimization - forecast optimal stock level that can meet customer needs, reduce waste and lessen storage; predict the demand based on previous buyers' activity.

	Input data: characteristics of previous buyers' activity, operating parameters, season, stock, and budgets. • Scheduling Optimization - predict demand to schedule buses, airplanes, and elevators. Input data: season, day-of-week, hour of the day, special events in the city/area, Weather, etc. • Managerial decision making - select the best decision option using the classification capabilities of neural network. Input data: initial problem parameters and final outcome.
Data Mining	• Prediction - use some variables or fields in the database to predict unknown or future values of other variables of interest. • Classification - map (classify) a data item into one of several predefined classes. • Change and Deviation Detection - uncover certain data records that are in some way out of the ordinary records; determine which cases/records suspiciously diverge from the pattern of their peers. • Knowledge Discovery - find new relationships and nonobvious trends in the data. • Response Modelling - build a neural network based response model. • Time Series Analysis - forecast future values of a time series.

Table 1.2.1. Application fields of Associative Memories (Ref. B.D.C.N. Prasad et al. Study on Associative Neural Memories, (IJACSA) International Journal of Advanced Computer Science and Applications, Vol. 1, No. 6, December 2010A.

In this context ANNs have drawn tremendous interest due to the demonstrated successful applications in a vast spectrum of fields[25] -such as pattern recognition, image processing, document analysis, engineering tasks, financial modelling, trading and forecasting, manufacturing, biomedical, optimization, quality control, gaming, modelling water resources, cryptosystems, etc. The future of AMs in relation to their use in ANNs also foresees the appearance of breakthrough hardware and software technologies and leveraged applications that will allow for revolutionary avenues to understand and implement computation. An example of this is the field of brain-like computers known as well as cognitive computers[26,27]. Cognitive Computing (CC) is an emerging paradigm of intelligent computing methodologies and systems based on cognitive informatics that implements computational intelligence by autonomous inferences and perceptions mimicking the mechanisms of the brain. The extreme importance of AMs in this field stems from the fact that the associative memory capabilities and architectures fit perfectly well with the vision of human cognition emergent from today brain neuro-imaging techniques. Our memories function as an **associative** or **content addressable**. That is, a memory does not exist in some isolated fashion, located in a particular set of neurons. Thus memories are stored in *association* with one another. These different sensory units lie in completely separate parts of the brain, so it is clear that the memory of the person must be distributed throughout the brain in some fashion. We access the memory by its contents not by where it is stored in the neural pathways of the brain. This is very powerful; for example, given even a poor photograph of a person we are quite good at reconstructing the persons' face quite accurately. This is very different from a traditional computer where specific facts are located in specific places in computer memory. If only partial information is available about this location, the fact or memory cannot be recalled at all. Traditional measures of AMs performance are its *memory capacity* and *content-addressability*. Memory capacity refers to the maximum number of associated pattern pairs that can be stored and correctly retrieved while content addressability is the ability of the network to retrieve the correct stored pattern. Obviously, the two performance measures are related to each other. Cognitive Computers represent a sub-field of the vast area known as Cognitive Informatics (CI) which constitute the ICT emerging paradigm and in which AMs are playing and will play a fundamental role[28]. Cognitive informatics (CI) is a trans-disciplinary enquiry of cognitive and information sciences that investigates into the internal information processing mechanisms and processes of the brain and natural intelligence, and their engineering applications via an interdisciplinary approach. Cognitive Informatics constitutes an interdisciplinary research and breakthrough innovation area that tackles the common root problems of modern informatics, computation, software engineering, AI, cognitive science, neuropsychology, computational intelligence, and life sciences. A wide range of applications of CI has been identified in multidisciplinary areas, such as the architecture of future generation computers known as the cognitive computers, explanation of human memory mechanisms and capacity, cognitive properties of information, data, knowledge, and skills in knowledge engineering, simulation of human cognitive behaviors using

[25] Koushal Kumar, Advanced Applications of Neural Networks and Artificial Intelligence: A Review, I.J. Information Technology and Computer Science, 2012, 6, 57-68

[26] IEE Times report 8/18/2011: IBM demos cognitive computer chips, available at http://www.eetimes.com/electronics-news/4218883/IBM-demos-cognitive-computer-chips . Also:

[27] D. S. Modha et al. Cognitive Computing, Communications of the ACM, August 2011, vol. 54, no. 8, 62-71.

[28] Y. Wang et al, Cognitive Informatics and Cognitive Computing in Year 10 and Beyond, International Journal of Cognitive Informatics and Natural Intelligence, 5(4), 1-21, October-December 2011.

descriptive mathematics, development of autonomous agent systems, studies on the CI foundations of software engineering, cognitive complexity of software systems, and the implementation of autonomous machine learning systems[29].

1.2.2. NEURONS project: beyond the state of the art

The NEURONS AMMA-board has different functionality compared to commercial CAMs and Associative Memories described in the above section. The AMMA-chip in fact, is not simply able to recognize and retrieve a particular pattern, but it is also able to find coincidences of N objects recognized at different times. This features for example allows to detect a searched object observing only a certain number of peculiar fragments of it, without pretending the matching of the whole object, whose image could be partial or imperfect or noisy, or too large to be analysed as a whole. As an example we could imagine an application where images with many faces are first of all filtered to put in evidence the contours, than analysed by the FPGA to find shapes that could be classified as eyes, noses, mouths, and reduced to the resolution of templates that are downloaded in the AMMA-chips with a lot of possible different flavours, including the change in facial expressions. A particular face could be recognized as the match of a particular eye with a particular nose and other parts of the face. The match is tolerant for missing parts, thanks to the implementation of the majority, and also the single piece matching can be made tolerant for noise or poor lightening condition. The combination of the AMMA-chip with its peculiar structure and the FPGA ability to provide the right missing functionality, will improve the results that usually are obtained only with the use of complex neural networks, more difficult to implement in large scale hardware systems. As the trend of using a combination of CPUs and ASIC or FPGA based hardware is expanding in the real-time massive computing realm, the NEURONS project AMMA-Chip implements an innovative strategy, based on the optimal mapping of a complex algorithm in different technologies. The purpose is to get the best results by innovatively combining the high performances of rigid dedicated hardware with the distinctive flexibility of general-purpose but lower-performance CPUs. The architecture's key role is played by high-level field programmable gate arrays (FPGA), while most of the computing power is provided by cooperating full-custom multicore ASICs of the AMMA-chip. In this sense the NEURONS project is certainly at the forefront area of "multistep analytical pipelines", where FPGAs and AMMA-chips are different steps of the pipeline. The AMMA-chip takes full advantage of the intrinsic parallel nature of the combinatorial problem and drastically reduces to linear the exponential complexity of CPU-based algorithms. The speed of AMs comes at the cost of increased silicon area and power consumption, two critical design parameters that designers strive to reduce. As AMs applications grow, demanding larger AMs sizes, the power problem is further exacerbated. Reducing power consumption, without sacrificing speed or area, is the main thread of recent research in large-capacity AMs. Besides silicon area and power consumption a critical figure of merit for AMs is the number of patterns that can be stored in the memory bank. The table 1.2.2. below offers a clear comparison of the figures of merit that the AMMA-Chip will improve with respect state of the art (see ref. 29 among others).

	State of the art	NEURONS project AMMA chip	Effect
Technology	180 nm	65 nm + custom pattern cell	Higher pattern density
Clock freq.	50MHz	100 MHz	Higher rate, lower latency
Die size	10 mm	2 dies 6x10 =120 mm^2	Higher yield - 2.5 D multi-packaging
Core voltage	1.8 V	1.2 V(potential to reach 1 V)	Lower consumption
Core power	1.3 W	1 W	Lover consumption relevant for vertical multi-packaging
Selective. Pre-charge.	No	yes	Lower consumption
Full custom	No	yes	Higher pattern density
Layers	6 (or 12)	8 (or 4)	Increased number of patterns
Patterns /chip	5k	Multi-packaged to reach 64 kpatterns per chip. Possibility to achieve higher densities (256 kpatterns) in project WP5 through 3D integration architectures.	Higher densities
Bits/layer	Up to 18	15	Increased number of patterns
Ternary/ Layer	N/A	Yes	Much more powerful memory bank

Table 1.2.2. Comparison with available state of the art figures of merit of Associative Memories and the achievements of the NEURONS project newly developed ones.

[29] Proceedings of the 10th IEEE International Conference on Cognitive Informatics and Cognitive Computing (ICCI*CC 2011) : Banff, Alberta, Canada, 18 - 20 August 2011.

The NEURONS project will develop a novel multicore "Associative Memory for Multi-Applications" (AMMA), taking advantage of very large scale integrated (VLSI) fabrication processes in the 65 nm technology node. The newly developed AMMA will be highly superior in performance as compared to existing state-of-the-art ones that have been developed using 180 nm technology actually in use[30] (see table 1.2.2). The NEURONS project will push fabrication technologies and therefore performance to the limits in 2D as well as explore 3D configurations seeking the integration of much larger banks inside the AMMA-chip in aggressive 65 nm technology. This breakthrough goals will be pursued working in different directions.

- First of all the NEURONS project will optimize the 2D design to occupy the maximum die size allowed by the package, keeping the power consumption at the minimum level to be able to package two AMMA-chips one over the other (2.5 D). In this case communication between different chips is limited to contacts between peripheral pads.
- Secondly the NEURONS project will develop a concept with a cutting-edge technological solution for the 3-Dimensional (3D) AMMA-chip. The idea behind this 3D integrated Circuit (IC) design development is to mount two or more 2 D dices on top of each other, and interconnect them by using Through Silicon Vias (TSVs) vertical technology. The 3D AMMA-chip integration is a viable and promising option to address the well-known memory wall problem in high performance computing system as with currently available AMs.

Another benefit with this 3D concept is that it allows the integration of otherwise incompatible technologies (Heterogeneous integration), this will give huge advantages when it comes to performance, functionality, and form factor. 3D technology will offer the possibility of even n superior pattern density obtained at a lower fabrication cost. Going as well for 3D architectures will allow increased pattern densities at an increased speed with decreased power density. The improved pattern density will be achieved from a reduction in the area required to build the 3D AMMA-chip through transistor reduction combined with vertical integration. The decreased power density will be achieved from a reduction of transistors and a minimization of parasitic capacitance. The increased speed is directly derived from the potential implementation of novel architectural modifications such as the Fischer Tree for readout.

The AMMA-chip demonstration scenarios will constitute a key innovation implementation route with respect to real time image analysis. This field has undergone a rapid development in the last few years, due to the increasing availability of low cost computational power. However computing power is still a limit for some high quality applications. High-resolution medical image processing, for example, are strongly demanding for both memory (~250 MB) and computational capabilities for allowing 3D processing in affordable time. The AMMA-chip will allow the reduction of execution time of image processing exploiting the computing power of parallel arrays of Field Programmable Gate Arrays (FPGAs) coupled to it. The NEURONS project will apply this idea to develop an algorithm that finds clusters of contiguous pixels above a certain programmable threshold and process them to produce measurements that characterize their shape. The dynamic image analysis proposed by the project NEURONS demonstrations will open new avenues in medical imaging for real time, fast diagnosis. Image processing performed at high rate would increase substantially the capability to perform exams for large categories of people, increasing the capability of early detection of cancer or other diseases such as Alzheimer, etc. The demonstration of the NEURONS project concerning data processing in the CERN detectors ATLAS and CMS will help directly to achieve key advances on the deep understanding of fundamental physical laws. The philosophy of performing almost offline selections at rates of the order of 20-40 kHz at LHC, or even more, is absolutely new. The idea of using dedicated mixed-technology for high parallel data processing is innovative in a world where the use of dedicated hardware has been strongly reduced. The NEURONS project constitutes a unique opportunity for demonstrating the worldwide high-energy community the capability of the AMMA-chip. The very precise LHC silicon detectors, which contain hundreds of thousands or millions of channels, increase the problem of complete particle tracking in large numbers of high multiplicity events. With hundreds or thousands of particles produced by multiple primary collisions and traversing many detector layers in all directions, this is a formidable challenge even for off-line analysis. A complete high-quality tracking for real time event selection has been considered impossible in LHC experiments at very high rates. As a consequence, real-time tracking is planned for a limited detector region or on a small subset of events, previously selected using other detectors. Many physicists dismiss a complete on-line tracking in LHC experiments because they see it as a too formidable problem. The goal of the NEURONS project is to prove that its newly developed technology, complemented with suitable organisation and algorithms, permits the development of high-performance particle tracking. The search for new physics not covered by the Standard Model requires collecting enormous samples of data in extreme conditions to improve the precision of future measurements. This gives increasing importance to parallel computing and dedicated real-time techniques such as the ones developed and implemented by the NEURONS project. The demonstration scenarios of the AMMA-chip planned in the NEURONS project will open the way to the application fields contemplated in the section of state-of-the-art regarding AMs. As mentioned in that section, the use of a tuned combination the AMMA-chip and FPGAs

[30] See among others A. Annovi, et al., "A VLSI processor for fast track finding based on content addressable memories," IEEE Trans. Nucl. Sci., vol. 53, no. 4, pp. 2428–2433, Aug. 2006.

will open up application fields nowadays closed by lack of enhanced parallel data processing power. The same approach demonstrated in NEURONS could be very incisive for astrophysical and meteorological calculations, for robotic automation, cybersecurity applications, complex systems analysis such as climate change models, financial forecasting, multimedia databases development based on image content rather than metadata, etc. It could be essential for neurophysiologic studies of the brain. Recent advances in ICT and neuroscience allowed to study and model "in silico" a significant part of the human brain. The brain is certainly the most complex, powerful and fast processing engine and its study is very challenging. The architectures for information processing developed by the NEURON project will pave the way for understanding how the brain processes information or how it communicates with the peripheral nervous system (PNS) which could provide new potential applications, new computational systems that emulate human skills (e.g. by using the directed fusion of diverse sensory information) or exploit underlying principles for new forms of general purpose computing.

The developed technology of the NEURON project will report significant improvements in terms of performance, fault tolerance, resilience or energy consumption over traditional ICT approaches. In this sense the potential use of the AMMA-Chip for brain studies is particularly fascinating. The most convincing models that try to validate brain functioning hypotheses are extremely similar to the real time architectures developed in the NEURONS project. A multilevel model seems appropriate also to describe the brain organization to perform a synthesis certainly much more impressive than what is foreseen in the NEURONS project for the CERN detectors ATLAS and CMS. The AMMA-chip parallelism for pattern matching will play a key role in high rate filtering/reduction tasks. As mentioned the NEURONS project will demonstrate a very innovative approach in the area of computer vision. NEURONS will test the AMMA-chip device capability at the first levels of this process, dedicated to external stimuli pre-processing. In this sense the NEURONS project will be able to test cutting-edge conjectures[31] stipulating that the brain works by dramatically reducing input information by selecting for higher-level processing and long-term storage only those input data matching a particular set of memorized patterns. The double constraint of finite computing power and finite output bandwidth determines to a large extent what type of information is found to be "meaningful" or "relevant" and becomes part of higher level processing and longer-term memory. The AMMA-chip based processor will be used for a real-time hardware implementation of fast pattern selection/filtering of the type studied in these models of human vision and other brain functions. This demonstration therefore has the potential to constitute an initial landmark towards developing novel paradigms in computing concepts and architectures.

1.3 S/T methodology and associated work plan

i) overall strategy of the work plan

The methodology of the NEURONS project is structured around 4 work packages together with WP1 and WP6 which are dedicated to project management and dissemination and exploitation activities respectively, see workflow structure shown with the pert diagram further below on page 44.

WP2 is dedicated to the development of the AMMA-chip ASICs contemplating the Associative Memory function. The work will be focused on full custom block design of the Associative Memory basic cell and standard cell for the control logic design. Global placement and routing strategy will be developed. Simulations will be performed to verify the functionality and compliance with the desired power consumption and speed. The resulting design will be taped-out on TSMC 65 nm MPW masks through Europractice and will result in two bunches of prototypes, a first set of 100 that will be tested at INFN to verify the functionality and to ensure that the prototype is compliant with the specifications, followed by other 500 AMMA-chips necessary to build the demonstrators for WP4. A packaging solution for 2D multi-die package of AMMA-chip cores will be developed and a concept of test including software development will be established to test the 500 AMMA-chips in the Microtest's machines.

WP3 is dedicated to the building of the computing unit, which is formed by a set of boards with accompanying firmware and software. The boards will be either a part of the final computing unit or needed for test purposes. The boards meant for test purposes are a mezzanine board and a small interface board (Load Board). The mezzanine board will be built to host an AMMA-chip on a ZIF socket, able to be plugged-in and unplugged on the mezzanine to test the first AMMA-chip prototypes and to define the test vectors and procedures for a very fast execution of the 500 AMMA-chips provided in WP2. The mezzanine will be plugged on the AMMA-Control-Board. The small interface board is needed between the AMMA-chip and the test machine that will execute the tests of the 500 AMMA-chips. To build the computing unit a commercial control board with fast FPGA and embedded CPU will be acquisitioned and connected with a custom-made board, the LAMB, hosting the AMMA-chips provided in WP2. The LAMB board will be designed in such a way to be plugged in the FPGA control board. **The idea is to use the AMMA-chips to reduce in a very fast way the amount of data which are subsequently handled by the FPGA. Therefore, the computing unit will be able to solve problems requiring high computing**

[31] Punzi & Del Viva (2006) Visual features and information theory JOV 6(6) 567.

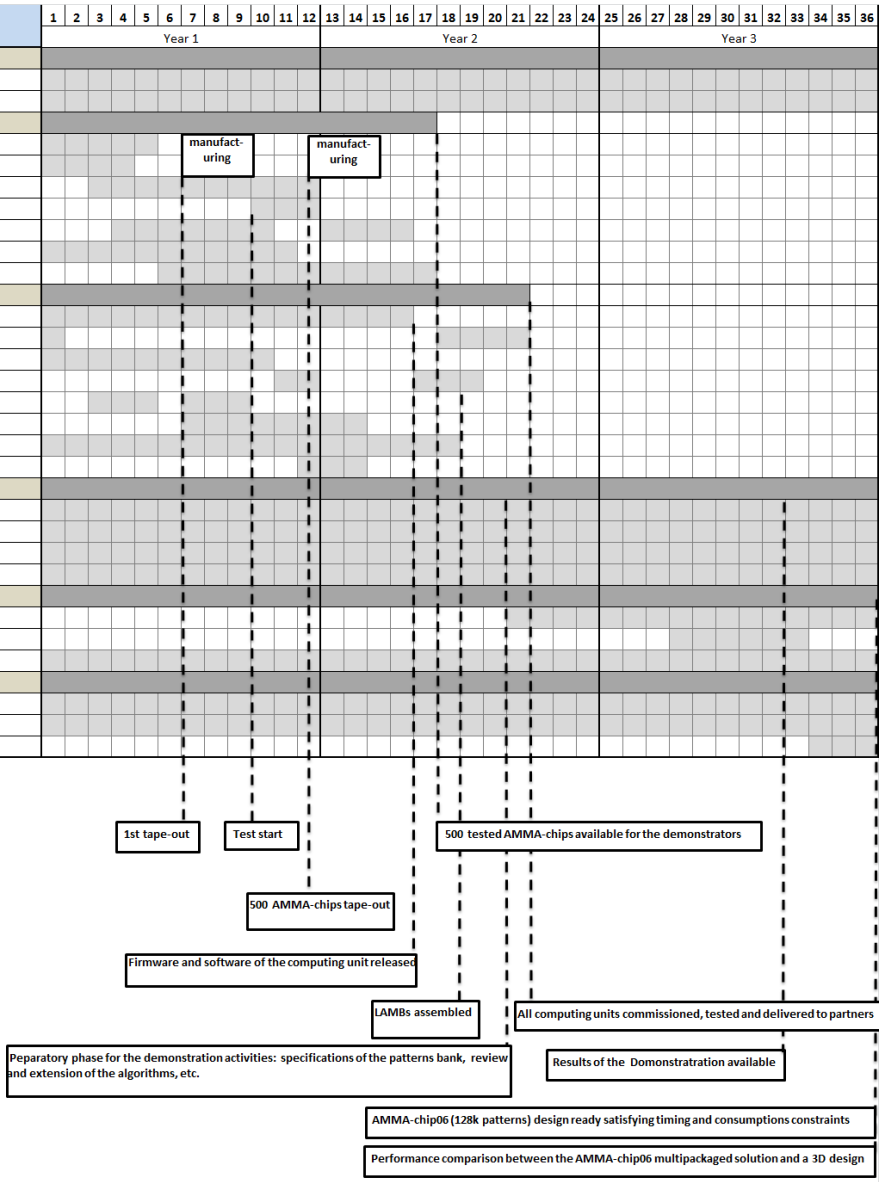
power in little time. In this WP firmware and software will be developed for the control board such as the communication of the control board to other devices, the distributing and collecting of information from the AMMA-chips, the configuration and controlling of the pattern banks on the AMMA-chips, etc. A test procedure for the assembled LAMB will be defined and executed to guarantee the hardware correct functioning before commissioning. All computing units (integrate FPGA control boards with LAMBs) will be commissioned with the firmware and software developed to deliver functioning products to all partners of the project, so that all partners have the same hardware with the same basic firmware and thus, have the same platform to develop the demonstration prototypes. Additionally, the readout system for the Plasma Tomography demonstrator will be developed in WP3 based on existing ATCA-AMC boards.

WP4 is dedicated for demonstrating the capabilities of the newly developed computing unit based on the AMMA-chip in four domains of applications requiring fast data processing: i) CMS simulation: development of track reconstruction for L1 trigger application at the CMS detector at CERN, ii) ATLAS simulation: Development of the pattern recognition for the ATLAS L1Track Trigger application at CERN, iii) Reconstruction of salient and moving visual features, iv) Plasma tomography image reconstruction: extraction of salient visual features in nuclear fusion plasma experiments.

WP5 aims at establishing the conceptualisation for the integration of much larger banks inside the AMMA-chip by i) optimising the 2D design to occupy the maximum die size allowed by the package, keeping the power consumption at the minimum level to be able to package two AM chips one over the other (2.5 D), ii) develop a concept with a cutting-edge technological solution for the 3-Dimensional (3D) AMMA-chip. The idea behind this 3D integrated Circuit (IC) design development is to mount two or more 2-D dices on top of each other, and interconnect them by using Through Silicon Vias (TSVs) vertically, like the VIPRAM concept. This will give huge advantages when it comes to performance, functionality, and form factor.

ii) Gantt chart

WP	Type	Tasks
WP1	**MGT**	**Project management and coordination**
1.1	MGT	Project Coordination
1.2	MGT	Project Management
WP2	**RTD**	**ASICs Development**
2.1	RTD	Full custom design/floorplanning of custom cell for the 2D AM & cell simulation
2.2	RTD	Standard cell design of 2D AM and cell simulation
2.3	RTD	Integration of full custom & standard cell design, placement & routing, global simulation & tape-out
2.4	RTD	Test of prototypes
2.5	RTD	2D Multipackaging: 2 AMMA-chips on the same plan
2.6	RTD	Concept of test and Translation of test vectors
2.7	RTD	Test SW development, test debug, test of samples
WP3	**RTD**	**Board Development**
3.1	RTD	Firmware and software development for the embedded system
3.2	RTD	Acquisition & commissioning of embedded systems for demonstration
3.3	RTD	LAMB design and development
3.4	RTD	LAMB assembly and first quality test of boards
3.5	RTD	Single AMMA-chip mezzanine for AMMA-chip tests design and test vector design
3.6	RTD	Firmware for array of AMMA-chip tests and LAMB tests
3.7	RTD	Plasma Tomography connection to the image processing device: the readout system.
3.8	RTD	Loadboard Design for Microtest tester
WP 4	**DEM**	**Test Bench Applications Demonstrations**
4.1	DEM	CMS simulation
4.2	DEM	ATLAS simulation
4.3	DEM	Reconstruction of salient and moving visual features
4.4	DEM	Plasma Tomography image reconstruction
WP5	**RTD**	**Design for further integration**
5.1	RTD	Logic Integration, placement & routing, global simulation for a maximum die compatible with the package
5.2	RTD	2.5D Multipackaging: one AMMA-chip over the other
5.3	RTD	Towards a 3D AMA-chip: evaluation of floorplan and conceptual integration
WP6	**MGT**	**Dissemination and exploitation**
6.1	MGT	Dissemination
6.2	MGT	Exploitation
6.3	MGT	Project Exit Plan



Selection of the most indicative steps and deliveralbles
Please see table 1.3b and 1.3c for the complete sets of deliverables and milestones.

Table 1.3a: Template - Work package list

Work package list

Work package No[32]	Work package title	Type of activity[33]	Lead partic no.[34]	Lead partic. short name	Person-months [35]	Start month[36]	End month[36]
1	**Management and coordination**	MGT	1	INFN	22	1	36
2	**ASICs Development**	RTD	2	CNRS	53	1	17
3	**Board development**	RTD	4	AUTH	90.5	1	21
4	**Test Bench Applications Demonstrations**	DEM	6	UNIFI	143	1	36
5	**Design for further integration**	RTD	8	UHEI	42	1	36
6	**Dissemination and exploitation**	MGT	7	PRIELE	37.5	1	36
	TOTAL				388		

32 Workpackage number: WP 1 – WP n.

33 Please indicate one activity (main or only activity) per work package:
RTD = Research and technological development; DEM = Demonstration; MGT = Management of the consortium

34 Number of the participant leading the work in this work package.

35 The total number of person-months allocated to each work package.

36 Measured in months from the project start date (month 1).

Table 1.3b: Template - Deliverables List

List of Deliverables

Del. no. [37]	Deliverable name	WP no.	Nature[38]	Dissemination level [39]	Delivery date[40] (proj. month)
D1.1	Operational Project Management Plan and establishment of Project Governing bodies	1	R	CO	M1
D1.2	Interim reports to the European Commission	1	R	CO	M18 and M36
D1.3	Final report to the European Commission	1	R	CO	M36
D1.4	Brief internal progress reports	1	R	CO	(Yearly)
D1.5	Minutes of Management Board / full consortium meetings	1	R	CO	Every 6 months
D1.6	Minutes of Technology Advisory Group meetings	1	R	CO	Yearly
D2.1	Publication of the fully characterized full custom AM cell	2	O	RE	M5
D2.2	AMMA-chip interface specification and operation manual	2	R	RE	M4
D2.3	First AMMA-chip prototypes tape-out	2	O	RE	M6
D2.4	500 AMMA-chip for demonstrators tape-out	2	O	RE	M12
D2.5	Publication of the prototype test results	2	R	PU	M13
D2.6	AMMA-chip package ready for two interconnected AMMA-chip cores	2	P	RE	M9
D2.7	Translated test vectors	2	O	RE	M15
D2.8	500 multi-packaged AMMA-chips for demonstrators tape-out	2	P	RE	M17
D3.1.1	Release firmware and software of the computing unit	3	P	RE	M16
D3.2.1	All computing units commissioned, tested and delivered to partners	3	P	RE	M21
D3.2.2	Scientific papers or a communication at an international conference	3	O	PU	M24
D3.3.1	Release of LAMB PCB	3	P	RE	M10
D3.4.1	Assembled and tested LAMBs prototypes	3	P	RE	M12
D3.4.2	Assembled and tested LAMBs	3	P	RE	M19

37 Deliverable numbers in order of delivery dates. Please use the numbering convention <WP number>.<number of deliverable within that WP>. For example, deliverable 4.2 would be the second deliverable from work package 4.

38 Please indicate the nature of the deliverable using one of the following codes:
R = Report, **P** = Prototype, **D** = Demonstrator, **O** = Other

39 Please indicate the dissemination level using one of the following codes:
PU = Public
PP = Restricted to other programme participants (including the Commission Services).
RE = Restricted to a group specified by the consortium (including the Commission Services).
CO = Confidential, only for members of the consortium (including the Commission Services).

40 Measured in months from the project start date (month 1).

D3.5.1	Release the single-AMMA-chip mezzanine boards	3	P	RE	M6
D3.6.1	Release the test-setup for the LAMBs	3	P	RE	M14
D3.7.1	Readout system ready for the Plasma Tomography demonstrator	3	P	RE	M18
D3.8.1	LoadBoard ready for the testing of the 500 AMMA-chips in the Microtest machine	3	P	RE	M15
D3.9.1	Paper and conference presentations describing the performance of the prototypes	3	O	PU	M24
D 4.1.1	Design of an AM bank suitable for L1 trigger application	4	O	RE	M24
D 4.1.2	Results on performance of the AM based system to provide tracks for L1 trigger	4	R	RE	M36
D4.2.1.1	Release of pattern bank for ATLAS L1Track application	4	O	RE	M24
D 4.2.1.2	Paper and conference presentations describing the performance of the released pattern bank for the ATLAS L1Track application	4	R	PU	M30
D 4.2.2.1	Release of the software infrastructure for running the ATLAS simulation, including L1Track, on a PC equipped with the AM board	4	O	RE	M36
D 4.2.2.2	Paper and conference presentations describing the results of task 4.2.	4	O	PU	M36
D 4.3.1	Public reports of results about salient visual patterns (at least twice a year)	4	R	PU	M24
D 4.3.2	Public reports of performances of the AM based system in extracting rapidly moving and salient visual features	4	R	PU	M36
D 4.4.1	Publication for the Plasma Tomography application with AM board and ATCA AMC Digitizer	4	O	PU	M36
D 5.1	AMMA-chip06 (64 kpatterns) design ready satisfying timing and consumptions constraints.	5	O	RE	M36
D 5.2	Feasibility study for two AMMA-chip06 packaged one over the other (2.5 D) ready.	5	R	RE	M36
D5.3	3D design performance comparison and evaluation of the complexity using a VIPRAM like architecture with AMMA-chip06 ready in forms of presentation to a conference or publication of results.	5	O	PU	M36
D6.1.1	Dissemination plan	6	R	CO	M3
D6.1.2	Project leaflets	6	O	PU	M5
D6.1.3.	Project newsletters and posters	6	O	PU	(first one M2 with 2 months periodicity)
D6.1.4	Project webinars/workshops	6	O	RE	M17, M22 and M32
D6.2.1.	Market Analysis, Competition	6	R	CO	M6 initial draft with 6 months periodicity
D6.2.2.	Exploitation Plan	6	R	CO	M7 initial draft with 6 months periodicity
D6.3	Project Exit Plan	6	R	CO	M36

Table 1.3c Template - List of milestones

List of Milestones

Milestone number	Milestone name	Work package(s) involved	Expected date	Means of verification
M1.1.	Project kick-off meeting	1	M1	Minutes of kick-off meeting
M2.1	Choice of full-custom technique and design constraints of AM block defined	2	M2	D2.1 and D2.2
M2.2	AMMA-chip functions completed in RTL code with satisfactory simulated performances	2	M2	D2.1 and D2.2
M2.3	Complete satisfactory simulation of the integrated full custom/standard cells AMMA-chip and defined layout	2	M4	D2.3
M2.4	AMMA-yield and power consumption measurements at maximum speed and standard operating conditions	2	M12	D2.3 and D2.4
M2.5	Interconnection strategy choice for packaging two AMMA-chip cores	2	M2	D2.5
M2.6	Substrate design detailed simulation results	2	M6	D2.3
M2.7	Translated test vector structure defined	2	M6	D 2.7
M2.8	Loadboard availability	2	M11	D2.7
M2.9	Test program ready for testing	2	M16	D2.7 and D2.8
M3.1.1	Performance measurement of a computing unit based on single-AMMA-chip mezzanine	3	M12	D3.1.1 and D3.2.1
M3.1.2	Performance measurement of the first available LAMB-based computing unit	3	M16	D3.1.1
M3.2.1	Commissioning of computing units done	3	M20	D3.2.1
M3.3.1	LAMB design ready	3	M8	D3.3.1
M3.4.1	LAMBs assembled	3	M18	D3.4.1 and D3.4.2
M3.5.1	Single-AMMA-chip mezzanine board designed and PCB submitted	3	M5	D3.5.1
M3.6.1	LAMB test procedure and test vectors defined	3	M13	D3.6.1
M3.7.1	CAEN digitizer piggy back on ATCA AMC carrier test passed		M12	D3.7.1
M3.7.2	ATCA AMC Digitizer firmware ready	3	M17	D3.7.1
M3.8.1	LoadBoard for the Microtest tester of 500 AMMA-chips designed	3	M13	D3.8.1
M 4.1.1	L1Trigger sector dimensioning based on minimum track pT	4	M18	D4.1.1
M 4.1.2	Implementation of L1 trigger test bench system for using AM boards	4	M32	D4.1.2
M 4.2.1	Specification/optimization of the pattern banks to be loaded to the AM chip	4	M18	D4.2.1.1 and D4.2.1.2 and D4.2.2.1
M 4.2.2	Commissioning of the testbed to use the new AM chip and AM board for the L1Track application	4	M32	D4.2.2.2
M 4.3.1	Extraction of salient visual features and motion patterns used for rapid reconstruction of natural images and movies	4	M18	D4.3.1
M 4.3.2	Realization of an AM based system able to perform rapid reconstruction of salient visual features (patterns) with performances similar to humans.	4	M32	D4.3.2
M 4.4.1	Software & firmware for Plasma Tomography application ready	4	M36	D4.4.1

M 5.1	Performance comparison between the AMMA-chip06 multipackaged solution and a 3D design to choose the best technology for future implementations.	5	M36	D5.1, D5.2 and 5.3
M6.1	Dissemination Plan	6	M3	D6.1.1
M6.2	Exploitation Plan	6	M7 initial version, M36 final version	D6.2.2
M6.3	Exit Plan	6	M36	D6.3

Table 1.3d: Template - Work package description

Work package description

Work package number	1	**Start date or starting event:**									M1
Work package title	**Management and coordination**										
Activity type[41]	MGT										
Participant number	1	2	3	4	5	6	7	8	9	10	11	12
Participant short name	**INFN**	CNRS	Microtest	AUTH	UNIGE	UNIFI	PRIELE	UHEI	IMEC	CAEN	UCL	IST ID
Person-months per participant	**14**	1	0.5	1	0.5	1	1	1	0.5	0.5	0.5	0.5

Objectives

The overall objective of this work package is to provide effective management and control of the project. The management structure, techniques and procedures that will be applied will ensure the following:

- The research project is carried out according to the time schedule and budget established;
- The project objectives are achieved efficiently;
- An effective co-ordinated structure that is handling the legal, contractual, financial and administrative management of the project is created and maintained.
- The establishment of communication and reporting protocols within the consortium and between the consortium and the commission;
- A system to provide a continuous evaluation feedback and a constant project monitoring is created;

The project is managed according to the contract between the Project Consortium and the EC, and a continuous link with the EC is maintained.

Description of work

Task 1.1 Project Coordination

Task 1.1.1 – Relationship with the Commission

Dr. Paola Giannetti will be the **Project Manager (PM)** of the NEURONS project. She will be the formal contact for communication with the commission, its officers and agents. Formal communication will be through periodic management, activity and financial reports (required by the contract terms).

Task 1.1.2 – Project Reporting

The PM will be responsible for the Project Management Reports and for setting up and updating communication channels and information related to the project and the participants. A system of internal reporting will be set up to compliment the mandatory reports to the Commission. These will ensure that all partners are kept up to date with progress on tasks and are provided with information to facilitate delivery of the project plan. To support management reporting and communication, a secure web platform will be implemented to house project documentation that can be accessed by all consortium partners. Consortium

[41] Please indicate one activity (main or only activity) per work package:
RTD = Research and technological development; DEM = Demonstration; MGT = Management of the consortium.

partners will be required to contribute to each of these reports according to an agreed format. The PM will coordinate input from consortium members to prepare and submit reports as per EC reporting requirements and facilitate implementation of recommendations from the EC reviewers.
Partners: INFN (leader); participants: WP leaders.

Task 1.2 Project Management

Task 1.2.1 Implementation of Project Governance
A **Management Board (MB)** and a **Technology Advisory Board (TAB)** will be formally appointed at the start of the project. The PM will set up, coordinate and facilitate the activities of the MB and the TAB. The MB will be composed of one representative of each partner. The MB will be the decision making body of the consortium and will meet at least two times a year and hold ad hoc meetings if necessary. The MB will handle legal and IPR issues and will be responsible for setting up the consortium agreement. The TAB will consist of senior executives from stakeholder organizations and will meet at least three times across the project duration. The TAB will provide guidance on strategic directions.

Task 1.2.2 – Review progress against deliverables and milestones
Regular formal reviews of project progress against its deliverables and milestones will be facilitated. The MB will be responsible for undertaking this review and will initiate any corrective action required to ensure the project remains on course. The PM will communicate any significant changes to planned activity and make formal requests for changes to the Commission for approval as required. In addition to management board meetings, the PM will hold monthly telecons with the work package leaders. The WP leaders (WPL) will form the **Steering Committee (SC)** that is in charge of the operational management and technological steering of the project. WPL will perform Management and Coordination activities of their respective WPs and will report to the PM.

Task 1.2.3 – Day-to-day management of the project
The PM will handle project correspondence and day-to-day requests from partners and external bodies. The PM will organize, prepare and execute project management meetings and ensure effective follow-up through preparation of minutes and coordinating delivery of actions. Set up and manage the relationship with the TAB and the MB. He will implement and maintain project infrastructure – e.g. platform for information exchange, contact lists, etc. The PM will be charged to distribute the received EC funding (pre-financing, interim and final payments) to the partners. The PM will be supported by the financial and administrative departments of INFN.
Partners: INFN (leader) Participants: All partners.

Deliverables
D1.1 – Operational Project Management Plan and establishment of Project Governing bodies (M1)
D1.2 – Interim reports to the European Commission (M18 and M36)
D1.3 – Final report to the European Commission (M36)
D1.4 – Brief internal progress reports (Yearly)
D1.5 – Minutes of Management Board / full consortium meetings (Every 6 months)
D1.6 – Minutes of Technology Advisory board meetings (Yearly)

Milestones
M1.1 Project kick-off meeting (M1)

Work package number	2	**Start date or starting event:**									M1
Work package title	**ASICs Development**										
Activity type[42]	RTD										
Participant number	1	2	3	4	5	6	7	8	9	10	11	12
Participant short name	INFN	**CNRS**	Microtest	AUTH	UNIGE	UNIFI	PRIELE	UHEI	IMEC	CAEN	UCL	IST ID
Person-months per participant	11	**11**	27	0	0	0	0	0	4	0	0	0

Objectives

Development of AMMA-chip ASICs implementing the Associative Memory function and matching the required specifications; tests of the prototypes to verify the correct functionality and compliance to specifications; development of advanced packaging solution for 2D multi-die package of AMMA-chip cores; test vector data preparation and automated testing of AMMA-chips for the demonstrator.

Description of work

Task 2.1 Full custom design and floorplanning of a custom cell for the 2D AM and cell simulation

Full custom design of the Associative Memory basic cell will be explored comparing different techniques and simulated. The choice of the technique used in the final design will be based on simulation results and floorplanning considerations. The resulting full custom block made of 64x8 AM cells will be fully characterized; models will be provided for Task 2.2 and Task 2.3. The results of the full custom block design and the chosen technique will be the topic of a scientific paper or a communication at an international conference.

Partners: INFN-LNF (leader), partner INFN-Pisa, INFN-Milan.

Task 2.2 Standard cell design of 2D AM and simulation

Development of the RTL code of the AMMA-chip in parallel with a C++ register-level model of its functionality.

A C++ test-vector generation program will be developed and used to finalize and verify each function of the AMMA-chip. The functions and operations modalities will be decided in agreement with the consortium partners. The RTL code will be synthetized using a standard cells library and simulated with the realistic full-custom block model from Task 2.1. Once all functions and operation modes are finalized and tested a detailed manual will be produced.

Partners: CNRS (leader), partner INFN.

Task 2.3 Integration of full custom and standard cell design, placement & routing, global simulation and tape-out

Development of global placement and routing strategy. Back-end implementation of the AMMA-chip integrating full custom block from Task 2.1 and standard cell logic from Task 2.2. The result will be simulated in detail to verify the functionality and compliance with the desired power consumption and speed. The resulting design will be sent for tape-out on TSMC 65 nm MPW through Europractice and will result in an AMMA-chip prototype (naked dies). First 100 prototypes will be packaged in Task 2.5. Further 500 prototypes (naked dies) will be produced with extra wafers from the MPW masks for demonstrator activities and packaged in Task 2.5, after the first lot will be tested in Task 2.4.

Partners: CNRS (leader), partner INFN, IMEC.

Task 2.4 Test of prototypes

The first prototypes from Task 2.3 will be tested at INFN and LPNHE to verify the AMMA-chip functionality and prepare final set of test vectors for task 2.6. The chips will be tested for power consumption at various speed, temperature and power conditions. We will verify that the prototype is compliant with the specifications and that the simulations from Task 2.3 were correctly

[42] Please indicate one activity (main or only activity) per work package:
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predicting the characteristic of the prototype. The results will be the subject of a scientific paper or a communication at an international conference.
Partners: INFN (leader), partner CNRS

Task 2.5 2D Multipackaging
Study of packaging solution in coordination with Task 2.3 results. Development of substrate for 2D multidie packaging. Detailed simulation of substrate to validate required performances. Package tooling. Assembly of the first 100 prototypes and the further 500 devices coming from the TSMC 65 nm MPW.
Partners: IMEC (leader), partner INFN

Task 2.6 Concept of test and Translation of test vectors
Analysis and organization of massive, fast, chip tests at the Microtest machines. Test definition. Test vectors translation from C++ produced vectors of Task 2.2, after their verification at task 2.4, to a format suitable for large scale automated testing.
Partners: Microtest (leader), partner INFN

Task 2.7 Test SW development, test debug, test of samples
Software development. Commissioning and debug of the HW setup including the Loadboard developed in WP3. The prototypes from Task 2.3 will be used for electrical debug and characterization. Quality check, repeatability spike analysis and endurance. Characterization and Cpk report development. Final documentation. Test of 500 prototypes will be executed to provide good chips for the demonstrators.
Partners: Microtest (leader), partner INFN

Deliverables
D 2.1 – Publication of the fully characterized full custom AM cell (M05)
D 2.2 – AMMA-chip interface specification and operation manual (M04)
D 2.3 – First AMMA-chip prototypes tape-out (M06)
D 2.4 – 500 AMMA-chips for demonstrators tape-out (M12)
D 2.5 – Publication of the prototype test results (M13)
D 2.6 – AMMA-chip package ready for two interconnected AMMA-chip cores (M09)
D2.7 – Translated test vectors (M15)
D 2.8 – 500 multi-packaged AMMA-chips for demonstrators tape-out (M17)

Milestones
M2.1 Choice of full-custom technique and design constraints of AM block defined (M02)
M2.2 AMMA-chip functions completed in RTL code with satisfactory simulated performances (M02)
M2.3 Complete satisfactory simulation of the integrated full custom/standard cells AMMA-chip and defined layout (M04)
M2.4 AMMA-chip yield and power consumption measurements at maximum speed and standard operating conditions (M12)
M2.5 Interconnection strategy choice for packaging two AMMA-chip cores (M02)
M2.6 Substrate design detailed simulation results (M06)
M2.7 Translated test vectors structure defined (M06)
M2.8 Loadboard availability (M11)
M2.9 Test program ready for testing (M16)

Work package number	3	**Start date or starting event:**									M1
Work package title	Board Development										
Activity type[43]	RTD										
Participant number	1	2	3	4	5	6	7	8	9	10	11	12
Participant short name	INFN	CNRS	Microtest	**AUTH**	UNIGE	UNIFI	PRIELE	UHEI	IMEC	CAEN	UCL	IST ID
Person-months per participant	14	0	3	**15**	10	0	26.5	0	0	4	0	18

Objectives

This work package prepares the boards (with the accompanying firmware) which are needed in other work packages. The main objective is to build "the computing unit", which is composed by i) a control board (commercial evaluation board with a fast FPGA), ii) connected with custom-made boards hosting Associative Memory (AM) chips provided by WP2. In this synergy, the AMMA-chips reduce very fast the amount of data (keeping the important features via pattern matching) which are subsequently handled by the FPGA. Thus, we'll build a computing unit able to solve problems requiring high computing power in little time. The success of this work package is imperative for WP4, were specific algorithms will be implemented for each demonstration application. The computing unit, which is the main product of this work package, will be described to the scientific community and industry via dissemination actions.

The necessary boards to build the computing unit will either be purchased from the market (evaluation boards with a powerful FPGA with embedded CPU and large-on board memory), or be designed and built by the partners (the "Little Associative Memory Boards" - LAMBs - to host the AM chips). We'll learn to use the computing unit, commission it with the necessary firmware to do I/O towards standard PCs and all
basic functionality for controlling, configuring and managing the unit, and, finally, provide one computing unit to each partner with the common functionality needed in order to operate it and be able to develop the demonstration applications of WP4.

Apart from the construction of the computing unit and delivery to the partners, there are two additional objectives in this work package. One arises from the need to test the final AM chips before putting them on the final LAMBs; two types of mezzanine boards will be developed, able to host a single AM chip each, on a ZIF socket so that the AMMA-chip can be plugged and un-plugged as needed. The first mezzanine will be built by INFN-Milano to produce a slow setup which will become available at INFN and CNRS to develop the AMMA-chip test, define and tune the test vectors (in WP2). The second board will be produced by Microtest to be able to load and execute the test vectors on their very fast test machine; this is also needed in WP2, at the testing phase of the 500 AMMA-chips. The other objective is to provide an ATCA based readout system for plasma tomography application. This readout system will be based on IST-ID carrier cards and CAEN digitizers and will be installed, tested and connected to our demonstrator.

Description of work

Task 3.1 Firmware and software development for the embedded system

Development of the firmware and software for the control board: i) for the communication of this board (having a powerful FPGA with embedded CPU and large on-bard memory) to the other devices (i.e., to a simple PC, via the PCI or the ethernet, and to the board which hosts the AM chips – the LAMB and the mezzanine board from Tasks 3.4 and 3.5, respectively); ii) for

[43] Please indicate one activity (main or only activity) per work package:
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distributing and collecting information to/from the AMMA-chips of the LAMB/mezzanine boards; iii) for configuring and controlling the pattern banks on the AMMA-chips; and iv) to provide functionality to complete the AMMA-chip function (pattern matching) in real time. For this task, the current know-how and high performing prototypes that already exist for the ATLAS detector at CERN will be exploited. First, development will proceed with a soft-core processor and an existing big AM board from ATLAS. Then, the FPGA board will be coupled with a mezzanine board (provided by Task 3.5) hosting an existing AM chip; since the mezzanine will couple to the FPGA evaluation board in exactly the same way as the final LAMB, most of the development will be done with this setup. Finally, the firmware and software will be used and adopted to the integrated system ("the computing unit") of an FPGA board with one final LAMB provided by Task 3.4.
Partners: AUTH (leader), PRIELE (partner)

Task 3.2 Acquisition and commissioning of embedded systems for demonstration
Acquisition, at the start of the project, of the control boards (evaluation boards with fast FPGA with embedded CPU and large on-board memory, Xilinx type) to be able to host one LAMB each. When the LAMBs are ready (from Task 3.4), commission all computing units (integrate FPGA control boards with LAMBs) with the firmware and software developed in Task 3.1 and deliver functioning products to all partners of the project, so that all partners have the same hardware with the same basic firmware and thus, have the same platform to develop the demonstration prototypes of WP4.
Partners: AUTH (leader) PRIELE (partner)

Task 3.3 LAMB design and development.
Design and develop the LAMB which will host the AM chips. This board has to be able to be plugged on the FPGA control board in order to provide the computing unit with the data-reduction capabilities of the AM chips. Industrial partner PRIELE will support UNIGE at the design phase of the LAMB Printed Circuit Board to consider production requirements and specifications imposed by international standards. The boards will be handed to Task 3.4 for integration with the AM chips.
Partners: UNIGE (leader), PRIELE (partner)

Task 3.4 LAMB assembly and first quality test of boards
The LAMBs developed in Task 3.3 by UNIGE will be assembled in the industrial partner PRIELE following all production standards and specifications under the strict ISO procedures. They will be then tested following the already specified test procedure and vectors provided by Task 3.6. The AM chips from WP2 have to be ready for this task. The assembled and tested LAMBs are then to be delivered to Task 3.2.
Partners: PRIELE (leader), UNIGE (partner)

Task 3.5 Single-AMMA-chip mezzanines for AMMA-chip tests design and test vector design
Build a mezzanine board to host an AMMA-chip on a ZIF socket, able to be plugged-in and unplugged on the mezzanine. This will be used to test the first AMMA-chip prototypes, to define the test vectors and test procedures (in WP2.3 and WP2.4), which will be later translated in the Microtest format (Task 3.8) for a very fast execution of the 500 AMMA-chip tests in WP2. This board will also, as a secondary task, allow the firmware and software development on the FPGA control board to go on in the other tasks (3.1), with the AMMA-chip on the mezzanine, before the final LAMB arrives.
Partners: INFN-Milano

Task 3.6 Firmware for array of AMMA-chip tests and LAMB tests.
Develop the tests that the AMMA-chips and the LAMB are functioning properly. The test procedure will be defined and the test vectors will be provided to the partners of Tasks 3.4 and 3.8.
Partners: INFN-Pavia

Task 3.7 Plasma Tomography connection to the image processing device: the readout system.
Prepare the readout system which will connect the image processing computing unit to the Plasma Tomography. This is an ATCA based demonstrator/system for tomography applications leveraging IST-ID carrier cards and CAEN digitizers. IST-ID will use an existing AMC module (1) together with the existing ATCA-AMC board (2) and the CAEN Digitizer piggyback board (3) to prepare the readout system for the Plasma Tomography demonstrator of WP4. IST-ID will develop special FPGA firmware for (1) and (2). CAEN will develop a special firmware for (3).
Partners: IST-ID (leader), partner CAEN

Task 3.8 Loadboard design for Microtest tester
Design and test of the small interface board between the AMMA-chip and the Microtest machine that will execute the tests of the 500 AM chips in WP2.
Partners: Microtest

Deliverables
D3.1.1- Release* firmware and software of the computing unit (M16)
D3.2.1 - All computing units commissioned, tested and delivered to partners (M21)
D3.2.2 - Scientific paper or a communication at an international conference (M24)
D3.3.1 - Release of LAMB PCB (M10)
D3.4.1 - Assembled and tested LAMBs prototypes (M12)
D3.4.2 - Assembled and tested LAMBs (M19)
D3.5.1 - Release the single-AMMA-chip mezzanine boards (M6)
D3.6.1 - Release the test-setup for the LAMBs (M14)
D3.7.1 - Readout system ready for the Plasma Tomography demonstrator (M18)
D3.8.1 - LoadBoard ready for the testing of the 500 AMMA-chips in the Microtest machine (M15)
* For the release of a product/result we consider any form of written report (note, paper or communication to a conference)

Milestones
M3.1.1 Performance measurement of a computing unit based on single-AMMA-chip mezzanine (M12)
M3.1.2 Performance measurement of the first available LAMB-based computing unit (M16)
M3.2.1 Commissioning of computing units done (M20)
M3.3.1 LAMB design ready (M 8)
M3.4.1 LAMBs assembled (M 18)
M3.5.1 Single-AMMA-chip mezzanine board designed (M 5)
M3.6.1 LAMB test procedure and test vectors defined (M 13)
M3.7.1 CAEN digitizer piggy back on ATCA AMC carrier test passed (M12)
M3.7.2 ATCA AMC Digitizer firmware ready (M17)
M3.8.1 Load board for the Microtest tester of 500 AMMA-chips designed (M13)

Work package number	4	**Start date or starting event:**									M1
Work package title	Test Bench Applications Demonstrations										
Activity Type	DEM										
Participant number	1	2	3	4	5	6	7	8	9	10	11	12
Participant short name	INFN	CNRS	Microtest	AUTH	UNIGE	**UNIFI**	PRIELE	UHEI	IMEC	CAEN	UCL	IST ID
Person-months per participant	21	0	0	15	0	**38**	9	0	0	6	34	20

Objectives

Test and verify potentialities of this computing unit in different scientific applications requiring fast data processing:

a. level 1 (L1) trigger based on tracking for the HEP CMS experiment
b. level 1 (L1) trigger based on tracking for the HEP ATLAS experiment
c. rapid salient visual features analysis for understanding the brain computation
d. rapid salient visual features analysis for plasma tomography

Description of work

Task 4.1 CMS simulation
Task 4.1.1. Development of a track reconstruction based on AM suitable for L1 trigger application
Partners: INFN (leader), partner UNIFI
Task 4.1.2 Test of L1 trigger functionality using AM board prototype.
Partners: INFN (leader), UNIFI, PRIELE (partners)

Task 4.2 ATLAS Simulation
4.2.1 Development of the pattern recognition for the ATLAS L1Track Trigger application, including the specification/optimization of the pattern banks to be loaded to the AM chip
Partners: UCL(leader), AUTH, PRIELE (partners)
4.2.2 Development of a testbed to exercise the new AM chip and AM board for the L1Track application.
Partners: U0CL(leader), AUTH, PRIELE (partners)

Task 4.3 Reconstruction of salient and moving visual features
Task 4.3.1 Develop and extend the existing algorithm for extraction of salient visual patterns (features) to complex natural visual scenes containing either moving and static stimuli. This will be accomplished by performing computer simulations, implemented on conventional computers, running at low rate.
Partners: UNIFI (leader)

Task 4.3.2 Implement the simulation algorithms for fast visual motion and salient features reconstruction on the new Associative Memory based system and perform tests with natural images and movies to extract rapidly salient information ("primal sketch")
Partners: UNIFI (leader), PRIELE, AUTH (partners)

Task 4.4 Plasma Tomography image reconstruction
IST-ID will develop the firmware for the AM board to extend the existing algorithm for extraction of salient visual patterns (features) to nuclear fusion plasma experiment. Subsequently, the necessary software to manage the whole system (readout system and image processing unit connected together) will be developed by IST-ID with the contribution of CAEN.

A set of relevant patterns using tomography images previously taken will be used for the training of the AM.
This software, used together with the AM board and the ATCA AMC Digitizer, will give the opportunity to explore the advantages of an AM pattern based system for real-time control in nuclear fusion plasma experiments.
Partners: IST-ID (leader), CAEN (partner)

Deliverables
D 4.1.1 - Design of an AM bank suitable for L1 trigger application (M24)
D 4.1.2 - Results on performance of the AM based system to provide tracks for L1 trigger (M36)
D 4.2.1.1 - Release of pattern bank for ATLAS L1Track application (M24)
D 4.2.1.2 - Paper and conference presentations describing the performance of the released pattern bank for the ATLAS L1Track application (M30)
D 4.2.2.1 - Release of the software infrastructure for running the ATLAS simulation, including L1Track, on a PC equipped with the AM board (M36)
D 4.2.2.2 - Paper and conference presentations describing the results of task 4.2 (M36)
D 4.3.1 - Public reports of results about salient visual patterns (at least twice a year) (M24).
D 4.3.2 - Public reports of performances of the AM based system in extracting rapidly moving and salient visual features (M36)
D 4.4.1 - Publication for the Plasma Tomography application with AM board and ATCA AMC Digitizer (M36)

Milestones
M 4.1.1 L1 Trigger sector dimensioning based on minimum track pT (M18)
M 4.1.2 Implementation of L1 trigger test bench system for using AM boards (M32)
M 4.2.1 Specification/optimization of the pattern banks to be loaded to the AM chip (M18)
M 4.2.2 Commissioning of the testbed to use the new AM chip and AM board for the L1Track application (M32)
M 4.3.1 Extraction of salient visual features and motion patterns used for rapid reconstruction of natural images and movies (M18)
M 4.3.2 Realization of an AM based system able to perform rapid reconstruction of salient visual features (patterns) with performances similar to humans. (M32)
M 4.4.1 Software & firmware for Plasma Tomography application ready (M36)

Work package number	5	**Start date or starting event:**									M1
Work package title	Design for further integration										
Activity type[44]	RTD										
Participant number	1	2	3	4	5	6	7	8	9	10	11	12
Participant short name	INFN	CNRS	Microtest	AUTH	UNIGE	UNIFI	PRIELE	**UHEI**	IMEC	CAEN	UCL	IST ID
Person-months per participant	8	8	0	0	0	0	0	**20**	6	0	0	0

Objectives

The most important goal of WP5 will be the integration of much larger banks inside the AMMA-chip. This goal will be pursued working in different directions.

(a) First of all we will optimize the 2D design to occupy the maximum die size allowed by the package, keeping the power consumption at the minimum level to be able to package two AM chips one over the other (2.5 D). In this case communication between different chips is limited to contacts between peripheral pads.

(b) Nevertheless it will be extremely interesting to understand the potentiality to go for 3D. The most interesting objectives of WP5, in fact, is to develop a concept with a cutting-edge technological solution for the 3-Dimensional (3D) Associative Memory (AM) chip. The idea behind this 3D integrated Circuit (IC) design development is to mount two or more 2 D dices on top of each other, and interconnect them by using Through Silicon Vias (TSVs) vertically, like the VIPRAM concept.

The 3D AMMA-chip integration is a viable and promising option to address the well-known memory wall problem in high performance computing system as the AMMA-chip. Another benefit with this 3D concept is that it allows the integration of otherwise incompatible technologies (Heterogenous integration), this will give huge advantages when it comes to performance, functionality, and form factor.

Description of work

Task 5.1 Logic Integration, placement & routing, global simulation for a maximum die compatible with the package

This task will start after the tests of AMMA-chip in task2.4 (AMMA-chip05 version which is 32 kpatterns chip). Development of placement and routing strategy. Back-end implementation of the AMMA-chip integrating full custom block from Task 2.1 and standard cell logic for an extended chip. The result will be simulated in detail to verify the functionality and compliance with the desired power consumption and speed. Evaluation of consumption and informations needed for task 5.2

Partners: CNRS (leader), partner INFN

Task 5.2 2.5D Multipackaging

Feasibility study for packaging of two large 2D AMMA-chip (AMMA-chip06 version which is at least 64 kpatterns on a die), one over the other. Study of packaging solutions in coordination with Task 5.1 results. Detailed simulation of possible solutions to validate required performances

Partners: IMEC (leader), partner INFN

Task 5.3 Towards a 3D AMMA-chip: Evaluation of floorplan and conceptual integration

This task aims at develop a concept design with a cutting-edge technological solution for the 3D AMMA-chip.

Such integration concerns a conceptual and a technical aspect:

[44] Please indicate one activity (main or only activity) per work package:
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- the first step will be based on the development on the current AMMA-chip (WP2).

A full understanding of the AMMA-chip topology and test characteristic is mandatory as a first step toward the 3D integration.

- the second step towards the 3D AMMA-chip is to evaluate the floorplan of the AMMA-chip to eventually improve the architecture, in particular the readout speed, the power distribution and potentially avoid hotspots (thermal management). Important is also to identify and analyze the chip functionality problems and requirements. Different floorplans will be explored to exploit all the advantages of a 3D AMMA-chip implementation. The outcome will guide the further chip development to be compared with the 2D version AMMA-chip06.

This approach aims at improving the performance of the AMMA-chip06 with 3D integration.
To assure technical interoperability, WP5 includes a continuous task on definition and elaboration of development standards, starting early in the project. The work will accumulate with a scientific paper or presentation on an international conference.
Partners: UHEI (leader), partner INFN

Deliverables

D 5.1 AMMA-chip06 design ready satisfying timing and consumptions constraints. Publication of results (M36)
D5.2 Feasibility study for two AMMA-chip06 packaged one over the other (2.5 D) ready. Report about simulation of possible solutions and final choice of the best one. (M36)
D5.3 3D design performance comparison and evaluation of the complexity using a VIPRAM like architecture with AMMA-chip06 ready. Presentation to a conference or publication of results (M36).

Milestones

M 5.1 Performance comparison between the AMMA-chip06 multipackaged solution and a 3D design to choose the best technology for future implementations. (M36)

Work package number	6	**Start date or starting event:**									M 1
Work package title	**Dissemination and exploitation**										
Activity Type	MGT										
Participant number	1	2	3	4	5	6	7	8	9	10	11	12
Participant short name	INFN	CNRS	Microtest	AUTH	UNIGE	UNIFI	**PRIELE**	UHEI	IMEC	CAEN	UCL	IST ID
Person-months per participant	9	1	9.5	2	1	1	**7**	1	2	2	1	1

Objectives

Disseminate the project objectives, approaches and results. Plan full exploitation of the results and the governance of IP and access rights in collaboration with the WP1 Management and with agreement of consortium partners; facilitate collaboration and two-way information exchange between relevant stakeholders (i.e. embedded computing and high performance computing communities, medical systems, ETPs (i.e. Manufuture) and JTIs (ARTEMIS, ENIAC), European Research Infrastructures Forums, etc) from the European Research Area at large and especially amongst specifically identified target groups ensuring the provision and implementation of feedback (ICT communities). Elaborate in collaboration with the consortium members a project exit plan to ensure transfer of research results for further development and innovation steps.

Description of work

Task 6.1 Dissemination

Task 6.1.1 – Elaboration of a project dissemination plan

A full and comprehensive project dissemination plan will be developed in collaboration and agreement with the project consortium members. The plan will contemplate dissemination tools (i.e. newsletters, leaflets, posters, etc), measures (i.e. participation in conferences, fairs, etc) and other forums such as CERN detectors meetings, medical imaging workshops, data treatment symposia, etc). More specifically, some of possible dissemination actions already identified by the partners are:

- Press release, jointly with the EC, in selected well diffused media at the start of the project.
- Presentation of project results in specific conferences and trade fairs. Preparation of a project brochure (in PDF format) for electronic mailing to target audience, such as Schools and Institutes for electronic manufacturing, medical electronics, community of European Research Infrastructures, European Technology platforms such as Manufuture and/or Join Technology Initiatives such as ARTEMIS, etc.
- Publications in popular science magazines and professional and scientific journals.

All activities encompassing any transfer of knowledge outside the Consortium will be coordinated by the Exploitation Manager; however particular actions will be executed by designated partners. All partners will take an active role in discussing and deciding the content of the material to be published to ensure that initially no confidential information is disclosed which could jeopardize the project. Material will be prepared and disseminated in various forms like conference participation, exhibitions, mailing to the target audience etc. The dissemination and exploitation plan will be internally reviewed periodically to ensure adaptation to appearing needs.

Partners: INFN (leader), CNRS, MICROTEST, AUTH, UNIGE, UNIFI, PRIELE, UHEI, IMEC, CAEN, UCL, IST-ID

Task 6.1.2. – Development of dissemination materials

Elaboration of dissemination materials supporting the web-portal content. A public website will be constructed with a restricted area for access and storage of technical information by consortium partners and a public access section whereby members of the public can consult non-confidential information about the project. Furthermore, at the end of the project, the relevant information and results will be available to the public via this website. During the project lifetime the website will be updated at least every 2-3 months. The website will also have a Restricted Area. Members only area, which will act as a document platform for the exchange of live documents and the upload of materials for the exclusive use of registered members. The dissemination and exploitation manager will be responsible for the content of the website ensuring in this way that it will fully reflect the end-users dissemination needs. A newsletter in pdf form will be elaborated every two months highlighting the project most recent

achievements suitable to be communicated to the public. Also, project leaflets and posters will be developed when necessary in order to disseminate the project in relevant events and forums that the project members will participate in.
Partners: INFN (leader), CNRS, MICROTEST, AUTH, UNIGE, UNIFI, PRIELE UHEI, IMEC, CAEN, UCL, IST-ID

Task 6.1.3 Organization of targeted dissemination actions for relevant identified communities
Three project webinars/workshops will be organized targeting specific communities (in principle foreseen towards the health care community (i.e. medical imaging, medical systems) and the embedded and high performance computing communities, industrial and academic communities interested in the Big Data challenge, etc.). Depending on the monitoring of the dissemination and exploitation plan additional workshops/webinars will be organized based on potential interest of different stakeholders (i.e. communities interested in image processing in general, intelligent systems, etc.).
Partners: INFN (leader), CNRS, MICROTEST, AUTH, UNIGE, UNIFI, PRIELE UHEI, IMEC, CAEN, UCL, IST-ID

Task 6.2. Exploitation
Task 6.2.1 Market Analysis
Technology watch and market survey to learn about possible competition, latest evolutions and trends on the specific technology and its applications (already in the market or under development). This will be a continuous task in order to produce every six months an update, which will create new concepts and conclusions to be used in the Exploitation plan update. All partners should participate in this analysis by contributing with data coming from their operational environment.
Partners: PRIELE (leader), INFN, CNRS, MICROTEST, AUTH, UNIGE, UNIFI, UHEI, IMEC, CAEN, UCL, IST-ID

Task 6.2.2 Exploitation Plan
The aim of this task is to prepare the ground for further exploitation of the project results. These results and the information gathered by the partners through dissemination activities and continuous market & technology watch will be used to prepare a draft Exploitation Plan. This draft will outline a preliminary Action Plan for each partner describing their concept on the use and exploitation of the knowledge generated during the project.
Through all the dissemination activities and the planning of the Exploitation (including market and technology watch) SMEs will form a clear picture on the exploitation potential of the project results, building further and precisely upon the already foreseen schemes. Based on this knowledge, the following activities will take place:

- Market analysis of state of the art and stakeholders prone to uptake the newly developed solutions.
- Management proposition of IP modalities (i.e. IP, licenses, copyrights, etc.) and strategy pathways (i.e. out licensing, new business services, etc.).
- Definition and monitoring of exploitation Key Performance Indicators to ensure an effective dissemination strategy.

Partners: PRIELE (leader), INFN, CNRS, MICROTEST, AUTH, UNIGE, UNIFI, UHEI, IMEC, CAEN, UCL, IST-ID

Task 6.3 Project Exit Plan
A project exit plan will be developed considering the different strategies to ensure a full exploitation of the project results, tools methodologies, contacts with relevant users' communities and stakeholders (such as industrial manufacturing, medical imaging, embedded systems, etc), etc. the plan will be elaborated in co-operation and agreement with the different consortium members. The exploitation agreement will detail the agreements between the consortium members regarding exploitation issues (i.e. IP ownership). It will mainly reflect procedures for defining and handling the background knowledge and will include the conditions and process by which the consortium will grant to the end-user SME's further manufacturing and distribution, outside the consortium, to meet the demand from the EU/worldwide markets, SME's and industries. It will also cover exploitation restrictions, licensing arrangements and protection of the intellectual property generated within the project, as well as methods for disseminating results.
Partners: MICROTEST (leader), PRIELE, INFN, CNRS, AUTH, UNIGE, UNIFI, UHEI, IMEC, CAEN, UCL, IST-ID

Deliverables
D6.1.1 - Dissemination plan (M3)
D6.1.2 - Project leaflets (M5)
D6.1.3 - Project newsletters and posters (first one M2 with 3 months periodicity)
D6.1.4 - Project webinars/workshops (M17, M22, M32)
D6.2.1 - Market Analysis, Competition (M6 initial draft with 6 months periodicity)
D6.2.2 - Exploitation Plan (M7 initial draft with 6 months periodicity)
D6.3 - Project Exit Plan (M36)

Milestones
M6.1 Dissemination Plan (M3)
M6.2 Exploitation Plan (M7 initial version, M36 final version)
M6.3 Exit Plan (M36)

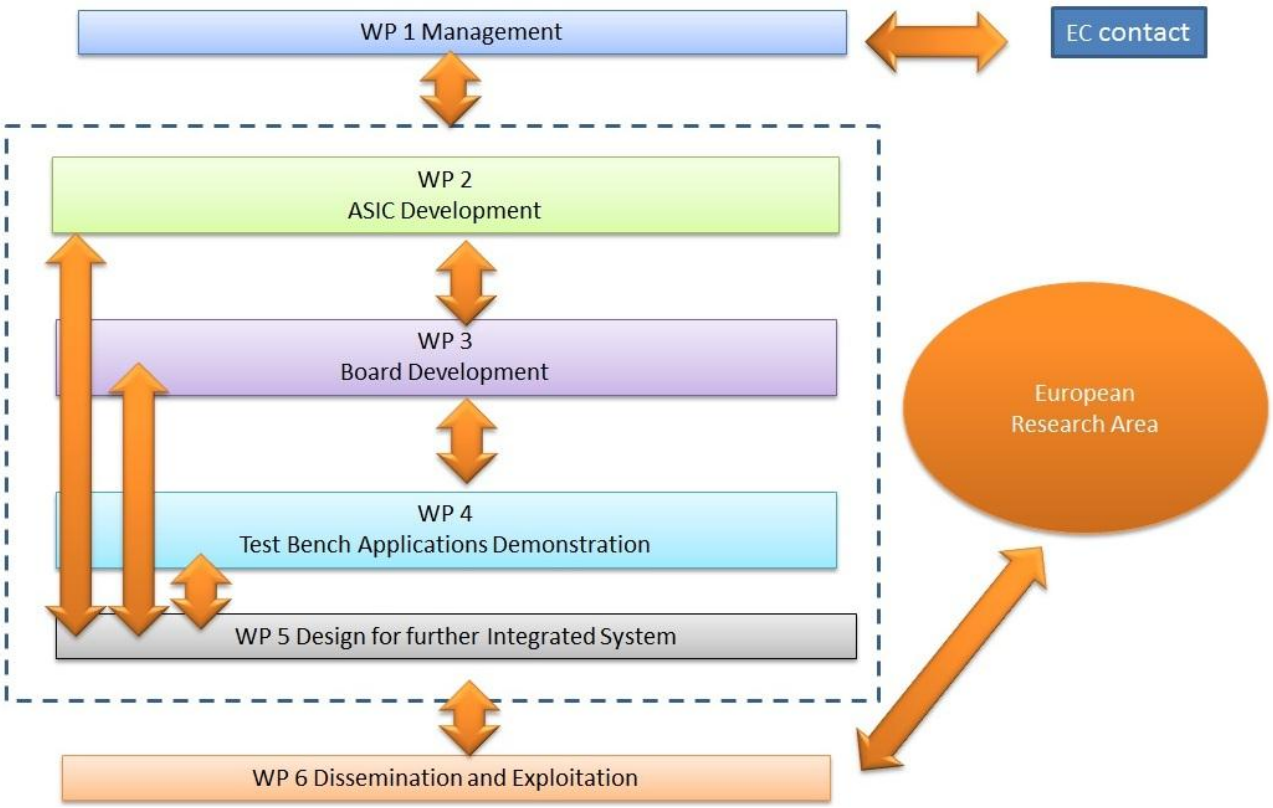
Table 1.3e Summary of effort

Summary of effort

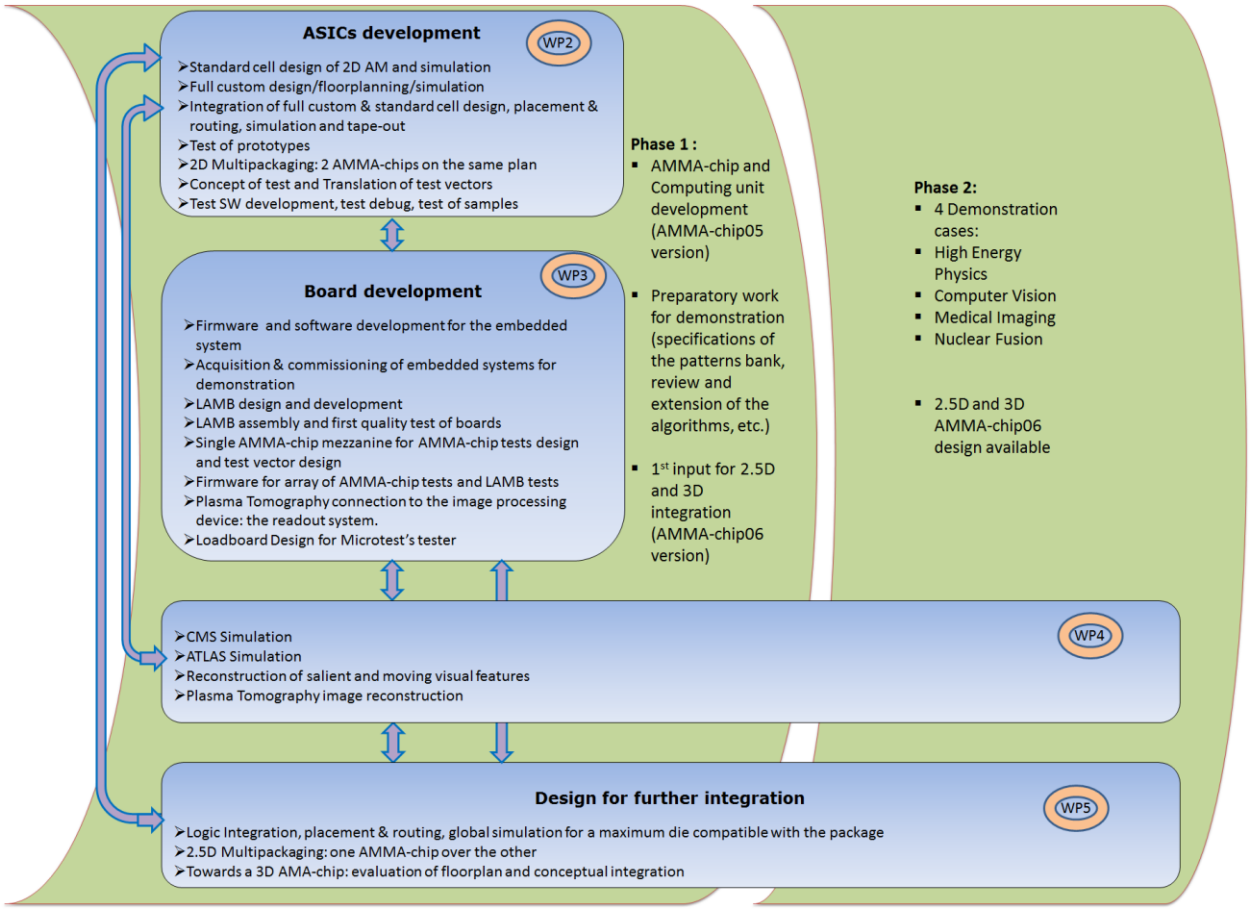
Partic. no.	Partic. short name	WP1	WP2	WP3	WP4	WP5	WP6	Total person months
1	INFN	**14**	11	14	21	8	9	**77**
2	CNRS	1	**11**	0	0	8	1	**21**
3	Microtest	0.5	27	3	0	0	9.5	**40**
4	AUTH	1	0	**15**	15	0	2	**33**
5	UNIGE	0.5	0	10	0	0	1	**11.5**
6	UNIFI	1	0	0	**38**	0	1	**40**
7	PRIELE	1	0	26.5	9	0	**7**	**43.5**
8	UHEI	1	0	0	0	**20**	1	**22**
9	IMEC	0.5	4	0	0	6	2	**12.5**
10	CAEN	0.5	0	4	6	0	2	**12.5**
11	UCL	0.5	0	0	34	0	1	**35.5**
12	IST ID	0.5	0	18	20	0	1	**39.5**
Total		**22**	**53**	**90.5**	**143**	**42**	**37.5**	**388**

iv) Pert diagram (top) and workplan structure (down) showing the research methodology

Pert Diagram



Workplan structure



v) Describe any significant risks, and associated contingency plans

The partners have large experience in working in EU projects. Therefore a concurrent research management approach has been chosen in order to ensure enough time and human resources for each work package. The already foreseeable risks have been taken into account by the project Partners in setting up the Work Plan, as shown by the work package descriptions, schedule and associated deliverables and milestones. However, unexpected risks might pop up during the project and a proactive approach which permits the minimization of their impact is essential to guarantee the full achievement of the project objectives.
The risk assessment methodology which was followed during the preparation phase of the project is based on failure modes and effects analysis (FMEA). The risks are first identified and classified by severity, likelihood of the failures and impact of the failures. The risks and potential of failure were identified based on the large experience of the partners with the development of advanced full system solutions and on common failure mechanism logic. The following table 1.3.1 presents the type of risks, probability, associated impact and related mitigation actions.

WP	Risk description	Probability[45]	Impact[46]	Proposed Contingency plans
1	Loss of a key partner from an application domain.	Low	High	Measures will be taken in the direction of assuming the workload of the partner and/or focusing of a substituting partner with similar profile.
1	Communication problems between partners and/or work packages.	Low	High	The project Steering Committee (SC) and the project Management Board (MB) will recommend and implement the necessary measures to restate a fluid communication based on analysis of the specific situations.
all	Communication problems within the work packages	Medium	High	Regular meetings (face-to-face or conference calls) for close communication
all	Delays in achieving a project milestone in time (valid for any WP)	Medium	Medium/High (depending on overall progress of project)	Setting up a periodic internal reporting and risk register to enable pro-active management of milestones EC will be duly informed and together with the SC and MB will agree upon measures to minimize the impact of the delays based on potential alternative routes.
all	Overspending of one or more partners (valid for any WP)	Low	Medium/high (depending on possibilities for shifting other resources)	Early detection via management reports and foreseen consortium periodic meetings. The situation will be analyzed by the SC and MB in order to mobilize resources capable of working more efficiently. Potential budget shifts in accordance with EC can be proposed only if absolutely necessary and always on overall project benefits avoiding detriment to other partners.
2	T2.4 Performance of the AMMA-chip (first 100 prototypes) not according to the ASIC test specification document.	Low	Medium	Depending on the severity of the non-compliance we could adapt the depending goals and/or correct the issue for the following tape-out.
2	Chip or package manufacturing has a delay.	Low	Low	Depending on the amount of delay it could be possible to absorb it in WP2 without affecting other packages. Otherwise we'll adapt the WP4/5 schedule. Production is an austere organized procedure. Delays may happen only due to not in-time delivery of materials.

[45] Probability of risk occurring
[46] Impact if risk occurs

2	Die yield is low (i.e. lower than 70%) and multi-packaging total yield will be too low (i.e. much lower than 50%)	Medium	Medium	multi-packaging will be tested only with the first 100 chips, and not used for the following 500 chips, unless test before packaging will be possible
3	Operating speed, power consumption or functionality measured on custom mezzanines not compliant with our goals	Low	Low	Understand the problem and produce a corrected version, introducing few months delay, that could be absorbed in WP3 itself, or produce a low impact on WP4.
3	Commissioning of the AMMA system has a delay.	Low	Low	We will adapt the WP4 program.
4	T4.3.2 – Demonstrator delivery delay or reduced AM bank size	Low	Medium	reconstruction of salient features in images, containing only static stimuli
4	T4.1.2 & T4.2.2 & T.4.4.1 Demonstrator I/O bottleneck	Low	Low	Communicate with WP5 to study more powerful I/O solutions for future HEP applications
5	T5.1 Operating speed, power consumption or functionality simulated for AMchip06 not compliant with expectations	Low	Low	Changes to the design will be investigated.
5	T5.3 Vipram architecture appears to be too difficult	Medium	Low	Reduce the goal to architectures that require a minor number of 3D connections
6	Early publication hinders patent application	Low	Medium	Rules concerning procedures for publishing project results will be established. Patent claims will be studied to overcome limitation.

Table 1.3.1 Type of risks, probability, associated impact and related mitigation actions.

Section 2. Implementation

2.1 Management structure and procedures

2.1.1. Organizational structure

The WP1 will be dedicated solely to the management and coordination of the NEURONS project, to ensure that the project management receives the suitable priority and attention and that the project can proceed efficiently. This WP1 will deal with all aspects of the technical and administrative management as well as the quality monitoring of the project.

To enable the efficient and professional management of the project, a clear and transparent management structure has been developed, as shown in figure 2.1.1:

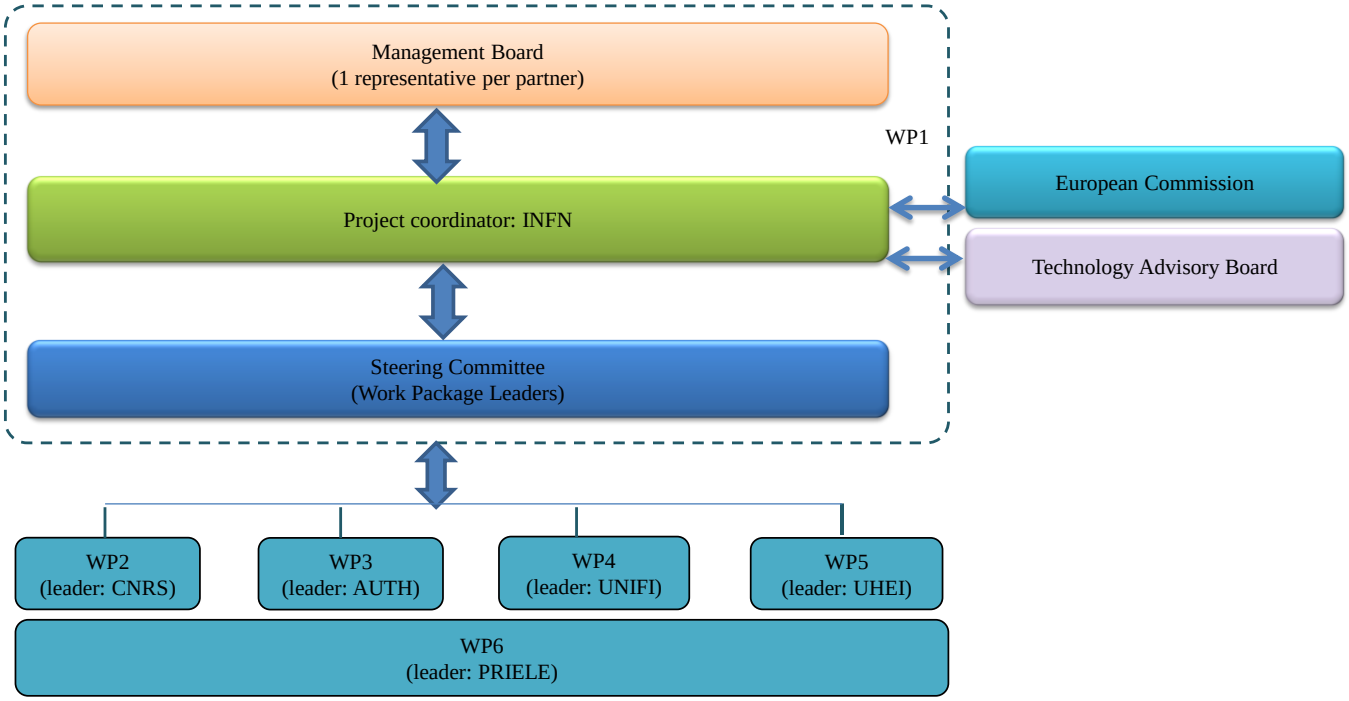


Fig. 2.1.1 Management structure

The responsibility of the project coordination will be taken by INFN, thus supplying the **Project Manager** (PM). To ensure that all partners are fully committed to adequately fulfill their responsibilities, they will each be represented by one member in the **Management Board** (MB) that will oversee the activities on a strategic level. The activities of NEURONS are divided in seven work packages, each of which has been assigned a Work Package Leader (WPL). The WPL are the members of the **Steering Committee** (SC) that is in charge of the operational management and technological steering of the project (including demonstration).

Ultimately, this structure should enable a timely fulfillment of the project objectives, by allowing clear and continuous communication among the project partners. Sufficient consultation moments (i.e. consortium meetings) between the partners are built-in at different levels (operational to strategic) to monitor the progress, to allow collectively solving problems, to react to unforeseen circumstances, and to adjust project efforts where necessary.

a. *The Management Board (MB)*

The project's MB is the **formal decision-making body** of the project. The board will have the overall responsibility of the **technical management** as well as on all the **administrative, contractual and financial issues** related to the project. It is composed of one representative from each consortium partner and is chaired by the PM. Each representative will have a sufficient level of seniority within the partner organization to take binding decisions for the organization.

The **main responsibilities** of the MB are to:

- Regularly monitor if the project remains in line with the initial objectives, and check the progress according to the set deliverables and milestones. Progress on the project will be reported to the MB by the PM who in turn consolidates input from the WPL in the SC.
- Have the authority to alter the work plan (shifts in budget, tasks, responsibilities, etc) and develop extra measures according to the established contingency plans (in case of delays etc.)
- Approve/reject changes in the consortium, the consortium agreement and the members of boards/committees.
- Define the rules for internal and external communication of knowledge and results, according to the project dissemination and exploitation plan.
- Formally review and approve every output (such as reports and deliverables) that needs to be dispatched to the EC.
- Promote the dissemination of the project, guide its execution in strategically relevant directions and maximize the uptake of the results, by establishing strategic relationships with relevant organizations outside of the project consortium such as:
    - interested stakeholders,
    - embedded system experts
    - relevant European Technology Platforms
    - the High Energy Physics (HEP) community
- Identify and solve important ethical and legal issues
- Manage and resolve conflicts and IPR-related issues. Disputes or conflicts during project execution shall be referred to the MB whose decision will be binding on all partners.

The MB will meet two times a year, either in person or through teleconferencing. The PM can decide to call additional emergency meetings if required by unforeseen project development circumstances that require urgent actions and decisions.

b. The Project Manager (PM)

The coordination and overall management of the project is with lead partner INFN and the role of PM will be performed by Dr. Paola Giannetti. She is Research Director of INFN_Department Pisa since 2002. Paola was proponent of the FTK processor for LHC experiments and was project leader of the INFN funded FTK R&D project (1999-2001). In addition, she was proponent of three trigger upgrades at CDF (2002-2008) and was responsible for INFN funds. Paola was FTK deputy project leader at ATLAS and responsible of INFN funds (2008-2012). She acted as Chair of the CMS experiment referee group in Italy (2007 and 2009), was scientist in charge of the FP6 OIF Marie Curie fellow POT and leader of the research program FP7 IOF Marie Curie fellow ITES program.

The PM is responsible for the coordination of the financial, administrative, technical and scientific activities and will safeguard and **monitor day-to-day, operational progress on the project objectives, deliverables, and milestones**. For this, he will receive regular updates on activities in the work packages from the WPL, through direct contacts and during the regular meetings of the SC. Based on the consensus in the SC meetings, the PM reports on overall project progress to the MB.
The PM will **implement strategic decisions** taken by the MB and is therefore in continuous contact with all partners involved. On this level, one-on-one meetings or ad-hoc consultations are organized in person or by teleconferencing, as the situation requires. In the unlikely event of conflicts, the PM will compromise negotiation in conjunction with the MB.

The PM will serve as the **unique contact point for the EC** (i.e. EC designated Project Officer (PO)) and will report on project status and progress on a yearly basis. At the end of the project, the PM will write a final report on deliverables for the EC, describing data, interpretations, opinions, and recommendations based on results and experiences.

In **summary**, the specific tasks of the PM are to:

- Coordinate the design and timely signing of the Consortium Agreement, and safeguard compliance with the agreement during the course of the project (supported by the EC PO).
- Coordinate the financial, administrative and contractual activities of the project, including monitoring and maintaining the financial budgets and distributing the EC contributed funding to the project partners (supported by the EC PO).
- Organize, chair, and report on the meetings of the MB and the SC and distribute the information pertaining to these meetings to all partners.
- Ensure adequate reporting to the MB (periodic progress) and act as a liaison to the EC in all verbal and written communication (e.g. final report).
- Implement clear administrative procedures and day-to-day financial administration of the project, both for internal use and external reporting obligations towards the EC.
- Maintain the coherence of the consortium through conflict mediation; larger scale conflicts will be escalated to the MB or even further to the Technology Advisory Board (TAB).
- Coordinate the organization of dissemination events to promote project results.

- Organize the internal and external project website.

c. The Steering Committee (SC)

The project's SC is composed of the WPL and has the **operational control** of the project. The SC focuses on operational aspects such as:

- Action plan for the next period (tasks, timetables, responsible, project plan)
- Exchange of information, experience, samples, tools
- Collaborative and creative problem solving for R&D and demonstration challenges

To achieve the scientific objectives of the project, the experimental, scientific and technical work has been organized into 3 RTD WPs (WP 2, 3, 5). WP4 is related to demonstration activities. All dissemination activities are grouped in WP6. The SC will monitor the technical progress in terms of deliverables, milestones and overall project objectives, by **designing and implementing collaborative RTD and demonstration actions and ensuring coherence of the different WPs**.

The SC will **meet a minimum of two times a year**, either in person or through teleconferencing, chaired by the PM. The timing of the meeting will be partially synchronized with the meetings of the MB. Additional meetings will be contemplated in case that project roadblocks are detected to ensure the proper resolution of all the bottlenecks according to the project contingency plans.

d. The Work Package Teams (WPT) and Leaders (WPL)

The WPT are composed of all people involved in a WP that are responsible for **performing the research and demonstration activities** in their work package. The work plan of the project has been divided in 6 work packages, each of which is implemented by a work package team.

Each work package is assigned a WPL, reflecting the partners' expertise and maintaining a balance between partners. The WPL:

- Take the technical control of and responsibility for the proper execution of the tasks related to their WP.
- Organize a detailed schedule of their WP, monitors the work in progress, and identifies possible risks.
- Appoint Task leaders, who are responsible for managing a Task and all work conducted by participants in this Task.
- Report to the SC and PM on the progress and possible deviations from the work plan.
- Chair the meetings among the partners participating to their WP and communicate continuously with all partners involved in their WP.
- Ensure extensive exchange of knowledge and expertise between the different WP.

PRIELE, the leader of WP6 is responsible for all exploitation activities related to NEURONS and thus additionally and with the collaboration, agreement and support of all project members will:

- Monitor the industrial exploitability of the project's outcomes.
- Develop an effective strategy for the commercialization of the project's results and produces a Business Plan.
- Support the PM in communicating and cooperating with external stakeholders, building external relationships, developing new linkages and partnerships.
- Promote the project's visibility in the international fora and events (conferences, workshop and similar)

PRIELE will be supported by INFN and Microtest that takes over the dissemination activities and the project exit plan. **Amanda Soukoulia**, Management & Production Engineer, MBA and MRes from PRIELE will act as WP6 Leader and *Exploitation Manager.* She is highly experienced in market research and marketing activities, while she has extensive involvement in project management in national and European research projects.
Chiara Meroni, research director at INFN Milano (INFN-MI) will act as *Dissemination Manager*. She is previous member of INFN National Scientific Committee and participated in FP7 project AIDA project as well as Atlas-Italia upgrade projects (2009-2012) and ATLAS-Milan INFN group (2007-2011).

e. The Technology Advisory Board (TAB)

The NEURONS project will launch a call for nomination of its TAB during M1. The TAB will be **composed of stakeholders** from different communities (e.g. high-performance computing, embedded computing, High Energy Physics, etc.), to whom the project

results may be useful and who will express their interest through an official 'Letter of Interest (LoI)". The TAB is regularly kept informed of the progress in the RTD and demonstration activities of the project by the PM. At least once a year, a representative of the TAB is therefore present at the MB meeting. The TAB has no deciding power and its main responsibility in the project is to **provide strategic input to the project**, thus safeguarding that the eventual project outcome will be appropriate and suitable for the relevant stakeholders and to enable the dissemination and early adoption of the project results. The TAB mission as well is to facilitate the contacts of the NEURONS project with the Communities at large promoting thus the transfer of useful innovative results and market uptake. It is foreseen that 3 meeting of the TAB will take place during the execution of the NEURONS project.

2.1.2. Decision making mechanisms

Decisions of the MB are normally taken by **consensus**. To ensure an efficient and transparent decision making process, a **voting system** by simple majority vote and with one vote per partner will be implemented if no consensus can be reached. In case of a tied vote, the vote of the PM will be decisive.

The SC will also strive to reach decisions by consensus. Only if an issue cannot be solved by consensus will it be escalated to the level of the MB. In the case of a conflict between the project partners or a lack of decision that cannot be resolved by either the PM or the MB, the issue may be further escalated to the TAB.

The EC will be informed beforehand of any conflicts that might jeopardize the smooth progress of the project. If urgent decisions and measures need to be implemented a previous consultation with the EC will be made to ensure the proper compliance of the project with the EC expectations.

2.1.3. Matched to the scale and complexity of the project

Overall, the management is organized in three levels:

- **Strategic** management (MB)
- **Project** management, i.e. administrative, financial and organizational management (PM)
- **Operational** management (SC and WPL)

The management structure safeguards that tasks, deliverables and responsibilities will be clear and manageable for all partners. The procedures - related to the monitoring of project progress, the communication and consultation between the partners at the different levels, the handling of conflicts or emergencies, and the deciding mechanisms - ensure that the project can be executed efficiently, transparently and with a fair distribution of responsibilities between the partners. Additional mechanisms have been built in to protect the interests of the SME participants.

The person month effort for management activities in the project (22 person-months) represents 5.7% of the total person month effort. This should be considered adequate and appropriate for an RTD project of the size of NEURONS (total cost **€4,235,745**, duration of 36 months and 12 partners).

2.2 Individual participants

1 (COORDINATOR)	ISTITUTO NAZIONALE DI FISICA NUCLEARE	INFN	I

INFN is an organization dedicated to the study of the fundamental constituents of matter, and conducts theoretical and experimental research in the fields of subnuclear, nuclear, and astroparticle physics. It was founded on 8th August 1951 to uphold and develop the scientific tradition established during the 1930s by Enrico Fermi and his school, with their theoretical and experimental research in nuclear physics. Today the INFN employs some 5,000 scientists whose work is recognised internationally not only for their contribution to various European laboratories, but also to numerous research centres worldwide. INFN's first National Laboratory in Frascati, INFN Laboratori Nazionali di Frascati LNF, and three important INFN Departments (i.e. INFN Pisa, INFN Pavia and INFN Milan) participate in the project NEURONS.

Tasks in the project
INFN is project coordinator and it is responsible for WP1 Project management and coordination. In addition, it has a significant contribution to WP2 ASICs Development, tasks 2.1 and 2.3 as well as to WP 3 Board development, tasks 3.5 and 3.6. INFN will be extensively involved in WP4 Test Bench Applications Demonstrations, tasks 4.1, WP 5 Design for further integrated system, task 5.1 and will be in charge of dissemination activities in WP 6 task 6.1.

Relevant experience
Of its countless international activities, some of the most important research is conducted at CERN in Geneva. Italy was one of the European laboratory's founding Member States and, through the INFN, it continues to be one of its most active members. Around 1,000 scientists from the INFN work in research groups at CERN, taking part in all experiments with the LHC particle accelerator (CMS, ATLAS, ALICE, LHCb, LHCf, Totem) and the SPS accelerator (COMPASS).
The INFN is also a major contributor to experiments at other leading foreign laboratories including FERMILAB, SLAC, BNL, and JLAB (United States); PNPI, BINP and JINR (Russian Federation); CIAE and IHEP (China); RIKEN and KEK (Japan); BARC (India), DESY and GSI (Germany), ESRF (France), PSI (Switzerland) etc.

In Italy, international collaboration is mainly concentrated at the INFN's four national laboratories, where major experimental facilities are available for use by the scientific community. One example is the VIRGO, interferometric antenna at Cascina, near Pisa, a joint-venture with the French CNRS IN2P3. The INFN also takes part in European scientific computing and nuclear physics projects. Together with numerous other research agencies from leading European countries, it founded the ApPEC (Astroparticle Physics European Coordination); it is a founding member of the French-Italian European Gravitational Observatory (EGO) Consortium (Cascina-Pisa); it is a member of the European Science Foundation (ESF) based in Strasbourg; it coordinates the EU-IndiaGRID2 project to improve grid technology in India. It has representatives on the NuPECC (Nuclear Physics European Collaboration Committee), on the PESC (Physical and Engineering Sciences) of the ESF, on the ICFA (International Committee Future Accelerators), on the ECFA (European Committee Future Accelerators) and on the FALC (Funding Agencies for Large Colliders). It is a member of the European Association for the Promotion of Science and Technology (EUROSCIENCE) in Strasbourg; it is a founding member of Science Europe based in Brussels; it holds a stake, with the CNR, in the European Synchrotron Radiation Facility (ESRF) in Grenoble.

Fundamental research in these areas requires the use of cutting-edge technologies and instrumentation, which the INFN develops both in its own laboratories and in collaboration with the world of industry. These activities are conducted in close collaboration with the academic world.
The INFN has a significant impact on Italian society. The technology and expertise developed by the INFN in conducting its experiments has major implications for the medical and healthcare industry and for the technology sector in general. Of the numerous examples, the development of a technique that uses carbon ions and protons to treat tumours (hadron therapy) stands out as particularly significant. The INFN has over a decade of experience in this field, gained directly at its laboratories in Catania. It built the hadron therapy machine installed at the CNAO in Pavia. The INFN is also a leading national and international player in the GRID, supercomputing network project and in expanding its use to applications in other scientific fields, e-commerce and culture. The INFN also uses its own analysis and research instruments and facilities to addresses issues regarding the cultural and environmental heritage.
Finally, the INFN is fully committed to promoting scientific culture. It takes part in all the main dissemination activities in Italy and each year it organises various exhibitions and events throughout the country, some of which are broadcast on TV.

Staff committed to the project
Staff from INFN's four national laboratories (i.e. INFN Pisa, INFN Laboratori Nazionali di Frascati LNF, INFN Pavia and INFN Milan) is commited in the project NEURONS.

Department: INFN Pisa	
Person short CV	**Paola Giannetti**, Director of Research. Proponent of the FTK processor for LHC experiments and project leader of the INFN funded FTK R&D project (1999-2001, [1]). Proponent of three trigger upgrades at CDF (2002-2008, [2]) and INFN funds responsible. FTK deputy project leader at ATLAS and responsible of INFN funds (2008, 2012 [3]).
WP activity	WP1: General coordination of the project. WP2: Cooperation with IMEC and Microtest. WP6: Participation to dissemination and exploitation activities.
Publications	[1] IEEE Trans. Nucl. Sci. **48**, 575 (2001): The Fast Tracker Processor for Hadron Collider Triggers [2] IEEE Trans. Nucl. Sci. **56**, 1685 (2009): Level-2 Calorimeter Trigger Upgrade at CDF [3] IEEE Trans. Nucl. Sci. **55**, 145 (2008): Performance of the Proposed Fast Track Processor for Rare Decays at the ATLAS Experiment
Person short CV	**Roberto Beccherle**, Technological Researcher. PhD in Physics with specialization in VLSI chips design. Analog and Digital VLSI circuits, using both standard cell libraries and full custom design, tailored to the readout electronics of both micro strip and pixel detectors. Development of global system architectures for fast and serial readouts.
WP activity	WP2: standard cell logic design and simulation for AMMA-chip05. Prototype tests, consumption measurement. WP5: optimization of the AMMA-chip06 design for the final size of the chip exploiting the past experience on AMMA-chip05 and increasing pattern density at the maximum level.
Publications	[1] "A VLSI Front-End circuit for microstrip silicon detectors for medical imaging applications", Nucl. Instr. and Meth. A436 (1999), pp. 401-414. [2] "A VLSI Front-End circuit for microstrip silicon detectors for medical imaging applications", Nucl. Instr. and Meth. A436 (1999), pp. 401-414. [3] "A high-rate X-Y coincidence VLSI system for 2-D imaging detectors", Nucl. Instr. and Meth. A394 (1997), pp. 191-198.
Person short CV	**Roberto Dell'Orso**, Senior Researcher. CMS Tracker Inner Barrel construction and commissioning project leader (2004-2007). CMS Pisa Team Leader (2005-2008). Co-proponent of micro-strip stacked modules for tracking at HL-LHC (2009-2010)
WP activity	WP4: Simulation of Pattern matching for HLT and L1 tracking triggers in CMS using the Associative Memory based computing unit
Publications	[1] IEEE 48, 2299-2302 (2001): Recent Results for the CMS Tracker Silicon Detectors [2] JINST 5, T03008 (2010): Commissioning and Performance of the CMS Silicon Strip Tracker with Cosmic Ray Muons [3] JINST 5, C11018 (2010): Design and Development of Microstrip Stacked Module Prototypes for Tracking at S-LHC
Person short CV	**Fabrizio Palla**, Senior Researcher Electroweak physics at LEP, Beauty physics at LEP and LHC, Higgs Physics at LHC ALEPH and CMS b-tagging group leader (1999-2005) CMS Tracker Detector Performance (Detector and Tracker offline Commissioning) Group Leader - (2007-2008). CMS Pisa Team Leader (2009-2012). Proponent of usage of the Tracker in the High Level Trigger in CMS, funded EU project and Pisa node leader (2002-2006). Proponent of L1 Track Triggers at LHC (2006-2012)
WP activity	WP4: Simulation of Pattern matching for HLT and L1 tracking triggers in CMS using the Associative Memory based computing unit
Publications	[1] JINST 2 P02002: Proposal for a First Level Trigger using pixel detectors for CMS at Super-LHC [2] Eur. Phys. J. C (2010) 70: 1165–1192, CMS tracking performance results from early LHC operation [3] Physics Procedia (2012) 37, 1925–1932, Design and Studies of μ-strip Stacked Module Prototypes for Tracking at Super-LHC
Person short CV	**Alessandro Giassi,** Researcher. DAQ expert for the Aleph Hadron Calorimeter and the CMS Silicon Strips Tracker [1]
WP activity	WP4: Running the Associative Memory based computing unit to perform pattern recognition in CMS
Publications	[1] R.Bainbridge et al "Data acquisition software for the CMS strip tracker" J. Phys. Conf. Ser. 119 (2008) 022008
Person short CV	**Giacomo Sguazzoni**. Researcher. Member of CMS (LHC) collaboration, former member of Aleph (LEP) collaboration. Tracking group convener [1] and tracker material group convener [2] in CMS. R&D, integration and commissioning of the CMS Silicon Strip Tracker with coordination responsibilities [3]. R&D, integration and commissioning of Upgraded ALEPH Silicon Vertex detector [4].
WP activity	WP4: application of AM to speed up the track reconstruction at CMS

Publications	[1] PoS(Vertex 2011)013, Performance of the CMS Silicon Tracker [2] CMS-PAS-TRK-10-003, Studies of Tracker Material [3] 2008 JINST 3 S08004, The CMS experiment at the CERN LHC [4] 1998 Nucl. Phys. Proc. Suppl. 61B 201–206, Construction and performance of the new ALEPH vertex detector

Department: INFN Laboratori Nazionali di Frascati (LNF)	
Person short CV	**Mario Antonelli.** Researcher. Responsible of the ATLAS-LNF INFN group. Kaon physics coordinator in KLOE, Kaon Physics coordinator in FlaviaNet, Particle Data Group author, physics generators convener in ECFA/DESY, ATLAS LNF Team leader
WP activity	WP6: Participation to dissemination and exploitation activities.
Publications	[1]The ATLAS level-1 trigger: Status of the system and experience from commissioning with cosmic ray muons, IEEE Nuclear Science Symposium Conference Record, 2007. NSS '07. Volume: 3, 2007 , Page(s): 2123 – 2129 [2] [KLOE Collaboration], First observation of quantum interference in the process phi ---> K(S) K(L) ---> pi+ pi- pi+ pi-: A Test of quantum mechanics and CPT symmetry, Phys. Lett. B 642, 315 (2006) [3] [ATLAS Collaboration], ``Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC", Phys. Lett. B 716, 1 (2012)
Person short CV	**Alberto Annovi**, Researcher. Project leader of the Silicon Vertex Trigger (SVT) upgrade for the CDF experiment [1](2004-2005). Responsible of the AMMA-chip and the Vertical Slice (2010-2012) for the FastTracker processor for the ATLAS experiment [2] and consultant for the future ATLAS and CMS L1 track trigger [3]. Inventor of the "variable resolution Associative Memory" [4].
WP activity	WP1 managment INFN (project leader) WP2 AMMA-chip development, submission, and tests; consultant for WP4, WP5 and WP6
Publications	[1] The Silicon Vertex Trigger upgrade at CDF, doi:10.1016/j.nima.2006.10.383 [2] Hadron collider triggers with high-quality tracking at very high event rates. doi:10.1109/TNS.2004.828639 [3] Associative Memory for L1 Track Triggering in LHC Environment, doi:10.1088/1748-0221/7/08/C08009 [4] A new "Variable Resolution Associative Memory" for High Energy Physics, doi:10.1109/ANIMMA.2011.6172856
Person short CV	**Matteo Beretta**, Hardware Engineer. Designer of the full custom Associative Memory core of the FTK processor [1] [2](2009-2012). Designer of the first prototype of the clustering mezzanine and the clustering algorithm implemented on it (2009-2012).
WP activity	WP2: Participation to Full custom design and floorplanning of 2D AM and simulation. WP3: clustering mezzanine firmware design, implementation and test.
Publications	[1] Real Time Conference (RT), 2010 17th IEEE-NPSS 2010 , Page(s): 1 - 3: Associative memory design for the FastTrack processor (FTK) at ATLAS [2] JINST 7 (2012) C10002 "FTK: A fast track trigger for ATLAS ", [3] Nucl.Instrum.Meth., vol. A617, pp. 254-257, 2010. A Fast General-Purpose Clustering Algorithm Based on FPGAs for High-Throughput Data Processing".
Department: INFN Pavia	
Person short CV	**Agostino Lanza,** Director of Technological Research. Involved in the ATLAS experiment since 1995, contact person of the ATLAS-Pavia group during the MDT chamber construction (2001-2006) [1], responsible of the ATLAS Muon detector services during the installation phase (2005-2010) [2], committed in the ATLAS Fast TracKer project since 2010 [3].
WP activity	WP3: development of test setup for the LAMB boards.
Publications	[1] Construction of the inner layer barrel drift chambers of the ATLAS muon spectrometer at the LHC, Nucl. Instr. and Meth. A 546, 481-497 (2005); [2] Power Supply System for the ATLAS Muon Spectrometer: Design Specifications and Test, IEEE Trans. on Nucl. Science, Vol. 51, 5 – 2220-2226 (2004); [3] The AMMA-chip04 and the processing unit prototype for the FastTracKer, JINST 7 C08007 doi: 10.1088/1748-0221/7/08/C08007.
Person short CV	**Roberto Ferrari,** Director of Research, responsible of the ATLAS-Pavia INFN group, committed in ATLAS data acquisition (DAQ) activities since the very beginning [1], developer and manager of several packages for ATLAS DAQ online monitoring [2][3], designer, developer and responsible of CERN-RD52 experiment DAQ.
WP activity	WP3: development of firmware and test setup for the LAMB boards.

Publications	[1] Comput. Phys. Commun. 110, Berlin (1998), Proceedings of the 1997 International Conference on Computing in High Energy Physics: The ATLAS DAQ and event filter prototype project [2] IEEE Transactions on Nuclear Science, vol. 53, New York (2006): GNAM: A low level monitoring program for the ATLAS experiment [3] Nucl. Phys. B Proc. Suppl. 215 (2011): ATLAS-detector operations with beams: the data-acquisition perspective
Person short CV	**Andrea Negri**, faculty researcher University of Pavia. Member of the ATLAS experiment since 1996. Involved in ATLAS data acquisition [1] with the following responsibilities: third level trigger infrastructure coordinator, data-flow evolution coordinator, Italian representative for trigger and data acquisition. From 2010 committed in the Fast TracKer project [2,3].
WP activity	WP3: development of firmware and test setup for the LAMB boards.
Publications	[1] Integration of the trigger and data acquisition systems in ATLAS, J.Phys.Conf.Ser. 119 (2008) 022001 [2] Enhancement of the ATLAS trigger system with a hardware tracker finder FTK, JINST 5 C12037, DOI 10.1088/1748-0221/5/12/C12037 [3] FTK: a fast trigger for ATLAS, JINST 7 C10002, DOI: 10.1088/1748-0221/7/10/C10002

Department: INFN Milan	
Person short CV	**Mauro Citterio,** Director of Technological Research. Design of Integrated and Hybrid Circuits, Multi Chip Modules (MCM) and Acquisition System for High Energy Physics Experiments [1, 2]. ATLAS Liquid Argon Calorimeter Electronics Coordinator. Testing of Electronics circuit and their qualification against radiation [3].
WP activity	WP3: Development of the test setup for the AMMA-chip.
Publications	1] J. Instrum. 3 (2008) P09003: ATLAS liquid argon calorimeter front end electronics [2] J. High Energy Phys. 06 (2011) P06005: Power supply distribution system for calorimeters at the LHC beyond the nominal luminosity [3] J. Instrum. 7 (2012) C08007: The AMMA-chip04 and the Processing Unit Prototype for the FastTracker
Person short CV	**Chiara Meroni**, Director of Research. Director of the Milan INFN Department. Responsibilities of: (a) Atlas-Italia upgrade projects (2009-2012) (b) ATLAS-Milan INFN group (2007-2011).
WP activity	WP6: Participation to dissemination and exploitation activities.
Publications	IEEE Transactions on Nuclear Science,Volume: 59 , Issue: 2 (2012) , Page(s): 348 – 357, "The FastTracker Real Time Processor and Its Impact on Muon Isolation, Tau and b-Jet Online Selections at ATLAS" IEEE Transactions on Nuclear Science, Volume: 37 , Issue: 2 (1990) , Page(s): 236 - 240 "Results on heavy quark selection through an impact parameter trigger"

2	CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE	CNRS	F

The LPNHE (Laboratoire de Physique Nucléaire et des Hautes Energies) of Paris is a Mixed Unit of Research (UMR7585) of CNRS, Université Pierre et Marie Curie (UPMC) and Université Paris Diderot. It is composed of 12 research and 5 support groups (administration and services) for a total of about 200 persons.

Tasks in the project
LPNHE is the leader of WP 2 ASICS development, and has contributions to WP 5 design for further integrated system, task 5.1

Relevant experience
Among the different Collaborations there are many involving High-Energy Physics: ATLAS at CERN, CDF and D0 at Fermilab, BaBar at SLAC, T2K in Japan; the participation in cosmic rays studies is represented by contributions to HESS in Namibia and AUGER in Argentina; cosmology by SNLS and LSST.

The LPNHE is equipped with a few ISO7 and ISO8 clean rooms, presently used for the ATLAS and LSST R&D. Among other instruments, they are equipped with a Karl Suss PA200 Semiautomatic Probe station with a temperature controlled chuck (-60+200C); semiconductor parameter analyzers; laser systems coupled to XY stages for charge collection efficiency characterization of Silicon sensors; all the other necessary instrumentation for R&D on silicon sensors.

The Electronics Division of the laboratory is providing all the necessary support in chip design (recently a 65nm CMOS process) and peripheral electronics development (FPGA programming, card design and assembly), Cadence for board design and Xilinx, Altera CADs, Tier3 Computing facility.
A large mechanical workshop equipped with numerical controlled machines is providing the necessary infrastructure for detector building.

Relevant publications:
[1] S. Amerio et al., “GigaFitter: Performance at CDF and perspective for future applications”, Nucl. Instr. and Meth. A, vol. 623, pp. 540-542, 2010.
[2] A. Andreani,et al., “The FastTracker Real Time Processor and Its Impact on Muon Isolation, Tau and b-Jet Online Selections at ATLAS”, IEEE Transactions on Nuclear Science, Volume: 59 , Issue: 2, 2012 , Page(s): 348 – 357
[3] Study of the radiation hardness of irradiated AToM front-end chips of the BaBar silicon vertex tracker. S. Bettarini, M. Bondioli, L. Bosisio, G. Calderini, S. Dittongo, F. Forti, M.A. Giorgi (2006) 5 pp. Published in IEEE Trans.Nucl.Sci. 53 (2006) 584

Staff committed to the project
Giovanni Calderini, former Pisa University and Scuola Normale student, is Director of Research (DR2) at LPNHE. He is the Group Leader of the Atlas Group. He was the Project Leader of the BaBar Silicon Vertex Tracker (SVT) and has been Run Coordinator of PEP-II at SLAC. He has extensive experience of Collider
Physics and Silicon Trackers in High Energy Physics and is the responsible of the activities for the ATLAS upgrade at LPNHE.
Francesco Crescioli Ingénieur de recherche classe IR2 (stagiaire). Activité : Electronique (Ph.D. in Applied Physics in 2010 at the University of Pisa). He had an important role in the SiliconVertex Tracker upgrade at the CDF experiment (Fermilab). He was the responsible of the GigaFitter, a single board that replaced the old 12 Track Fitters (9U VME boards) to perform10^9 track fits per second. Crescioli had also a key role in FTK, for the ATLAS experiment. He developed the FTK simulation package, was one of the key designer of the AM04 chip , and organized the vertical slice environment for prototype tests.

3	Microtest SRL	Microtest	I

Founded in 2004, Microtest is a company operating in the field of microelectronics consultancy relating to the design, testing, qualification and industrialization of electronic circuits primarily for use in automotive applications. In particular, the company operates in the field of advanced electronics dedicated to the design and manufacture of machinery for the testing of electronic devices used in the automotive industry. Microtest has researched and manufactured products resulting from the collaboration with leading electronics companies such as ST Microelectronics, Philips, Infineon, Delphi, Denso, Motorola, Bosch and has partnerships with US-based Teradyne.
Microtest's mission covers three main objectives: Integration of design and semiconductor test within the same structure, optimizing the synergies needed to reduce the time-to-market and cost of the product; Optimization of the flow test, reducing the time and increasing the quality of the product; Ability to provide ready to use solutions that are integrated in the same organization: designing, testing and reliability, delivering to their customers the product at an early stage of production. Microtest is a UNI EN ISO 9001: 2008 certified company and it is ISO compliance with following activities: "Design, testing development and testing execution of integrated circuits. Design and production of electronic application boards and ATE (Automatic Test Engine)".

Tasks in the project
The main contribution of Microtest is in WP 2 ASICS Development and responsible for tasks 2.6 and 2.7. In addition, Microtest is responsible for task 3.8 and 6.3.

Relevant experience
Microtest participated (2001-2002) in the Test program development for Coincidence Matrix ASIC Trigger, (CMA) that performs most of the functions needed for the read-out of the ATLAS Muon Barrel LVL1 trigger.

In the latest years, Microtest has also launched four major projects for innovation and R & D as described below:
1) Innovation project in the application concessionary advanced on 31/1/07 to Tuscany to rely on a decree of the Tuscany Region 5425 of 27/10/06; total amount of € 369,485.23.
2) R & D project under Contract 2006 "Aid for pre-competitive development" of Tuscany entitled *"Development of a prototype machine for electronic components Burn In"* funded with an intervention of € 60,581.50 in respect of an investment held allowable € 173,090.00.
3) R & D specified in the notice of the Tuscany Region dedicated to R & D in the area of 2, 3 and 4-wheel vehicles and components. The investment program, referred to in the contract signed between the Region of Tuscany and Microtest as leader of a group of companies on 19/11/2007, consists in the *"Research and development of innovative investment in ATE and accessories, including the purchase of equipment specifications characterized by a high degree of innovation"* and the registration of a patent on an international level. This project had an eligible investment of € 891,300.00 and € 446,160.00 contribution recognized.
4) R & D project referred to in Notice 2010 "Aid for pre-competitive development" of Tuscany entitled "Creation of micro devices". The project includes the study, design, construction and development of a microelectronic device for integrating multi-function voltage generators and digitizers for different uses including, the main one is in a ATE; financed by an intervention of € 300,000.00 against an investment of € 135,000.00 considered eligible.

Staff committed to the project
The working group is chosen for the project is highly qualified. All employees have long-term experience in the field. The working group has been appropriately selected among the 49 people employed at the company crossed the activities of the project with an established company specific competencies. The staff involved in the present project is highly qualified and consists of R&D people with degree in electronic engineering.
Masoni Simone, degree in electronic engineering, joined Microtest in 2000. He has experience in Analog and Digital Designer, Cadence, VHDL Verilog, C++ .
Consani Emiliano joined Microtest in 2000. He is an electronic engineer and has experience in Analog and Digital Designer, Cadence, VHDL Verilog, C++ .
Gennai Simone, degree in electronic engineering has extended experience in Testing of Microelectronic circuit, for different fields. Automotive, Space, Medical etc.
Germani Eleuterio graduated as electronic engineer and is senior engineer in high complex PCB design.
Picchi Francesco: has experience in testing of microelectronic circuits and production test program development for different fields (i.e. Automotive, Industrial etc.)
Valvo Francesco is an electronic engineer with strong experience in production process and test program optimizations for production applications.

4	ARISTOTELIO PANEPISTIMIO THESSALONIKIS	AUTH	EL

AUTH is the largest Greek University with more than 90k students, and the largest span of topics covered. It is a pioneer in research in Greece; from Archeological excavations, Classics and Medicine, to Engineering and Sciences, the University holds a leading role in the cultural life of Thessaloniki. As far as Science is concerned, the University is a pioneer in the dissemination of Science in the broader region of Northern Greece (Macedonia and Thrace), having established the very active Centre, NOESIS, for the Diffusion of Sciences in the Society).
The Physics Department has about 90 faculty members. It conducts research in Solid State Physics, Nano science, Nuclear and Particle Physics, Astronomy and Astrophysics, Electronics and Computing, and other Applications of Physics (including environmental Physics, antenas, archeometry and measurements on nuclear fallouts). The Department of Physics has a very significant share of the publications and research conducted AUTH. Two divisions of The Physics Department are participating in the NEURONS project: *Division of Nuclear and Particle Physics* and *Division of Electronics and Computing*.

Tasks in the project
The main contribution of AUTH is in WP3 and WP4. AUTH is leader of WP 3 Board Development and together with other partners it is involved in WP4 Test bench Applications and Demonstrations, tasks 4.2 and 4.3.

Relevant experience
The Division of Nuclear and Particle Physics has a long standing involvement in particle physics experiments at CERN. The ATLAS group of AUTH was formed 14 years ago and had a sizable contribution (over 10%) to the construction of the precision tracking muon chambers of ATLAS. The group has also expertise in Trigger and Data Acquisition (DAQ), specifically in the event building software with multi-threaded C++, and online monitoring of the data collected from the muon detectors. The group has also a leading role in the physics exploitation of the collected data (conveners of the B-physics group, leading the analysis of ZZ production, which is not only the main background for the Higgs->ZZ->4l channel, but also a probe for new physics). The group has a good laboratory infrastructure and access to the Grid facilities of the University, to the establishment of which it was a pioneer.
The Division of Electronics and Computing has extensive experience in high speed and low power system level digital design, FPGA programming, algorithm implementation on hardware, testing and firmware development. The group is experienced in hardware design and verification (VHDL) as well as Hardware/Software codesign (EDK Xilinx environment) for the implementation of DSP and computationally intensive image/video processing algorithms. The group has developed in house machine vision applications targeting FPGA devices. Their research also targets ASIC design (Cadence).

Staff committed to the project
Dr. Konstantinos Kordas, Ph.D in Experimental Particle Physics (McGill University, Canada, 2000) is Lecturer at Division of Nuclear and Particle Physics, Dept. Physics and he is AUTH - Local Coordinator of NEURONS project. He was working at the CDF experiment at Fermilab, searching for penguin decays of B mesons and started involvement in the ATLAS experiment at CERN in 2000, as a Research Associate at LAL, Orsay, France, working on the ATLAS simulation with the Geant4 C++ tool kit. He continued to work at the CDF experiment (2002-2004) as a Research Associate at University of Toronto, measuring the mass of the top quark. Since then he is involved in ATLAS, at the Trigger and Data Acquisition (TDAQ) system; initially as Research Associate with the Frascati labs of INFN in Italy (2004-2006), and then with the University of Bern in Switzerland (2006-2009) working mostly in the global event builder (software with multi-threaded C++ and system commissioning). Since 2010 he is a faculty at AUTH, continuing in the ATLAS TDAQ and participating in physics analysis with the group with an interest in Diboson, and Higgs and physics beyond the standard model. Since December 2011 he is the coordinator of the ZZ->4 leptons analysis and participates in the upgrade projects in the TDAQ (FTK) and in the detector activities (new muon detectors: Micromegas) of the group.
Dr. Chariclia Petridou, Ph.D. in Experimental Particle Physics (University of Syracuse, New York, 1983) is Professor at Division of Nuclear and Particle Physics, Dept. Physics. From 1985 to 1995 she worked at CERN, at the UA2 experiment, where she studied the weak interactions, the properties of the intermediate vector bosons W and Z and then at the DELPHI experiment at LEP, where she studied the properties of the b-quark and the trilinear gauge couplings of the W and Z bosons. In addition, already from 1992 she was participating in studies for the discovery of Higgs from muon measurements at LHC. Since 1995, as Associate Professor of the Department of Physics at AUTH, she created the ATLAS group of Thessaloniki that built in collaboration with the Laboratory of Engineering (EEDM) of AUTH, the University of Athens and the NTUA in Athens, 10% of the ATLAS muon spectrometer. The group tested the performance of the first chambers with cosmics, in Thessaloniki and participated in the commissioning certification and installation of the chambers at CERN. The past two years she was the convener of the b-Physics working group of ATLAS and today she coordinates the b-physics and the multilepton analyses for diboson measurements, the discovery of the Higgs and New Physics at the Aristotle University.
Dr. Dimos Sampsonidis, PhD in Experimental Particle Physics (Aristotle University of Thessaloniki, 1995) is Ass. Professor at Division of Nuclear and Particle Physics, Dept. Physics, AUTH. He has worked as Research Associate at CNRS at Strasbourg France and at CERN. Since 1996 he joined the ATLAS group of Thessaloniki and worked on the construction of the muon

chambers of the ATLAS muon spectrometer. His research activity is mainly in the field of experimental Particle Physics, in detector instrumentation and in GRID applications. He is actively involved in the development of a Micromegas detector for the upgrade of the muon spectrometer for the SLHC. The results of his research have been published in well over 150 papers in international scientific journals and conference proceedings. He is high experienced on the alignment system (RASNIK) which was used in the Quality Control procedure during the ATLAS muon chambers construction in Thessaloniki. The same system is used for the alignment of the whole ATLAS muon spectrometer.

Dr. Spiros Nicolaidis, PhD in Electrical Engineering is Assoc. Prof, Division of Electronics and Computing, Dept. Physics, AUTH. Since September 1996 he has been with the Department of Physics in AUTH. He is employed in the area of digital circuit and system design. His current research interests include: modelling the operations of basic CMOS structures, development of analytical expressions for the propagation delay and the power consumption of CMOS structures, design of high speed and low power digital circuit and embedded systems, modelling the power consumption of embedded processors. He is author and co-author in more than 130 scientific articles in international journals and conference proceedings while his work has taken more than 400 references. Two articles presented in international conferences were achieved honorary awards. He also contributes to a number of research projects funded by European Union and Greek Government where in many of that has the scientific responsibility.

5	UNIVERSITE DE GENEVE	UNIGE	CH

The Département de Physique Nucléaire et Corpusculaire (DPNC) of the University of Geneva (UNIGE) is one of the leading institutes in particle and astroparticle physics in Switzerland.

Tasks in the project
The main contribution of UNIGE is in WP3 Board Development, tasks 3.3 LAMB design and development.

Relevant experience
DPNC has been the founding member of several major international collaborations, including L3, ATLAS, AMS. It has a long tradition in the R&D, design and construction of silicon tracking detectors and its associated electronics and has been the leading institute in the L3 Silicon Microvertex detector (SMD), the CDF Silicon Vertex Trigger (SVT), the AMS silicon tracker, the ATLAS Silicon tracker (SCT) and the ATLAS Insertable Barrel Layers (IBL). Specific to the Fast Tracker (FTK) project, the DPNC has excellent expertise on developing electronics for high performance online computation, having developed many similar systems in the past. Currently the DPNC is participating in the vertical slice integration of the FTK into the ATLAS experiment and is planning to play a leading role in the LAMB development and production.

Staff committed to the project
Xin Wu (Associate Professor) has obtained a Ph.D in particle physics from Massachusetts Institute of Technology in 1990, and has been associated with the DPNC since 1991, first as a postdoc, then as senior lecturer, and now associate professor. Over the past twenty years has participated and made important contributions to several major experiments in particle physics (UA1, CDF, ATLAS). As a key person of the Hadron Collider Group at DPNC, he has initiated and led many detector and data analysis projects. He has long experience in trigger and readout electronics, and played a leading in the ATLAS trigger development and commissioning, serving as Deputy Trigger Coordinator for ATLAS in 2007-2009. He is currently the deputy team leader of the ATLAS Geneva group, responsible for trigger related activities, including FTK, and several data analyses.
Szymon Gadomski (Scientific Computing Specialist): as a Technical Doctoral Student at CERN in 1992 he has started working for future experiment that later became ATLAS, testing prototypes of the silicon microstrip detectors and performing inner tracker performance studies. He has obtained a Ph.D in experimental particle physics from the Institute of Nuclear Physics in Cracow in 1996. Between 1996 and 1998 he has worked at the University of Toronto analysing data of the CDF experiment. Returning to CERN as a Fellow in 1999, he has played the leading role in the development of the simulation for the Semiconductor Tracker of ATLAS. Between 1992 and 1997 he was working at the University of Bern, playing an important role in the development of the ATLAS data acquisition software and helping to set up the first Grid computing facility. Since 1997 he is responsible for the Grid computing cluster at the University of Geneva. He has recently started to contribute to the tests of the FTK prototypes.

6	UNIVERSITA DEGLI STUDI DI FIRENZE	UNIFI	I

The University of Florence (UNIFI), established in 1321, is one of the largest organizations for research and higher education in Italy, with over 2000 tenured teaching staff and researchers, over 1600 permanent technical/administrative staff and language assistants, over 1900 PhD Students and Postdocs and over 55 thousand students enrolled. It comprises 12 faculties and 139 first and second level degree Programmes.

Tasks in the project

UNIFI is leader of WP 4 Test Bench Applications Demonstrations and its main contribution refers to tasks 4.3 Salient visual features and motion reconstruction.

Relevant experience

This research will be developed within two distinct Departments of University of Florence: *NEUROFARBA* and the *Physics and Astronomy Department.* Following the recent reorganization of Italian University system, new Departments will be formed and will be effective from January 1st 2013.

1. *NEUROFARBA* is one of these and one of the largest Departments of the University, comprising researchers from the old departments of Psychology, Preclinical and Clinical Pharmacology, Neurology, Pediatrics and Pharmaceutical Sciences, covering research programs within the fields of neuroscience, psychobiology, neuropharmacology, study of neurologic and psychiatric diseases, experimental psychology, neonatal retinal and brain damage. These scientists have collaborations throughout the world, a high rate of publications on high impact journals such as Science and Nature, with very high bibliometric indexes, and some of them are rated Top Italian scientists (VIA-academy). The departments has funding by several national and international agencies and institutions (European Union: FP7- ERC, Miur, Regione Toscana, IIT, Telethon, Royal Society, Fondazione Meyer) as well as private institutions (Fondazioni Bancarie, Industries).
2. *The Physics and Astronomy Department* is doing research in the fields of Nuclear and Particle Physics, Atomic and Solid State Physics, Theory of Fundamental Interactions, Astronomy, Astrophysics and Space Physics. It has been rated among the Excellence group by the Centre for Higher Education Development (CHE) in 2010. The research program in Particle Physics is large and has important collaborations with European Center for Particle Physics (CERN) and Italian Institute for Nuclear Physics (INFN). One of the main collaboration is the participation to the Compact Muon Solenoid Experiment at the CERN Large Hadron Collider. The Physics Department contributed, together with the local INFN section to the design, construction, and test of the inner part of the Silicon Strip Tracker, the largest ever built.

Staff committed to the project

1. NEUROFARBA Department

Maria Michela del Viva (Researcher at University of Florence, Coordinator of the consortium): has graduated in Biology, 110/110 summa cum laude, University of Pisa (1990) and was granted her PhD in Biophysics by University of Pisa (1997). She is currently Assistant Professor at the Department of Psychology (UNIFI) (2000) and Senior Fellow and Associate of Institute for Mind and Biology, University of Chicago (2008).

Since 1991 (Neuroscience Institute of CNR-Pisa and Department of Psychology-UNIFI), she has been studying human vision, by devising computational models of motion perception, psychophysical experiments and visual evoked potential recordings in adults, elderly and typically developing children. She has done applied research as consultant for "Technobiochip" (software simulating human vision) and F.I.A.T. Research Center (psychophysical measurements of optimal car lights illumination). She has been studying visual deficits in clinical populations, with psychophysical and electrophysiological (VEP) techniques, in collaboration with the Neurology Division of Careggi Hospital of Florence (DAT patients) and IRRCS Stella Maris, (patients with autism, down syndrome and periventricular leucomalacia). She participated to collaborations with engineers for applications to robotics: CNR project "Robotics"(computational models of motion perception) and Italian Institute of Technology (cross-modal visuo-haptic perception).

Since 2006, she has been studying pattern recognition in information processing systems, in collaboration with physicists of INFN, Universita' di Pisa and Fermilab and the Institute for Mind and Biology (IMB)-University of Chicago, devising a model for feature extraction and information compression in early vision.

She is referees for international journals and has received funding by MIUR and University of Florence.

Selected Publications

1. Del Viva M. M. & Morrone M.C. (1998). Motion detection by feature tracking. *Vision Research*. **38** 3633-3653.
2. Del Viva M. M. & Morrone M.C. (2006) A feature-tracking model simulates the motiondirection bias induced by phase congruency. *Journal of Vision* 6(3), 179-195.
3. Del Viva M.M. & Gori M. (2008) Anti-glass patterns and real motion perception: same or different mechanisms? *Journal of Vision* 8, (2): 1-15
4. Guzzetta A., Tinelli F., Del Viva M.M., Bancale A., Arrighi R., Pascale R.R. and Cioni G.(2009) Motion perception in preterm children: role of prematurity and brain damage. *NeuroReport.* 20(15):1339-1343.

5. Del Viva M.M., Agostini R., Benedetti D. and Punzi G. (2010) The limited availability of brain resources determines the structure of early visual processing *Journal of Vision* 10(7): 1360.
6. Del Viva M. M., Tarallo N., Benedetti D., Punzi G. and Shevell S. (2012) Color information processing in early visual analysis *Perception* 41: 19.

Manila Vannucci has Graduated in Psychology (1997), UNIFI. She had a Research Scholarship (1999) granted by University "La Sapienza", Rome and conducted research at the Department of Epileptology, University of Bonn. She was awarded her PhD (2004) in Psychology and Cognitive Sciences, at UNFIF. She was granted a Research Fellowship by CNR (2006) and performed research at Department of Clinical Neurophysiology, Zurich (Switzerland). Since 2004 she is assistant Professor at Department of Psychology at UNIFI.
Her research activities and interests are in the field of cognitive psychology and neuropsychology on visual object processing: object identification and aesthetic processing; visual imagery; visual memory and memory distortions in healthy subjects and neuropsychological patients (temporal lobe epilepsy patients and patients with Alzheimer disease), using different research techniques, such as behavioral (reaction times, accuracy, self-report questionnaires) and electrophysiological techniques (surface ERPs and intracranial ERPs with subdural and depth electrodes). Her recent and on-going research work includes experimental studies on visual object identification and misidentifications, on false memories for visual objects (induced by misidentifications).

Selected Publications

1. Vannucci, M., Mazzoni, G., Marchetti, I., Lavezzini, F. (2012). "It's a hair-dryer. No, it's a drill". Misidentification-related false recognitions in younger and older adults. *Archives of Gerontology and Geriatrics, 54,* 310-316.
2. Vannucci, M., Mazzoni, G., & Cartocci, G. (2011). Lack of control enhances accurate and inaccurate identification responses to degraded visual objects. *Psychonomic Bulletin and Review, 18,* 524-530.
3. Vittori, A., Mazzoni, G., Vannucci, M. (2011). It's a hairbrush…no, it's an artichoke". Misidentification-related false recognitions in younger and older adults. *Perception*, *40*, 126.

2. The Physics and Astronomy Department

Vitaliano Ciulli, Researcher at University of Florence, has graduted in Physics (1993), 110/110 summa cum laude, at Scuola Normale Superiore di Pisa and Università di Pisa and has awarded his Ph.D. in Physics (1997) at Università di Pisa. In the periode Nov 1997 - Dec 1999 he hold a CERN Fellowship in EP Division. He was Research Physicist at Scuola Normale Superiore di Pisa for couple of months (Jan 2000 - Oct 2000), Università di Firenze (Jan 2003- Mar 2003), at the Istituto Nazionale di Fisica Nucleare and since 2005 is Research Physicist at Università di Firenze. His research activity is in the field of particle physics: since 1993, in the ALEPH collaboration at LEP and, since 1997 in the CMS collaboration at the LHC. He contributed to the design, construction and commissioning of the CMS Silicon Strip Tracker, taking a leading role in the development of the software for simulation, data analysis and quality monitoring. He is Team Leader of the Firenze Institute in CMS since 2012. He has more than 400 publications in peer reviewed journals and 15 international conference proceedings.

Selected publications:

1. V. Ciulli, "The CMS Silicon Strip Tracker: from integration to start-up", Proceedings of 10th ICATPP Conference on Astroparticle, Particle, Space Physics, Detectors and Medical Physics Applications, Villa Olmo, Como 8-12 October 2007
2. M. Pioppi et al., "First level trigger using pixel detector for the CMS experiment", Nucl. Inst. Met. A570 (2 SPEC. ISS.), pp. 271-275
3. V. Khachatryan et al. (CMS Collaboration), "CMS tracking performance results from early LHC operation", Eur. Phys. J. C 70, 1165 (2010).

7	PRISMA ELECTRONICS ABEE	PRIELE	EL

PRISMA ELECTRONICS (PRIELE) is an SME with main mission to promote and support the right and effective use of the emerging technologies in the field of Electronics, ICT and Energy. PRIELE has setup a modern technological environment, where technology and know how are the dominant elements, creating the preconditions to develop and support hi-tech innovative applications.

Tasks in the project
PRIELE is leader of WP 6 Dissemination and exploitation, responsible for task 6.2 Exploitation. In addition, PRIELE is contributing to WP3 Board Development, tasks 3.1- 3.4 and it has also a significant contribution in WP4 Test Bench Applications Demonstrations, tasks 4.1-4.3.

Relevant experience
Major activities directly related to the NEURONS project objectives are :
- design of PCB
- assembly of PCB (SMT and THT) as well as integration of devices
- design/setup test environment/kit
- functional testing
- coating, burn in test, isolation and continuity test.

PRIELE staff is highly experienced and trained in complex electronics manufacturing applications. There are 9 ESRs and ERs in the R&D Sector of the Company, which are familiar to handle European projects.

Staff committed to the project
Petros P. Soukoulias, MSc Computer Science, Essex University (UK). Former General Manager (14 years), he is today the President of the Scientific/Advisory Board of PRISMA ELECTRONICS. He has an extensive experience as coordinator in several European and national hi-tech large and medium scale projects.
Serafeim Katsikas, Electrical Engineer. He is member of the BoD and Head of R&D Sector of PRIELE. He graduated at National Technical University of Athens / School of Electrical and Computer Engineering / Faculty of Telecommunications Activities. He is an experienced researcher with more than 10 years' experience. In addition, he is member of the BoD of the Hellenic Semiconductor Industry Association (Hellenic-SIA); Regular attendant in the International Wireless Congress; member of COMADEM (Condition Monitoring and Diagnostic Engineering Management); member of WCEAM (World Congress on Engineering Asset Management); member of Open Group Organization.
Fotis Moschou: Electrical and Computer Engineer, Master degree from Democritus University of Thrace. He is Manager of the Electronics Sector of Prisma Electronics since 2003. His expertise includes PCB assembly, cable harnessing, electronics integration and testing procedures. He has participated in 5 European and national research programs.
Panagiotis Kalaitzidis, Electrical and Computer Engineer. He is currently Production Manager and is highly experienced in carrying out prototypes production and performing tests (functional, Isolation & Continuity and burn in tests) in R&D projects, during the last 7 years.
Konstantina Mermikli, Electrical and Computer Engineer. She is R&D projects manager and is specialized in embedded software development and Testing tools design. She has 3 years experience in testing boards and integrated systems and is familiar with CERN projects.

8	Ruprecht-Karls-Universiät Heidelberg	UHEI	D

The Physics Institute is one of the main institutes of the Faculty for Physics and Astronomy of the University Heidelberg (UHEI), which is engaged in teaching of undergraduate and graduate student and doing research in the field of fundamental physics covering nuclear and particle physics, quantum dynamics and laser physics.

Tasks in the project
UHEI is Leader of WP 5 Design for further integrated system and it is responsible for task 5.3.

Relevant experience and publications
The institute is heavily engaged in high energy experiments at the Large Hadron Collider (ALICE, ATLAS and LHCb) and also contributes to heavy ion physics at GSI.

ASIC design projects:
2000-2003 PreAmpli_erShAper for the ALICE TPC @ LHC
2001-2004 PreAmpliferShAper for the ALICE TRD @ LHC
2005-2006 Wafer testing of the TRD PreAmpli_erShAper
2005-2006 Development of the DETNI chip for CASCADE Neutron Detector
2005-2006 PreAmpliferShAper development of the Fast TRD for the CBM @ FAIR
2007 Development of the N-XYTER for CBM and other FAIR experiments
2006-2007 PreAmpli_erShAper for the PANDA experiment (readout bu_er) @ FAIR
2008 ADC development for the Super ALTRO @ CERN
2009-2010 Engineering run of the N-XYTER for CBM and other FAIR experiments
2010-2011 Associative Memory Design for the FastTrack Processor (FTK) at ATLAS @ LHC
2011-2012 Multi-Gigabit Wireless data transfer at 60 GHz for ATLAS

Relevant publications to NEURONS project:
1. H. K. Soltveit, R. Brenner, A. Schoning and D. Wiedner, \Multi-Gigabit Wireless data transfer at 60 GHz," arXiv:1206.2287 [physics.ins-det].
2. H. K. Soltveit, J. Stachel, P. Braun-Munzinger, L. Musa, H. A. Gustafsson, U. Bonnes, H. Oeschler and L. Osterman et al., \The Preampli_er shaper for the ALICE TPC-Detector," Nucl. Instrum. Meth. A 676 (2012) 106 [arXiv:1203.3564 [physics.ins-det]].
3. A. Annovi, ..., H.K. Soltveit,... et al., \Associative Memory Design for the FastTrack Processor (FTK) at ATLAS," Proceedings of 2011 IEEE Nuclear Science Symposium and Medical Imaging Conference, Valencia, Spain, 23 - 29 Oct 2011.
4. A.S. Brogna, S. Buzzetti, W. Dabrowski, T. Fiutowski, B. Gebauer, M. Klein, C.J. Schmidt, H.K. Soltveit, R. Szczygiel, U. Trunk, \N-XYTER, a CMOS read-out ASIC for high resolution time and amplitude measurements on high rate multi-channel counting mode neutron detectors," Nucl. Instr. Meth. A 568 (2006) 301.
5. H. K. Soltveit, \Preampli_er-shaper prototype for the Fast Transition Detector of the Compressed Baryonic Matter (CBM) experiment at FAIR," Proceedings of the 12th Workshop in electronics for LHC and future experiments.
6. H.K. Soltveit et al., \Development of a test setup for the ALICE TRD PASA," GSI Report 2004. GSI 2005-1.
7. H.K. Soltveit et al., \Final version of the Analog Front-End electronics for ALICE TPC detector and ALICE TRD detector," GSI Report 2003. GSI 2004-1.
8. A.Schöning, for the ATLAS Collaboration, A Self Seeded First Level Track Trigger for ATLAS, JINST 27 P0612 (2012).
9. S.Schmitt and A.Schöning 2010 A Fast Track Trigger for ATLAS at Super-LHC, *JINST* **5** C07013 (2010).
10. A.Schöning, The Fast Track Trigger at the H1 Experiment: Design Concepts and Algorithms, NIM A **566** (2006) 130.
11. A.Schöning, *et al*., A Fast Track Trigger for the H1 Experiment, NIM A **518** (2004) 542.
D.Meer, D.Müller, J.Müller, A.Schöning and C.Wissing, A Multifunctional Processing Board for the Fast Track Trigger of the H1 Experiment, IEEE TNS **49** (2002) 357.
12. A.Baird, A.Schöning, *et al*., A Fast Track Trigger for the H1 Collaboration, NIM A **461** (2001) 461.
13. A.Baird, A.Schöning, *et al*., A Fast High Resolution Track Trigger for the H1 Experiment,
IEEE TNS **48**}(2001) 1276.

Staff committed to the project
André Schöning is Managing Director of the Physics Institute of the University Heidelberg, project leader for the Fast Track Trigger at the H1 experiment from 1999-2007. Since 2009 he is ATLAS group leader. He was involved in two ATLAS upgrade projects: design of a First Level Track Trigger and FTK.
Hans Kristian Soltveit is since 2000 Scientist (ASIC Desinger) at Universitat Heidelberg (Germany).
GSI POSITION: 1999-2000 Grant from City of Bergen (Norway) @ GSI Darmstadt
CAND. SCIENT. Thesis Title "Design av ASIC for signalbehandling for gamma-detektorer" (1999)

9	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	IMEC	B

Europe's largest independent micro-electronics research center, IMEC was founded in 1984 by the Flemish Government and it is one of the largest independent research centers in the world in the field of microelectronics, with an annual budget of over € 300 million € in 2011 and a staff of more than 1800 people. IMEC performs scientific research which runs 3 to 10 years ahead of industrial needs. The most important scientific activities are concentrated on the development of new process technologies for the next generation of chips, optoelectronic components, microsystems, solar cells, sensors… In addition, work is oriented towards new design technologies for electronic systems (such as the design of complete systems on a single chip), with a special focus to telecommunications and multimedia. IMEC performs education and training of experts in the field of microelectronics through its microelectronics training center. Many training courses are organized annually in the field of chip design, process technology and related domains.

Tasks in the project
IMEC is involved in WP2 and WP5 and is responsible for task 2.5 and task 5.2.

Relevant experience
From 1989 until 1995, IMEC was partner of the EU-funded project EUROCHIP. This project was funded by the Commission in order to set up a pan-European service for access to CAD tools and access to low cost prototyping for academics. IMEC was responsible for the access to prototyping in EUROCHIP. From 1995 until now, IMEC is the leading partner of the EU-funded project EUROPRACTICE and is responsible for the ASIC part of the EUROPRACTICE IC Service.

Relevant Tools Available at IMEC: IMEC has numerous CAD tools available for supporting this service: CADENCE, MENTOR GRAPHICS, SYNOPSYS, COVENTOR, etc. The hardware configuration of IMEC mainly consists of Linux-PCs and numerous peripheral devices all networked with Ethernet.

Dr. Carl Das, who has been responsible for the pan-European foundry negotiations and organization of support throughout the entire 20 years of the EUROCHIP and EUROPRACTICE, is the Director of IMEC's ASIC. Technical Support Managers for different IC technologies are L. Laeveren and P. Malisse who have extensive experience of those tasks over the past 15 years.

Staff committed to the project
Dr. ir. Carl Das was born in Diest, Belgium on 13 August 1954. He received the degree of electronic engineer from the Katholieke Universiteit Leuven in 1977. From 1983 until 1985 he was employed at the Katholieke Universiteit Leuven as a logistic engineer and in charge of the set-up of a clean room and prototype line for CMOS technology. Since 1986 he is employed by IMEC in the INVOMEC division where he is in charge of the Multi Project Wafer prototyping service and the analog design group. Within the EUROCHIP program he was chairman of the foundry working group and currently is director of the ASIC Services within IMEC and is heading the EUROPRACTICE IC Service and responsible for the IC fabrication service.
Ing. Danny Lambrichts was born in Sint-Truiden, Belgium on 13 December 1961. He received the degree of Industrial Engineer Electricity, option electronics from the Katholieke Industriële Hogeschool Leuven (GROUP T) in 1985. Since 1986 he has been working at IMEC in the former EUROCHIP and actual EUROPRACTICE project as a support engineer for On-Semi. He was responsible for all test solutions developed within the EUROPRACTICE service where he was the interface between customer, foundry, assembly house and test house. He has been involved in test solution developments, for space, industrial and biomedical applications. Since 2000 he became ASIC Volume production manager. Since 2009 he became team leader of the ASIC volume production team within INVOMEC/SV.
Ing. Tom Raman was born in Dendermonde, Belgium on 27 December 1984. He received the degree of Industrial Engineer Electronics, option design techniques from the University College Ghent (Applied Engineering science) in 2007. Since 2008 he has been working at IMEC in the EUROPRACTICE project as a volume production support engineer in the group of Danny Lambrichts. He is acting as the interface customer, foundry, assembly house and test house. He has been involved in test solution developments, for space, industrial and medical applications.

10	COSTRUZIONI APPARECCHIATURE ELETTRONICHE NUCLEARI C.A.E.N. SPA	CAEN	I

Costruzioni Apparecchiature Elettroniche Nucleari (CAEN) is one of the most important spin-offs of the Italian Nuclear Physics Research Institute, founded in Viareggio (Lucca) in 1979. CAEN (www.caen.it) designs and manufactures sophisticated electronic equipments for nuclear physics research and is today the world's leading companies in the field: there are several hundreds of thousand CAEN Low/High Voltage and data acquisition channels now working in all the most important Nuclear Physics Laboratories over the World.
In the last years CAEN diversified its offer, extending its market, taking part into national and international programs and becoming a real "Innovation Company". In this way CAEN joined to its core business new experiences in new fields such as the UHF Radio frequency identification, the microelectronics, the aerospace applications, biomedicine, and homeland security. CAEN is known today as the a company able to offer, besides a complete range of power supply and data acquisition systems, a large choice of Front-End modules (NIM, CAMAC, VME, VME-64) implemented using ASIC (Application Specific Integrated Circuit).
CAEN portfolio includes today more than 250 products, ranging from power supply systems to data acquisition boards and crates. Its catalogue is printed in 10.000 copies and widespread in all research centres all over the world. Besides catalogue products CAEN offers custom solutions dedicated to the different customers needs, which reach the 40% of the annual production. The quality of its products is monitored during all the production cycle and guaranteed by the UNI EN ISO 9001:2000 certification obtained in 1997.

Tasks in the project
CAEN is mainly involved in WP3 and WP4 and together with other partners is responsible for tasks 3.7 and 4.4. CAEN will be supporting partner in WP 6 Dissemination and Exploitation.

Relevant experience
CAEN has been involved in the design of sophisticated electronic equipment for nuclear and particle physics experiments in the Large Hadrons Collider (LHC) project at CERN (Genève), taking part to the development of the main experiments: CMS, ATLAS, ALICE. Most of the electronic circuits used in these experiments shall work in a very high radiation environment (5 KGauss) with high magnetic fields and quite difficult accessibility.
From the point of view of the Project Management, CAEN was partner in several projects from the European to national and regional level. Some of them are:

- EuriTrack under FP6
- SlimPort under INDUSTRIA 2015 Italian program
- MODES_SNM funded under the FP7 - Security program with the GA 284842 in 2011

Staff committed to the project
Ing. Stefano Petrucci had started his activity in electronics in 1997 as power supply designer for nuclear physics in CAE. In 2000 he became vice-coordinator of the power supply system design for LHC experiment at CERN (Geneva). In 2004 he became the person in charge for the entire power supply system of all the 4 LHC experiments. From 2009 he is the CAEN responsible of regional, national and international funded projects.

11	UNIVERSITY COLLEGE LONDON	UCL	UK

University College London (UCL) is one of the leading European academic institutions and is placed regularly among the top-20 universities worldwide in most international surveys. The High Energy Physics group of the Department of Physics and Astronomy comprises nearly 80 research staff and PhD students, among which 16 faculty members. It has a record of strong involvement and leadership in many particle physics experiments and particular expertise in designing and building triggering and data acquisitions (DAQ) systems and in developing the associated software. The UCL-HEP group have been playing a leading role in the ATLAS experiment, currently with 6 faculty members, 14 research and technical staff and 10 PhD students, and have made major contributions in physics analyses, the detector operation, the offline software, and the Trigger & DAQ systems.

Tasks in the project
WP4, task 4.2 Development of the ATLAS Level-1 Track Trigger system using the Associative Memory chip developed in this project.

Relevant experience
The UCL ATLAS group has had a major involvement in designing and building the Trigger & DAQ systems of ATLAS. It has designed the Timing Interface Module (TIM), which provides the necessary signals to synchronise the data acquisition of the various detector components of ATLAS with the LHC bunch crossing timing. The TIM was originally designed for the silicon tracker, but was subsequently used by most other sub-detectors of ATLAS. The group also had a major role in developing the Readout System software of the experiment and is a key institute in the Level-2 Track Trigger software project.
More recently, UCL has taken a leading role in planning the upgrades of ATLAS in view of the high-luminosity running in the coming 10-20 years. The group has been most prominent in defining the future ATLAS trigger strategy and was the proponent of the Level-1 Track Trigger (L1Track) project, which is now adopted as part of the baseline ATLAS upgrade programme.

Staff committed to the project
Prof. Nikos Konstantinidis is the ATLAS L1Track project co-convenor (and member of the ATLAS Trigger-DAQ project Steering Group) and has been playing a leading role in planning the ATLAS upgrades (as co-convenor of the Phase-I Upgrade Subcommittee and member of the Upgrade Steering Committee). He has been a lead developer of the Level-2 Tracking Trigger algorithms that were used online since the start of data taking in ATLAS and was recently elected as (deputy) leader of the ATLAS-UK project for (2013-16) 2016-19.
Mr Matthew Warren is a senior electronics engineer with significant expertise in electronics for Trigger and DAQ systems in HEP. He was the lead developer of the TIM board for the current ATLAS and the “Trigger & Timing” expert for the current silicon tracker of ATLAS and a key developer of the data acquisition system for the tracker upgrade and the of the L1Track dataflow design.
Mr Gordon Crone is a senior software developer and data acquisition expert with major contributions to the DAQ systems of several major HEP experiments. He was a key developer of the ATLAS Readout System software and have been playing a major role in the feasibility studies for the L1Track system in ATLAS.

12	ASSOCIACAO DO INSTITUTO SUPERIOR TECNICO PARA A INVESTIGACAO E DESENVOLVIMENTO	IST- ID	P

The Association of Instituto Superior Técnico for Research and Development (IST-ID) is a private not-for-profit institution, which primarily aims at carrying out Science and Technology activities, fostering knowledge transfer and promoting the involvement of national and foreign researchers, internally and externally, in RD&I projects in their areas of expertise.

Tasks in the project
IPFN/IST-ID is mainly involved in WP3 and WP4 tasks 3.7 and 4.4.

Relevant experience
The Instituto de Plasmas e Fusão Nuclear (IPFN/IST-ID) is one of the largest RD&I centres out of the 31 that operate at IST-ID. It is the leading institution of the contract of Association EURATOM-IST for fusion development. IPFN/IST-ID has been strongly involved in two thematic areas: (i) Controlled Nuclear Fusion; (ii) Technologies of Plasmas and Ultra-Intense Lasers. The competences of the IPFN/IST-ID staff encompass Microwave/mmWave electronics & very Fast electronics (FPGA, digital circuitry); Microwave/mmWave systems; Diagnostic integration; special component design (non electronics): structural & electromagnetic; simulation of reflectometry experiments; Data processing and automatic analysis including Real time algorithms; Plasma physics. In addition, staff of IPFN/IST-ID staff has expertise in hardware and software developments for control, data acquisition and processing, networking and real-time control. This expertise has been extensively applied on several generations of ISTTOK CODAC system which has been fully developed by IPFN/IST-ID staff.
IPFN/IST-ID has lead or participated in several control and data acquisition projects for JET (TOFOR Data acquisition, Real-Time Control Project, Data acquisition to Gamma-ray spectroscopy, Plasma Control Upgrade – Vertical Stabilisation, Real-Time Test Bench, Fast visible camera) as well as for other machines across EU (ASDEX-Upgrade, TCV, MAST, TJ-II, CASTOR;COMPASS) and Brazil (TCA/BR, ETE). IPFN/IST-ID is presently leading the development of the control and data acquisition system for the ITER prototype Fast Plant System Controller. IPFN/IST-ID has expertise in performing developments for several fusion experiments resulting from work developed in the context of the EURATOM Fusion Programme.

Staff committed to the project (Department: IPFN/IST-ID)
Bruno Miguel Soares Gonçalves, President of IPFN is graduated in Physcis Engineering by Instituto Superior Técnico (1997), has a Master in Physics (IST/UTL, 2000) and a PhD in Physics Engineering (IST/UTL, 2003).
Since May 2012Bruno Soares Gonçalves is the President of IPFN/IST-ID. He is responsible for the Portuguese participation in JET and is Project Leader for the ITER prototype Fast Plant System Controller and Plasma Position Reflectometer projects. He is also member of the European Fusion Development Agreement Seering Committee, member of the Consultative Committee for the EURATOM Specific Research and Training Programme in the Field of Nuclear Energy (Fusion) - CCE-FU, member of the External Advisory Panel to the project European Spalation Source- Bilbao and JET representative at the EIROForum Instrumentation Working Group. He is also invited professor at IST for the course of Management of Science and Technology.
Bernardo B. Carvalho, Assistant Professor at Physics Department. He has expertise in software development and was responsible for ITER FPSC Prototype Project. He was proposer and Project Leader of the EFDA JET EP2 Real-Time Measurement & Control Upgrade [RTM] (2008-2012)
Antonio Batista, Researcher with experience in hardware architectures for fast control and data acquisition systems in nuclear fusion experiments. He is ATCA hardware and firmware developer of the new Plasma Vertical Stabilization system for tokamak JET as well as developer of a new ATCA/AXIe board for fast control and data acquisition systems, used in the ITER beta version of the Fast Plant System Controller prototype.
Ana Fernandes, Full time researcher at IPF IST. Her main expertise is in Control and Data Acquisition Group on the development of FPGA code for ATCA systems and Development of real time processing algorithms for FPGA, applied to gamma-ray spectroscopy.
Rita Costa Pereira, Post-Doc Research Fellow in the Control and Data Acquisition Group of IPFN/IST. She has extensive experience in the design of control and data acquisition modules (VME, PCI, ATCA) and participated in JET-EFDA projects, being the last collaboration the development of a fast data acquisition and processing system based on ATCA for gamma-ray diagnostics at JET.
Jorge Sousa, Head of the IPFN Instrumentation group at IPFN. He was in charge for technical coordination of various JET-EFDA Projects as well as ITER Projects. He has participated in other Control and Data Acquisition Projects in collaboration with various international laboratories. He has a total of 103 published peer-reviewed papers since 1993.

2.3 Consortium as a whole

2.3.1 Adequacy of the consortium to achieve the project objectives

The NEURONS project is formed by a well-balanced consortium composed of 12 partners in which seven from academia, two independent research organizations and three industrial partners (SMEs). The consortium is formed in such a way to guarantee a large impact of the developed AMMA-chip and to demonstrate its potential in several applications such as in salient visual and moving features reconstruction, plasma tomography, and particles detection in the CMS and Atlas detectors at CERN. The research, development, demonstration and dissemination activities needed for achieving the objectives of the NEURONS project require the involvement of experts from a variety of disciplines. The partners of the NEURONS project provide the necessary competences to perform the activities according to the work plan and are carefully selected for achieving the project objectives. The Consortium of the NEURONS project ensures:

- The presence and involvement of leading EU organisations in research and development activities and solid experience in working in European cooperative projects.

- The presence of teams from embedded computing (PRIELE, AUTH, INFN) and teams from high-performance computing (INFN, LPNHE-CNRS, IMEC, UHEI, Microtest) for Exploiting synergies and strengths between the two computing segments that will focus on the Big-data challenge to provide an innovative data-intensive parallel computing platform (AMMA-chip) which is suitable for a wide range of applications.

- The presence of a team representing a group of users of the developed AMMA-chip (UNIFI, UCL, CAEN, IST-ID, INFN) in a diversity of applications.

- The presence of innovative and successful SMEs as essential technology providers for the activities of the NEURONS project.

- A wide European coverage to ensure sufficient level of dissemination of the project results. The consortium is formed by partners from 7 Member States (Italy, France, Germany, Greece, UK, Portugal and Belgium) and 1 Associated Country (Switzerland) with an impressive reaching potential for the dissemination and exploitation of the project results.

- A well-established balance between key actors from academia, research organizations and industry with a proven track record of excellence regarding similar R&D activities of the NEURONS project. The partners are highly experienced in designing and developing high performance and advanced solutions comprising ASICs, firmware, software, electronic boards, advanced packaging, embedded systems, conceptualisation, simulation, design and testing of integrated systems, etc.

2.3.2 Balance of the consortium

The consortium has the right mix of organisations and teams to achieve the project objectives as follows:

Teams of the high performance-computing: Four world class organizations (INFN, LPNHE-CNRS, IMEC and UHEI) and one SME (Microtest) are participating in the project to develop the ASICs.

INFN will be participating with one national laboratory and three departments: INFN Pisa, INFN Laboratori Nazionali di Frascati LNF, INFN Pavia and INFN Milan. The INFN takes part in European scientific computing and nuclear physics projects. It has countless international activities, where some of the most important research is conducted at CERN in Geneva. Fundamental research in these areas requires the use of cutting-edge technologies and instrumentation, which the INFN develops both in its own laboratories and in collaboration with industry. The INFN is a leading national and international player in the Grid Initiative, supercomputing network project and in expanding its use to applications in other scientific fields, e-commerce and culture. The technology and expertise developed by the INFN has major implications in several technological sectors such as medical and healthcare. INFN Pisa and LNF will be participating in the ASIC development.

LPNHE-CNRS has many international collaborations in which many of them are involving high-energy physics such as the Atlas detector at CERN, CDF and D0 at Fermilab (USA), T2K (japan) to name a few. LPNHE has developed outstanding skills in highly diversified physics, electronics, computer science and mechanical fields to support the running projects in high-energy

physics. The Electronics Division of LPNHE will be participating in the NEURONS project and will be providing all the necessary support in chip design and peripheral electronics development.

IMEC is Europe's largest independent micro-electronics research center. The most important scientific activities of IMEC are concentrated on the development of new process technologies for the next generation of chips, optoelectronic components, microsystems, etc. IMEC will be mainly responsible for the multi-packaging design and development.

UHEI: Heidelberg University is Germany's oldest university and has one of the strongest research profiles in all of Europe. The Physics Institute is participating in the NEURONS project and is one of the main institutes of the Faculty for Physics and Astronomy of the University Heidelberg. The institute is engaged in high energy experiments at the Large Hadron Collider (ALICE, ATLAS and LHCb). The institute has been involved in many ASIC design projects over the last decade to support the detection of high –energy particles. Its main role in the project is to investigate the concept design for the 3D AMMA-chip.

Microtest is an innovative and successful SME operating in the field of microelectronics consultancy relating to the design, testing, qualification and industrialization of electronic circuits primarily for use in automotive applications. Microtest has collaboration with leading electronics companies such as ST Microelectronics, Philips, Infineon, Delphi, Denso, Motorola, Bosch and has partnerships with US-based Teradyne. Microtest will mainly provide a concept for massive and fast chip test and develop the test software and provide testing on 500 AMMA-chips for the demonstrators using Microtest machines.

Additionally two world class organizations (**INFN**, **UNIGE**) will bring the AMMA-board to real functionality, providing the mezzanines to test the ASIC as a multicore engine:

The "Département de Physique Nucléaire et Corpusculaire" (DPNC) of the University of Geneva **UNIGE** is participating in the NEURONS project. DPNC has been the founding member of several major international collaborations, including L3, ATLAS, AMS and is one of the leading institutes in particle and astroparticle physics in Switzerland. DPNC-UNIGE has the task of designing and developing the Local Associative Memory Board (LAMB) which will host the AMMA-chips.

INFN Pavia and **INFN Milan and INFN LNF** will be participating in the development of firmware and test setup for the LAMB boards and the test setup for the AMMA-chip.

Team of from embedded computing: This team is formed by one SME (PRIELE) and two academic partners AUTH and INFN:

PRIELE is an innovative SME with modern technological environment and expertise in complex electronics manufacturing applications and capabilities for the design and construction of Electronic Systems. Nine experienced researchers are working at PRIELE in R&D projects. PRIELE will be involved in the firmware and software development for the embedded system, the development of the LAMB board, assembly and test. It will also support the other partners during the demonstration phase.

AUTH is the largest Greek University. Two divisions of The Physics Department are participating in the NEURONS project: Division of Nuclear and Particle Physics and Division of Electronics and Computing. The first one has a long standing involvement in particle physics experiments at CERN and has expertise in Trigger and Data Acquisition (DAQ), specifically in the event building software with multi-threaded C++, and online monitoring of the data collected from the muon detectors. The second one has extensive experience in high speed and low power system level digital design, FPGA programming, algorithm implementation on hardware, testing and firmware development. AUTH is involved in Firmware and software development for the embedded system as well as in demonstration activities.

Group of users of the developed AMMA-chip: the demonstration of the capabilities of the developed AMMA-chip will be performed by a group of users as follows:

UCL is one of the leading European academic institutions and is placed regularly among the top-20 universities worldwide in most international surveys. The High Energy Physics (HEP) group of the Department of Physics and Astronomy is participating in the NEURONS project. The UCL-HEP group have been playing a leading role in the ATLAS experiment at CERN and have made major contributions in physics analyses, the detector operation, the offline software, and the Trigger & DAQ systems. The main demonstration activities that will be carried out by UCL are the development of the pattern recognition for the ATLAS L1Track Trigger application.

UNIFI is one of the largest organizations for research and higher education in Italy. Two distinct departments of UNIFI will participate in the NEURONS project to perform demonstration activities of the capabilities of the AMMA-chip: NEUROFARBA in reconstruction of salient and moving visual features and the Physics and Astronomy Department in reconstruction of CMS events, in collaboration with INFN-Pisa.

CAEN is one of the most important spin-offs of the Italian Nuclear Physics Research Institute. CAEN designs and manufactures sophisticated electronic equipment for nuclear physics research and is today the world's leading companies in the field. CAEN will be supporting IST-ID in performing demonstration of the capabilities of the AMMA-chip in plasma tomography.

IST-ID is a private R&D institution carrying out R&D activities in major areas such as ICT, energy, environment, nuclear reactors etc. The Instituto de Plasmas e Fusão Nuclear (IPFN-IST) is one of the largest RD&I center out of the 31 that operate at IST-ID. IPFN-IST is participating in the NEURONS project with the aim to make demonstration of the capabilities of the developed AMMA-chip in Plasma Tomography image reconstruction for the extraction of salient visual patterns for real-time control in nuclear fusion plasma experiments.

INFN Pisa: Will demonstrate the capabilities of the AMMA-chip in CMS simulation with the development of a track reconstruction based on AM suitable for L1 trigger application, in collaboration with the Physics Department in Florence.

2.3.2 Specific expertise of the partners and relevance to the NEURONS project

The aforementioned partners have been selected according to their unique features, and capabilities to fully achieve the objectives of the NEURONS project. They have been selected in order to take advantage of their complementariness and to facilitate strong synergies among them. The following table provides an overview of the partner's competences and complementarities to carry out their specific role in the project:

Partner	*Role in the project*	*Expertise relevant to the project*
INFN	• INFN will be the **project coordinator** and is in charge of the related management tasks (**WP1**). • INFN will participate in **WP2**. INFN will **lead task 2.1**: Full custom design and flooring of 2D AMMA-chip and simulation, and will **lead task 2.4** test of prototypes. INFN will contribute to all other tasks of WP2. • INFN will participate in **WP3**. INFN will **lead task 3.5**: Single AMMA-chip mezzanine for AMMA-chip tests design and test vector design, and **lead task 3.6**: Firmware for array of AMMA-chip tests and LAMB tests. • INFN will participate in the demonstration activities in **WP4** mainly in **leading task 4.1.** CMS simulation. • In **WP5**, INFN will contribute to **task 5.1**: logic integration, placement & routing & global simulation and to **task 5.2** multipackaging and to **task 5.3** towards a 3D AMMA-chip. • INFN will contribute to **WP6** and will **lead** the dissemination **task 6.1** and participate	The departments of INFN which are participating in the NEURONS project have high experience and expertise to perform the assigned tasks. The teams involved have international collaborations, solid management experience in large projects and worldwide recognition in the domain of embedded-computing and high performance computing. INFN has been involved in about 70 FP7 projects (20 as a coordinator). In the following a selected set of FP7 projects related to the activities of INFN in the NEURONS project: • INFIERI: **Intelligent Fast Interconnected and Efficient Devices for Frontier Exploitation in Research and Industry.** • ITES: **Innovative Tools for Event Selection in high energy physics.** • SLHC-PP: **Preparatory phase of the large hadron collider upgrade.** • ARTLHCFE: **Accurate Real-time Tracking in LHC Full Events.** INFN has a large network in the academia and industry and is part of the National Grid initiative (NGI) which is a part of the European Grid Infrastructure. NGIs are *"legal organizations, supported by governments, and providing a unique representation at the European and international levels for all the communities related to national grid infrastructures: from*

	in the exploitation **task 6.2** and in elaborating the project exit plan in **task 6.3**.	*resources providers to scientific users".*
LPNHE-CNRS	• LPNHE will **lead WP2.** More particularly, LPNHE will **lead task 2.2** Standard cell design of 2D AM and simulation and **lead task 2.3**: integration of full custom and standard cell design, placement and routing, global simulation and tape-out, and will contribute to **task 2.4**. • In **WP5**, LPNHE will **lead task 5.1** in order to provide a placement and routing strategy for a maximum die compatible with the package. • LPNHE will contribute to all the tasks of **WP6**, and will participate in the dissemination the exploitation of the project results.	The LPNHE is equipped with a few ISO7 and ISO8 clean rooms, presently used for the ATLAS and LSST R&D. The Electronics Division of the laboratory has relevant expertise in chip design, based on the 65nm CMOS process, and expertise in peripheral electronics development (FPGA programming, card design and assembly), Cadence for board design and Xilinx, Altera CADs, Tier3 Computing facility.
Microtest	• In **WP2**, Microtest will **lead task 2.6** and **lead task 2.7.** Microtest will mainly develop a concept of test and develop the test software and test the chips for the demonstrators using Microtest machines. • In **WP3,** Microtest will **lead task 3.8** to design and test a small interface board which will be placed between the AMMA-chip and the Microtest machines. • Microtest will participate in all the tasks of **WP6.** It will **lead task 6.3** that will provide an exit plan of the project.	Microtest has strong expertise in the design, testing, qualification and industrialization of electronic circuits and has the ability to provide ready to use solutions to its customers. In the latest years, Microtest has launched four major projects for innovation and R & D as described below: 1) Innovation project in the application concessionary; 2) R & D project "Development of a prototype machine for electronic components Burn In" 3) R & D in the area of 2, 3 and 4-wheel vehicles and components. 4) R & D project entitled “Creation of micro devices”. The project includes the study, design, construction and development of a microelectronic device for integrating multi-function voltage generators and digitizers for different uses including, the main one is in a ATE.
AUTH	• AUTH will **lead WP3** “Board development”. AUTH will **lead task 3.1 and task 3.2** where the firmware and software for the control board will be developed and the acquisition and commissioning of the embedded systems for demonstration will be performed. • AUTH will participate in the demonstration activities in **WP4**. AUTH will participate in **task 4.2** for the Atlas simulation and in **task 4.3** for implementing the simulation algorithms for fast visual motion and silent features reconstruction. • AUTH will participate in the dissemination **task 6.1** and exploitation **task 6.2** of the project results in **WP6.**	The Division of Electronics and Computing is participating in the NEURONS project. It has extensive experience in high speed and low power system level digital design, FPGA programming, algorithm implementation on hardware, testing and firmware development. The group is experienced in hardware design and verification (VHDL) as well as Hardware/Software codesign (EDK Xilinx environment) for the implementation of DSP and computationally intensive image/video processing algorithms. The group has developed in house machine vision applications targeting FPGA devices. Their research also targets ASIC design (Cadence). The ATLAS group of AUTH which is also participating in the NEURONS project had a sizable contribution (over 10%) to the construction of the precision tracking muon chambers of ATLAS. The group has also expertise in Trigger and Data Acquisition (DAQ), specifically in the event building software with multi-threaded C++, and online monitoring of the data collected from the muon detectors. The group has also a leading role in the physics exploitation of the collected data. The group has a very good laboratory infrastructure and access to the Grid facilities of the University.
UNIGE	The main involvement of UNIGE is in **WP3**. UNIGE will **lead task 3.3** to design and	*UNIGE* has a long tradition in the R&D, design and construction of silicon tracking detectors. It has excellent expertise on

	develop the Local Associative Memory Board (LAMB) which will host the AMMA-chips. UNIGE will participate in the dissemination of the project results in **WP6**.	developing electronics for high performance online computation and has developed many similar systems in the past. Currently the DPNC is participating in the vertical slice integration of the FTK into the ATLAS experiment.
UNIFI	• UNIFI will **lead WP4** "Test Bench application and Demonstrations". UNIFI will lead the salient visual features and motion reconstruction demonstration activities **task 4.3**. UNIFI will participate in the dissemination activities in **WP6**.	The UNIFI team participating in the NEURONS project has collaborations throughout the world and a high rate of publications on high impact journals. One of the main collaboration is the participation to the Compact Muon Solenoid Experiment at the CERN Large Hadron Collider with contribution to the design, construction and test of the inner part of the silicon Strip Tracker, the largest ever built. The team has expertise in pattern recognition in information processing systems, information compression in early vision, motion detection by feature tracking, visual imagery, etc.
PRIELE	• In **WP3,** PRIELE is **leading task 3.4** where the LAMB developed by UNIGE will be assembled. PRIELE is also contributing in task 3.1, 3.2 and 3.3. • PRIELE will support the partners involved in the demonstration activities in **WP4** mainly in the CMS and Atlas simulations and the implementation of algorithms for fast visual motion and salient features reconstruction **task 4.1, 4.2 and 4.3.** • PRIELE will **lead WP6** "Dissemination and Exploitation".	PRIELE staff is highly experienced and trained in complex electronics manufacturing applications. The expertise of PRIELE staff encompasses: - design of PCB, - assembly of PCB (SMT and THT) as well as integration of devices, - design/setup test environment/kit - functional testing - coating, burn in test, isolation and continuity test.
UHEI	UHEI is the **leader of WP5**. UHEI will **lead task 5.3** in order to develop a concept design with a cutting-edge technological solution for the 3D AMMA-chip. UHEI will also be involved in dissemination activities in **WP6**.	UHEI has been involved in several ASIC design projects. In the following a selection of projects: • Associative Memory Design for the FastTrack Processor (FTK) at ATLAS at LHC • Multi-Gigabit Wireless data transfer at 60 GHz for ATLAS • Engineering run of the N-XYTER for CBM and other FAIR experiments • ADC development for the Super ALTRO at CERN • PreAmpli_erShAper for the PANDA experiment (readout bu_er) at FAIR • Development of the N-XYTER for CBM and other FAIR experiments • Development of the DETNI chip for CASCADE Neutron Detector • PreAmpli_erShAper for the ALICE TPC at LHC. • Wafer testing of the TRD PreAmpli_erShAper.
IMEC	The main contributions of IMEC are in **WP2** and **WP5**. IMEC will **lead task 2.5** 2D Multipackaging and **lead task 5.2** 2.5D Multipackaging. IMEC will contribute to the dissemination and exploitation activities in **WP6**.	IMEC scientific activities are concentrated on the development of new process technologies for the next generation of chips, microsystems, components and other devices. IMEC is the leading partner of the EU-funded project EUROPRACTICE and is responsible for the ASIC part of the EUROPRACTICE IC Service. EUROPRACTICE offers state-of-the-art design tools as well as an MPW prototyping and packaging service to

		European universities and publicly funded research institutes for microelectronic and microsystem design.
CAEN	CAEN will be mainly involved in WP3 to support IST-ID in the readout setup for plasma tomography application **task 3.7** and in the demonstration activities of the AMMA-chip in **WP4** in plasma tomography **task 4.4**. CAEN will also contribute to the dissemination and exploitation of the project results in **WP6** including the development of an exit plan of the project.	CAEN has been involved in the design of sophisticated electronic equipment for nuclear and particle physics experiments in the Large Hadrons Collider project at CERN, taking part to the development of the main experiments: CMS, ATLAS, ALICE. CAEN offers custom solutions dedicated to the different customer needs. CAEN portfolio includes today more than 250 products, ranging from power supply systems to data acquisition boards and crates. Its catalogue is printed in 10.000 copies and widespread in all research centres all over the world. CAEN has been involved in several EU project such as: • EuriTrack under FP6, • MODES_SNM funded under the FP7.
UCL	UCL will be mainly involved in demonstration activities in **WP4** where it will **lead task 4.2** the Atlas simulation. Besides, UCL will be involved in the dissemination activities in **WP6**.	The UCL ATLAS group has had a major involvement in designing and building the Trigger & DAQ systems of ATLAS. It has designed the Timing Interface Module (TIM), which provides the necessary signals to synchronise the data acquisition of the various detector components of ATLAS with the LHC bunch crossing timing. More recently, UCL has taken a leading role in planning the upgrades of ATLAS in view of the high-luminosity running in the coming 10-20 years.
IST-ID	IST-ID will be **leading task 3.7** in order to develop a readout setup for plasma tomography applications and will be leading the demonstrations activities of plasma tomography in **WP4 task 4.4**. Besides, IST-ID will be participating in the dissemination activities in **WP6**.	IST-ITD has been strongly involved in the area of (i) Controlled Nuclear Fusion and (ii) Technologies of Plasmas and Ultra-Intense Lasers, among other areas. The competences of the IPFN-IST staff encompass Microwave/mmWave electronics & very Fast electronics (FPGA, digital circuitry); Microwave/mmWave systems; Diagnostic integration; special component design (non electronics): structural & electromagnetic; simulation of reflectometry experiments; Data processing and automatic analysis including Real time algorithms; Plasma physics. In addition, the IPFN-IST staff has also expertise in hardware and software developments for control, data acquisition and processing, networking and real-time control.

i) **Sub-contracting:** The only subcontracting activities in the project are related to the establishment of a project website and audit reports.

ii) **Other countries:** None.

2.4 Resources to be committed

The overall costs required for the implementation of the NEURONS project are **€4,235,745** with a requested EU contribution of **€3,099,968**. It's worth mentioning that all partners have understood the rules of the Commission relating to budget allocation and have agreed to the proposed budget. All parties have agreed on the project work and cost shares and are well prepared to support financially their self-funded shares with own resources. All parties have secured the required financial own resources to be invested in the development of this project. The project will last for 36 months. The total project investment has been broken down into 3 major activities: Research, Demonstration, Management (MGT). It's worth mentioning that the management category encompasses the costs of management and coordination of the project, and the costs of dissemination and exploitation of the project results. Figure 2.4.1.a shows the project cost breakdown per activity.

The costs have been carefully distributed over the different activities in order to achieve the project objectives and to guarantee high impact of the developed solutions. 60% of the project costs are related to research, while 24% are dedicated to demonstration activities. The cost of management activities related to project management and coordination is 7% which is reasonable considering the high number of partners involved (12 partners). The cost of other Management activities related to dissemination and exploitation of the project results is 9% and is meant to guarantee sufficient dissemination and exploitation of the project results.
The budget of each activity has been broken down into 5 different cost categories: personnel; subcontracting, travel, consumables and indirect costs (overheads). Table 2.4.1. shows the budget breakdown per partner, activities and cost categories. Figure 2.4.1.b shows the percentage of the overall costs per category. In the following a detailed description of the costs of each category:

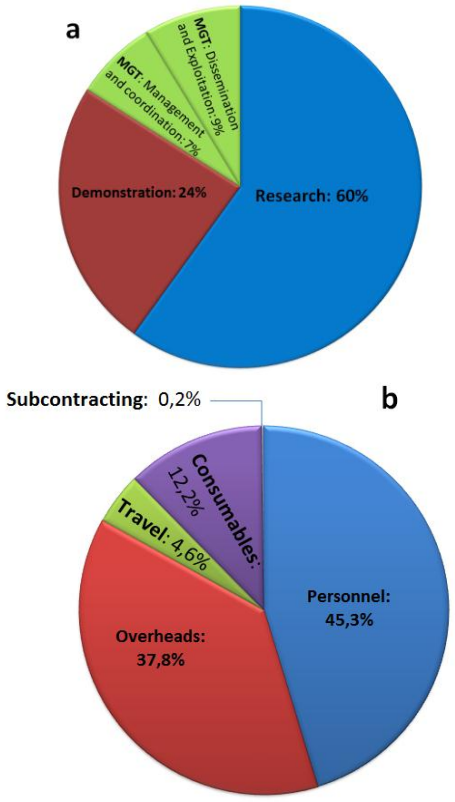


Fig.2.4.1: a) Cost breakdown per activity, b) Cost breakdown per category.

Personnel costs:

The overall personnel costs amount to **€1,919,097.** These have been calculated taking into account the anticipated effort and staff category costs of each partner. The calculation of the budget has been determined by clearly identifying the responsibility for all tasks at the proposal stage of the project. Manpower has been allocated at task level to enable an accurate forecast of costs and to facilitate project management by allowing accurate verification of the contributions of partners with respect to expected results. The requested EC funding for personnel costs is **€1,360,475** and was calculated according to the rule of the Commission taking into account the type of activity and organisation.

Subcontracting costs:

The subcontracting costs amounts to **€8,000** *as follows:*

- €5,000 costs of audit certificates for partners requesting more than €375,000 from the EC (INFN and CNRS).
- €3,000 costs to establish a website for the project.

Travel costs:

The total travel costs amount to **€193,000** and have been estimated according to the number of travels necessary to perform the different activities: €72,000 (6,000€ per partner) travel costs for management activities (kick-off

meeting, consortium meetings, coordination activities), €38,000 travel costs for dissemination and exploitation activities (€4,000 for 6 partners who are heavily involved in the dissemination and exploitation and €2,000 per partner for the other partners), €71,000 travel costs for research activities (travel costs of the researchers involved in the ASIC and Board development and the design for further integrated system), €12,000 travel costs of the researchers involved in demonstration activities.

Consumables:

The costs of consumables amount to **€516,000** and are meant for research activities as follows:

1- 145,000€: €40, 000 wafers cost to produce chips for the demonstrator, €10,000 costs of material for the single chip mezzanine (PCB, assembly, socket), €40,000 costs for the AMMA-chip package tooling, €40,000 packages costs and €25,000 cost of tests before packaging.
2- €250,000 cost for the production of the multi-project wafer (MPW).
3- €25,000 costs of the board with zif socket.
4- €40,000 costs for the evaluation board.
5- €10,000 costs for PCB production.
6- €10,000 costs for LAMB assembly
7- €36,000 cost of CAD rent.

Other indirect costs (overheads): The overall indirect costs amount to **€1,599,648.**

		INFN	CNRS	Microtest	AUTH	UNIGE	UNIFI	PRIELE	UHEI	IMEC	CAEN	UCL	IST-ID	Total
BUDGET RTD activities														
Personnel		183.018	127.224	173.760	42.855	116.870	0	79.500	105.436	74.000	16.000	0	65.070	**983.733**
Subcontracting														**0**
Other direct costs	Travel	8.000	8.000	4.000	8.000	4.000		8.000	8.000	15.000	4.000		4.000	**71.000**
	Consumables	145.000	250.000	25.000	40.000	10.000		10.000		36.000				**516.000**
	Durable Equipement													**0**
	Other													**0**
Total other direct costs		153.000	258.000	29.000	48.000	14.000	0	18.000	8.000	51.000	4.000	0	4.000	**587.000**
Indirect Costs		201.611	231.134	121.656	54.513	78.522	0	58.500	106.491	62.900	12.000	0	41.442	**968.769**
Total eligible RTD Costs		**537.629**	**616.358**	**324.416**	**145.368**	**209.392**	**0**	**156.000**	**219.927**	**187.900**	**32.000**	**0**	**110.512**	**2.539.502**
Required EU funding for RTD		**403.222**	**462.269**	**243.312**	**109.026**	**157.044**	**0**	**117.000**	**164.945**	**140.925**	**24.000**	**0**	**82.884**	**1.904.627**
BUDGET Demonstration activities														
Personnel		116.466	0	0	42.855	0	167.656	27.000	0	0	24.000	175.100	72.300	**625.377**
Subcontracting														**0**
Other direct costs	Travel						8.000					4.000		**12.000**
	Consumables													**0**
	Durable Equipement													**0**
	Other													**0**
Total other direct costs		0	0	0	0	0	8.000	0	0	0	0	4.000	0	**12.000**
Indirect Costs		69.880	0	0	25.713	0	105.394	16.200	0	0	14.400	107.460	43.380	**382.426**
Total eligible Demonstration Costs		**186.346**	**0**	**0**	**68.568**	**0**	**281.050**	**43.200**	**0**	**0**	**38.400**	**286.560**	**115.680**	**1.019.803**
Required EU funding for DEMO		**93.173**	**0**	**0**	**34.284**	**0**	**140.525**	**21.600**	**0**	**0**	**19.200**	**143.280**	**57.840**	**509.902**
BUDGET Management activities														
Personnel		127.558	13.392	57.920	8.571	17.531	8.824	24.000	10.544	18.500	10.000	7.725	5.423	**309.987**
Subcontracting		5.500	2.500											**8.000**
Other direct costs	Travel	10.000	10.000	10.000	10.000	8.000	8.000	10.000	10.000	8.000	10.000	8.000	8.000	**110.000**
														0
														0
	Other													**0**
Total other direct costs		10.000	10.000	10.000	10.000	8.000	8.000	10.000	10.000	8.000	10.000	8.000	8.000	**110.000**
Indirect Costs		82.535	14.035	40.752	11.143	15.318	10.094	20.400	8.962	15.725	12.000	9.435	8.054	**248.453**
Total eligible Management Costs		**225.593**	**39.927**	**108.672**	**29.714**	**40.849**	**26.918**	**54.400**	**29.506**	**42.225**	**32.000**	**25.160**	**21.476**	**676.440**
Required EU funding for Management		**225.593**	**39.927**	**108.672**	**29.714**	**40.849**	**26.918**	**54.400**	**29.506**	**42.225**	**32.000**	**25.160**	**21.476**	**676.440**

Overall Budget	INFN	CNRS	Microtest	AUTH	UNIGE	UNIFI	PRIELE	UHEI	IMEC	CAEN	UCL	IST-ID	Total
Total project costs	**949.567**	**656.286**	**433.088**	**243.650**	**250.241**	**307.968**	**253.600**	**249.433**	**230.125**	**102.400**	**311.720**	**247.668**	**4.235.745**
Total requested EC funding	**721.987**	**502.196**	**351.984**	**173.024**	**197.893**	**167.443**	**193.000**	**194.451**	**183.150**	**75.200**	**168.440**	**162.200**	**3.090.968**

Table 2.4.1: Breakdown of the project costs per activity, category and partner.

Section 3. Impact

3.1 Expected impacts listed in the work programme

3.1.1. NEURONS: Impact according to Work Programme

The following table 3.1.1. summarizes the foreseen impacts of the NEURONS project with respect to the ones contemplated in the Work Programme.

Work Programme foreseen Impact	NEURONS project contribution
Reinforced competitiveness of European technology suppliers across the computing spectrum; in particular for data-centre servers with two orders of magnitude improvements in total cost of ownership and energy efficiency.	The NEURONS project constitutes a unique opportunity for the SMEs involved to act not only as standard technology suppliers but also to acquire new skills and knowledge in developing breakthrough components for novel computing architectures. The miniaturization towards 65 nm technology node will certainly constitute a challenging objective that will help to increase the "know-how" of technology suppliers as well as the development of critical elements of the AMMA-chip such as multi-packaging, characterization, board development, etc. The foreseen activities associated to design of 2.5D and 3D architectures will allow for the development of innovative processing alternatives (i.e. interconnect by using Through Silicon Vias (TSVs), heterogeneous integration, low power, etc) with the opportunity to secure critical IP and know-how. The customized algorithms developed for the application of the AMMA-chip towards massive data parallel processing (i.e. medical imaging, pattern recognition, computer vision, etc) and tackling the Data Deluge challenge will certainly open up new avenues for hardware architectures and software algorithms dedicated to optimize the information transmission and processing, a critical factor that can directly benefit data centres and suppose a straightforward impact in terms of optimizing running costs and achieve better energy efficiency. Moreover future datacentre designs require a hand-in-hand collaboration of software and hardware to provide both energy and thermal management especially for future 3D-stacked server chips. The NEURON project proposes novel 2.5D and 3D architectures that certainly contribute to tackle these challenges.
Reinforced European technological leadership and industrial competitiveness in the design, operations, and control of embedded systems with mixed criticalities and SoS.	The hardware architectures and software algorithms developed in the NEURONS project as well as the foreseen demonstrations open up new breakthrough avenues in the design, operations, and control of embedded systems requiring the control of mixed criticalities (i.e. SoS). The high performance capabilities of the NEURONS project specially the ones associated with the parallel processing of massive data (i.e. dynamic image processing) are directly applicable for example to digital control systems in the automotive and avionics domain, process control systems for any kinds of industrial plants (e.g., automated manufacturing) as well as devices and technologies employed for health care (e.g., medical imaging, control and efficiency of drug delivery, patient monitoring systems, dynamic and real time diagnostics, etc). The NEURONS project will allow reinforcing European leadership in key markets such as automotive, aerospace,

	manufacturing and building automation, smart cities, health care, etc in which breakthrough applications will come out of innovative embedded computing systems with superior performance with respect to (real time) integration and processing of heterogeneous data. Certainly the realization of NEURONS and the IP and/or publications that can derive from it will contribute to position Europe at the leading forefront in emerging areas such as for example Big Data as well as to pioneer the pathways towards revolutionary computation paradigms such as cognitive computers and intelligent decision systems.
Improved systems characteristics: energy/cost efficiency, controlling dynamic and emergent behaviour, managing different criticality levels, security, safety, degree of integration in generic architectures and platforms.	The computing system developed by NEURONS constitutes a breakthrough in the field of Associative Memories and therefore opens the way towards massive data processing in areas where solutions are on high need (i.e. image processing, multimedia databases, etc) but as well in many application fields in which SoS is the future route to be followed and that depend also on managing the Big Data challenge (i.e. climate modelling, cybersecurity, emergency protocols, etc). The NEURONS technology massive parallel computing capacity paves the way to control the different SoS criticality levels and study emergent behaviour (i.e. one of the NEURONS computing pipeline elements is a series of FPGAs that actually acts as a Neural network that can be trained). In summary the impact that the NEURONS technology will achieve are (a) maximum parallelism exploitation, (b) low power consumption coupled to cost efficiency, (c) execution times at least 1000 time shorter than the best commercial Control Processing Units (CPUs) performing the same task, d) distributed debugging and monitoring tools suited for a pipelined, highly parallelized structure, high degree of configurability to face with the best efficiency different applications.
Increased take-up of European computing technologies in industry, in particular SMEs.	The NEURONS project foresees demonstration scenarios that will have a direct impact on taking European computing technologies to industry especially in those areas where Big Data is generated such as industrial processes, health care management, etc. The role of SMEs in the NEURONS consortium if crucial to develop the novel technologies envisioned so they immediately will be acquiring a market competitive advantage. They will be also benefitted by working with cutting edge academic partners in forefront fields of embedded computing and high-performance computing. The academic partners themselves and especially through the dissemination and exploitation plan of NEURONS will have a high exposure towards the European Industrial community which will enhance future academia-industry relationships and therefore foster faster technology transfer pathways.
More efficient application software development by breaking the dependence on dual expertise for application development and customisation for advanced computing systems.	The technology developed in the NEURONS project constitute an interdisciplinary effort of industrial and academic experts in the fields of embedded computing and high-performance computing therefore constituting a key example of synergy towards avoiding the need of dual expertise. Software development is an integral part of NEURONS especially in the foreseen demonstration of data massive processing (i.e. image

	processing, computer vision, high energy physics and nuclear physics pattern recognition, etc) and will be elaborate on the basis of the interdisciplinary expertise of the whole consortium. A similar reasoning applies to the hardware testing methodologies that will be developed (i.e. test vectors and tests of AMMA-chips, etc). All these aspects will allow streamlining application software development in customized advanced computing systems.

Table 3.1.1. Correspondence of the impacts of NEURONS with the ones foreseen by the Work programme.

3.1.1.1 Impact towards European innovation and industrial competitiveness

Every day we rely on the functionalities of embedded systems as for example aircraft control, the braking control in our cars or the control systems used in our railway systems. The capacity to process in parallel and in real time massive amounts of unstructured data especially coming from images/video will be key in the nearby and long term future in order to empower with breakthrough functionalities embedded computing systems in command of many critical functions ruling our lives (Fig. 3.1.1.).

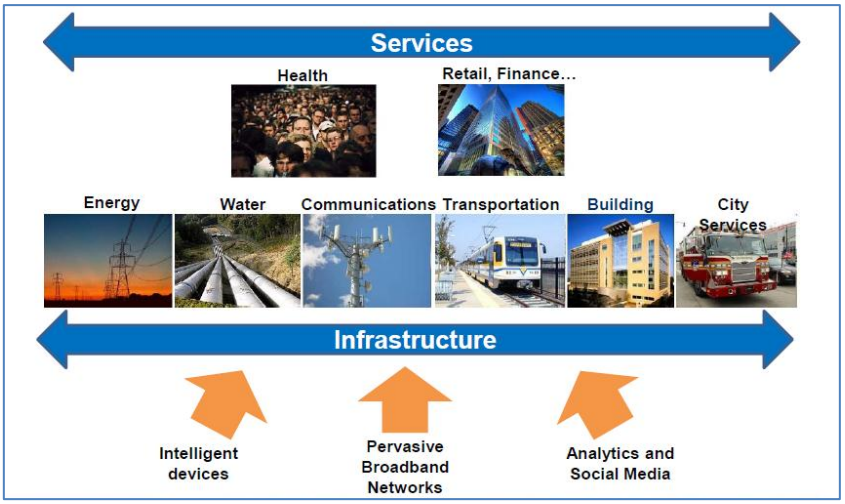


Fig. 3.1.1. The NEURONS project can contribute to the next generation of embedded computing systems (i.e. System of Systems) in which massive data processing becomes a must to be able to deal with mixed criticalities associated to societal challenges[47].

The NEURONS project opens the possibility through its parallel data processing capabilities to impact in areas such as automotive and aerospace in which driver, operator or passenger services and interaction are redefining product innovation to compete in a globalised market, e.g. through advanced driver assistance, automatic cruise control, autonomous driving or smart collaborative interfaces. More specifically, the driver or passenger real life experience combined with virtual, augmented services is considered one of the most challenging differentiating factors that would transfer cars, aircraft, trains et al into smart personalised comfortable spaces. The European leadership exercised today will not be possible to be held tomorrow unless breakthrough advances combining embedded computation with high performance one are made. The NEURONS project constitutes a unique endeavour that not only will develop new parallel computing architectures for massive and parallel data processing but also will open up the way in demonstrating the capacity of those in critical areas affecting the forefront of European Industry.

The NEURONS project will also set up the basis to boost the European industry of 3D Medical Imaging providing it with innovative hardware and software platforms capable to process in real time different heterogeneous images, classify them according to critical features and effectuate dynamical diagnostics; It is necessary to remember that Europe represents the largest regional market in 3D Medical Imaging, although the US constitutes the single largest market globally[48]. The escalating usage of MRI, CT, and ultrasound imaging has fuelled growth of the European market for 3D medical imaging market. In

[47] Design of Future Embedded Systems Toward System of Systems, International Data Corporation (IDC) Report for the EC, May 2012.
[48] Global Industry Analysts, Inc. Report. http://www.prweb.com/releases/3D_medical_imaging/ Global 3D Medical Imaging Market to Reach US$5.9 Billion by 2017, According to a New Report by Global Industry Analysts, Inc.2012.

Europe, the 3D imaging segment has expanded over the recent years as applications became increasingly affordable. The NEURONS project situates in the forefront of providing new avenues towards the increasing popularity for 3D as a tool for rapid diagnosis that is capable of tackling large amounts of medical data produced daily in hospitals across Europe, resulting in enhanced workflow efficiency and patient benefit.

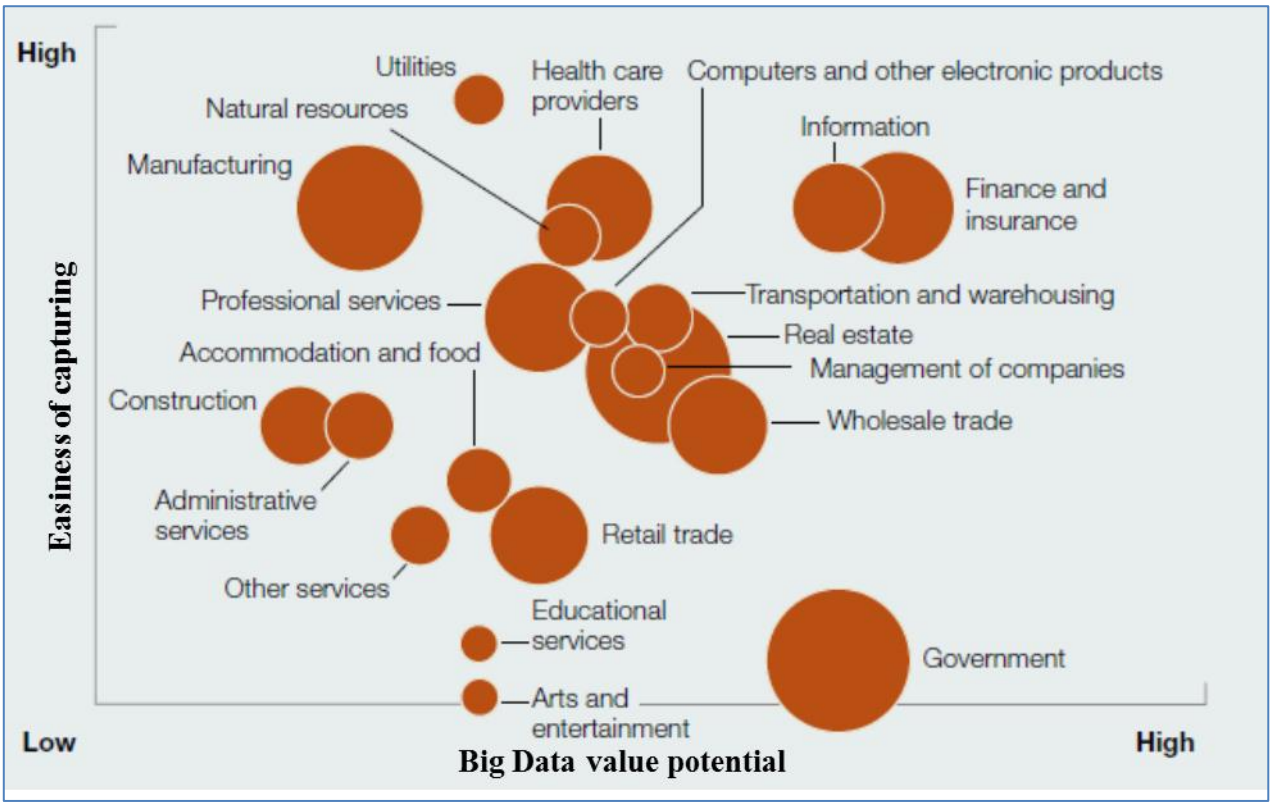


Fig. 3.1.2. The technology developed in the NEURON project will open up breakthrough avenues to capture the value of Big Data across different sectors[49]. Example based on US Economy. Bubble size shows relative contribution to GDP.

It is also important to emphasize once more the impact that the new parallel technologies for data processing develop by NEURONS will have in positioning Europe at the forefront of benefiting from the so-called Big Data Challenge (Fig. 3.1.2.). The foreseen demonstration scenarios for the NEURONS technology allow establishing novel avenues to treat and process the types of data generated and stored (i.e. video, images, audio, or text/numeric information) and its idiosyncratic nature across different sectors seeking for new added informational value that translates into new applications, products and markets.. For instance, financial services, administrative parts of government, and retail and wholesale all generate significant amounts of text and numerical data including customer data, transaction information, and mathematical modeling and simulations. Other sectors such as manufacturing, health care, and communications and media are responsible for higher percentages of multimedia data. Manufacturing generates a great deal of text and numerical data in its production processes, but R&D and engineering functions in many manufacturing subsectors are heavy users of image data used in design.

Finally it is extremely important to mention the benefits that NEURONS will report towards fundamental and applied scientific fields on the need to process massive amounts of data such as for example, high energy physics, fusion technology, astrophysics, climate models, genomics, proteomics, etc. Certainly the capabilities foreseen by the breakthrough advances of NEURONS could constitute the seed for cutting edge advances in Europe and it is in many cases directly linked to the development and future strategy associated with unique European Research Infrastructures.

3.1.1.2 European dimension of the project and connection with key European strategies and initiatives

The interdisciplinary and cross-fertilization aspects and impact of the NEURONS project have with no doubt a pan-European and global footprint not possible to be realized only at a national scale. The realization of a project like NEURONS depends on

[49] Source: MacKinsey report: Are you ready for the era of 'big data'? https://www.mckinseyquarterly.com/Are_you_ready_for_the_era_of_big_data_2864_2011). Example based on US Economy. Bubble size shows relative contribution to GDP.

a combined and synergetic effort of European key players in the area of embedded computing systems and high performance computing only possible and accessible through European funding frameworks. NEURONS as well connects and contributes directly with main key European initiatives as illustrated in the following table (Table 3.1.2):

Key European Initiative	**NEURONS connection (example)**
Europe 2020 strategy[50].	Certainly the impact of NEURONS will translate into the development of advanced computing platforms and paradigms implemented in embedded and control Systems which will constitute powerful enablers to applications oriented to more efficient management of energy and resources.
Digital Agenda for Europe[51]	NEURONS seeks the applicability of forefront massive parallel data processing technologies into marketable products and services across multifold domains ranging from medical imaging towards industrial manufacturing aiming to maintain Europe's competitive edge especially in the next generation of computing technologies.
Innovation Union[52]	The NEURONS computing architectures constitutes certainly an opportunity for interested stakeholders (especially SMEs) of turning ideas into jobs, growth and social entrepreneurship and progress.
Resource efficient Europe[53]	The NEURONS project constitutes a proactive initiative that develops novel computing technologies becoming fundamental components of intelligent systems supporting the shift towards a resource-efficient, low-carbon economy to achieve sustainable growth.
Industrial Policy for the Globalisation Era[54] A European strategy for Key Enabling Technologies – A bridge to growth and jobs[55]	NEURONS develops breakthrough ICT-based key enabling technologies to provide the basis for a wide variety of new processes and goods and services, including the development of entirely new industries over the next decade and contributing that Europe strengthens its leading position in scientific research and innovation.
Agenda for new skills and jobs[56]	The NEURONS project constitutes a first-hand opportunity for SMEs and micro-enterprises, for discovering innovative solutions to respond to social demands providing specific new employment opportunities.

Table 3.1.2. Connections of the NEURONS project with major European strategic initiatives.

Finally it is extremely important to framework NEURONS as a complementarity project in relationship to other EU ones in curse in the area of Advanced Computing, Embedded and Control Systems and related areas. In such a context the NEURONS project focuses on the development and implementation of technologies specially in relation to parallel massive data computing applicable to SoS which is in clear complementarity for example with initiatives such as DANSE (focused Designing for Adaptability and evolutioN in SoS Engineering) COMPASS (Comprehensive Modelling for Advanced SoS) and/or DESTECS (Design Support and Tooling for Embedded Control Software). The findings and developments of NEURONS will also contribute to the elaboration of road mapping projects such as T-Area SoS and Road2SoS as well as constitute a reference project for eventually a roadmap in SoS for still unexplored areas such as health care, industrial manufacturing, etc.

[50] EUROPE 2020: A strategy for smart, sustainable and inclusive growth, EC Communication. Brussels, 3.3.2010 COM (2010) 2020 final.
[51] A Digital Agenda for Europe, EC Communication Brussels, 26.8.2010 COM(2010) 245 final/2.
[52] Innovation Union, EC Communication Brussels, 6.10.2010 COM(2010) 546 final.
[53] A resource-efficient Europe, EC Communication Brussels, 26.1.2011 COM(2011) 21.
[54] An Integrated Industrial Policy for the Globalisation Era Putting Competitiveness and Sustainability at Centre Stage, EC Communication Brussels, COM(2010) 614.
[55] 'A European strategy for Key Enabling Technologies – A bridge to growth and jobs' EC COM(2012) 341 final.
[56] An Agenda for new skills and jobs: A European contribution towards full employment, EC Communication Strasbourg, 23.11.2010 COM (2010) 682 final.

3.2 Dissemination and/or exploitation of project results, and management of intellectual property

3.2.1. Dissemination of results and relevant audiences

The main mechanisms that the NEURONS project foresees are:

- Elaboration of a project website in which not only the European ICT community at large but other relevant communities (i.e. medical area, financial area, complex systems modeling, industrial data management, neuroscience area, etc) and the general public will be able to get up-to-date results related to the project achievements and project dissemination actions (i.e. presentations by consortium members, etc) across the project duration. The website will also contain any relevant downloadable dissemination materials produced by the project (i.e. leaflets, newsletters, demo-videos, etc). The website will also constitute a living, interactive platform, in which stakeholders can offer input (i.e. documentation materials, announcement of relevant events, results of relevant initiatives, etc).

- Participation (and publication of articles in peered reviewed international journals) of the Consortium members in key events and/or conferences such as IEEE International Electron Devices Meeting (IEDM), International Conference on Computer Medical Applications (ICCMA), SC - International Conference for High Performance Computing, Networking, Storage and Analysis, IEEE High Performance Extreme Computing Conference (HPEC), International Symposium on VLSI Technology, Systems and Application (VLSI-TSA), International Conference on Information Communication and Embedded Systems (ICICES), International Conference on Emerging Applications of Information Technology (EAIT), ACM International Conference on Computer Applications, ACM Workshops on Architectures and Systems for Big Data, Annual conference of the Visual Science Society, European Conference of Visual Perception ,etc.

- Organization of dedicated project workshops/webinars (i.e. medical imaging workshops, embedded computing, etc) intending the dissemination of the project results, the expansion of the project network as well as gathering and incorporating valuable input of all stakeholders as well as facilitating the uptake of the project results. In this sense it is necessary to emphasize that several consortium members are part of the large team behind the development of the ATLAS and CMS detectors at CERN so the NEURONS project results will benefit with the large and widely international audience that this entails and the dedicated seminars to associated technology that is developed for that purposes. Also the project results will be disseminated to the Health and Medical Physics community operating at CERN.

- Establishment of direct connection with relevant European actors and initiatives such as European Technology Platforms (ETPs) and Joint Technology Initiatives (JTIs) (i.e. EPoSS - The European Technology Platform on Smart Systems Integration, JTI ARTEMIS on Embedded Systems, ETP Manufuture Future Manufacturing Technologies), Industrial Sector Organizations, SME clusters, standardization bodies, etc).

- Given the future applications in terms of Big Data that the NEURONS projects opens it will be considered the establishment of direct connection with different EU initiatives that will welcome solutions for massive data processing such as such as the Virtual Physiological Human Network of Excellence, European Climate Change Programme (ECCP), Global Monitoring for Environment and Security (GMES), PRACE the Partnership for Advanced Computing in Europe, Galileo European global navigation satellite system (GNSS), Europeana Foundation, etc.

- It is also necessary to mention that due to the benefits that the NEURONS project will entail in relation to Big Data Processing hardware equipment it will be contemplated to establish contact with representatives of Large European Research Infrastructures (i.e. EIROFORUM) that are on the need of the advances that the NEURONS project will provide such as European Molecular Biology Laboratory (EMBL), European Space Agency (ESA), DArIAH The Digital Research Infrastructure for the Arts and Humanities, eMSo European Multidisciplinary Seafloor Observatory, Euro-Argo Global Ocean Observing Infrastructure, eccSeL European Carbon Dioxide Capture and Storage Laboratory Infrastructure, etc.

The NEURONS project will also foresee the possibility to use, in collaboration with the EC, dissemination channels such as:

- **The Research EU magazine** to potentially reach a wide audience since it has a circulation of over 80 000 copies – and a readership of almost ten times that.
- **The Research website on EUROPA** – the European Union's web portal that allows to connect massively across EU and outside (i.e. over the first eight months of 2003, the site averaged 1.25 million hits per month).

- **CORDIS Wire**, as a platform available to submit press releases taking advantage that those can be available for downloading by journalists and other interested readers.

Additionally the NEURONS project will consider the use of more generally available dissemination platforms of free use such as:

- **AlphaGalileo** as a non-profit leading website resource for European research news and offering the possibility to disseminate results in a fast and fast and effective way to communicate with journalists around the world.
- **ECSITE (European Collaborative for Science, Industry and Technology Exhibitions)** is a European network of museums, science centers and other organisations involved in science communication to a wide public. Covering over 35 countries, it promotes the exchange of experience and novel ideas.
- **Research-TV** which potentially can offer the possibility to produces ten-minute video news releases distributed to over 2 000 broadcasters worldwide.

Besides it should be emphasized the direct possibility to disseminate the project in the high traffic websites of the ATLAS and CMS detectors at CERN, the e-bulletins such as ATLAS e-news, CERN bulletin, etc.

Among the relevant audiences that the project NEURONS foresees it is necessary to mention specially the following ones:

- European ICT community at large (i.e. Enterprises, SMEs, RTOs, Academia, European Technology platforms, Join Technology Initiatives, etc) especially the one closely linked to embedded computing and high-performance computing, cloud applications, etc.
- European Research Area scientific and industrial community closely following the research, advances and commercial opportunities that Big Data will bring in different areas..
- European Medical Imaging community at large especially emphasizing on cancer detection, Alzheimer, Parkinson, etc and including not only pure research institutions but also Hospitals, Foundations, etc.
- European scientific and industrial community directly involved in the development of Large European Research Infrastructures and especially the ones seeking for highly parallel data computing capacity.
- European Semiconductor Manufacturing Industry (i.e. devices, systems, components, etc).
- European Software developing community at large.

The NEURONS project will take special care during the elaboration of dissemination material to address specifically those interest communities by tailoring the messages of relevant project results and their linkage with the strategic interests of those communities.

3.2.2. Management of Intellectual Property and Exploitation of Project Results

The Consortium participants will ensure a proper covering of any issues concerning IP access rights (background and foreground) by the Consortium agreement and Grant Agreement. Reviewing of access rights conditions will be also a fundamental point in the project kick-off meeting agenda. All partners will reveal at the outset any knowledge, technical devices and technologies (background) that they hold that is relevant to the execution of the project. Access rights to background for implementing the project will be granted on a royalty-free basis, unless otherwise agreed by all participants before acceding to (or signing in case of the coordinator) the Grant Agreement. The consortium will ensure that any special access conditions if existing are not left open, so as to avoid unforeseen circumstances arising later. Therefore the covering of such aspects will be contemplated in the consortium agreement. Alternatively or in addition, right access might be the subject of specific arrangements between the participants concerned if applicable. IP arising from the project will be patented by the responsible partners and exploited. The following table 3.2.1 resumes the general principles to be applicable for an efficient management of IP that the NEURONS project will contemplate.

	Access to background	Access to foreground
Project implementation	Royalty-free, unless otherwise agreed before acceding to the Grant Agreement.	Royalty-free
Use of results (exploitation or further research)	Royalty-free, or on fair and reasonable conditions	Royalty-free, or on fair and reasonable conditions.

Table 3.2.1. IP management summary principles considered by the NEURON project.

Due to the highly collaborative nature of the NEURONS project and the close interlock of the work packages it is expected that results leading to IP and/or copyrights, etc will be obtained by more than one partner. IP resulting from the RTD activities of NEURONS will be shared on the basis of the inventive steps performed by the individual partners and will mention the FP7 program as a funding source. For foreground which is jointly developed by two or more partners *Joint-Ownerships-Agreements* will be established. Costs arising through filing and maintenance will be shared on the basis of the ownership shares. **Access rights to background and IP necessary for implementing the project, will be granted on a royalty-free basis until the end of NEURONS,** unless otherwise agreed by all participants before acceding to the Grant Agreement. The NEURONS project has also set-up the required project management structure and decision mechanisms to solve efficiently any potential issue related to IP access rights. It is necessary to mention here that in the case that out licensing possibilities are a viable exploitation route (i.e. software), special measures will be taken in reference to the out licensing process of the IP such as negotiation of beneficial out licensing conditions for the parties owning the critical IP, establishment of beneficial contractual. In this respect the NEURONS project work package structure has defined a fully dedicated work package only focusing in project dissemination and exploitation whose main mission besides a thorough dissemination of the project results is the development of a detailed project exploitation plan counting with the collaboration of all the consortium partners. In this sense the focus on exploitation is ensured with respect to its execution and common agreement. The NEURONS project foresees the development of a tailored Exploitation Plan with the following general objectives:

- To ensure wide dissemination of the results of the project to the different interested parties targeting the identification of good practice and avoid barriers for technological further development.
- To investigate and search on potential exploitation pathways and actors and business models for the results of the project and safeguard the process of exploitation of such results.

The plan starts with a market analysis including the identification and evaluation of existing solutions and services as well as analysis of the factors that would influence the exploitation of the project results. Based on the course of the project and the achieved results, potential opportunities and actors for exploitation will be identified and specific rules for exploitation will be defined and updated in a continuous basis. The exploitation plan will contain as well commonly agreed Key Performance Indicators (i.e. publications, filed patents, contacted stakeholders, etc) that will allow for a close monitoring as well as then implementation of additional measures if necessary to ensure the best exploitation of results. Exploitation activities of the NEURONS consortium will take several forms to best fit the innovation results and the exploitation opportunity. It is possible to structure these activities along several dimensions:

- The exploitation actor(s) will influence the type and target audience of an exploitation activity. The NEURONS project distinguishes between industrial actors (SMEs, etc), and academic actors for exploitation (i.e. research institutes, universities, etc).
- The exploitation type depends on the achieved innovation result and on the time horizon of the exploitation activity. Some exploitation uses direct technical improvements and usually has a relatively direct impact within a short time frame. Other activities leverage research results with a long-term impact on the networking community to derive strategic guidelines.
- Exploitation activities can also be specifically targeted internally to members of the consortium and their own operation, or they can be geared towards external activities, for example, to set the basis to develop cutting-edge Medical Imaging Systems, massive data processing centers, etc.

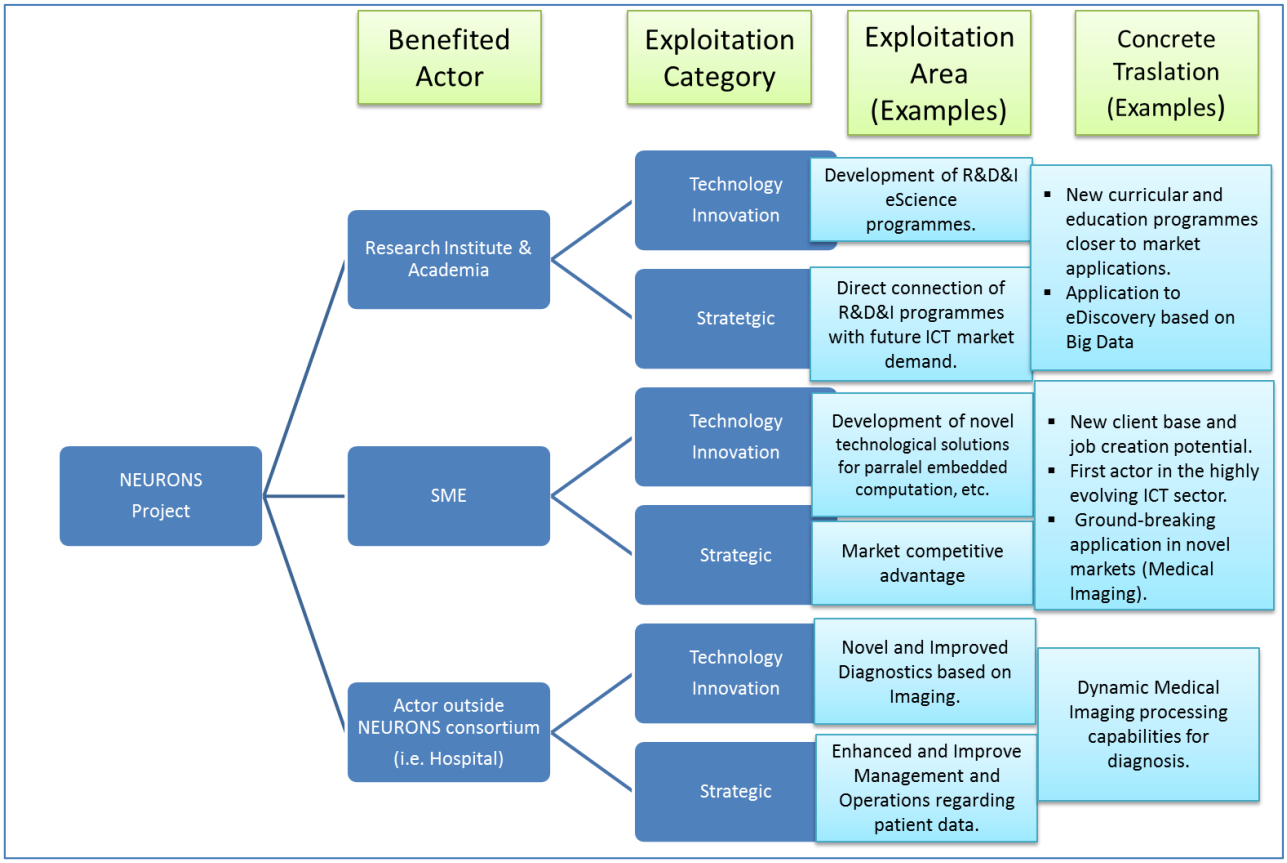


Fig. 3.2.1. Exploitation routes, actors and elements of the NEURONS project.

In different combinations of these dimensions, the weight of our exploitation activities differs, but is present everywhere. The exploitation structure is summarized in Figure 3.2.1.and will be used in the following description. Despite this structure the NEURONS project obviously seeks for synergies and joint potential between these exploitation opportunities during the project.
The NEURONS **industrial SME partners**, will be mainly focusing their exploitation activities on improving their current operation and business position in existing markets and on the creation of and preparation for new markets, with the intention to secure a strong leadership position in these new markets (i.e. medical Imaging, Computer Vision, Embedded Computing Systems, etc). To this end, potential **standardization** is an important means for example in terms of the device and system architecture and/or data processing algorithms. Also, the **modular approach** of the NEURONS technology (i.e. AMMA-chip, FPGAs, AMMA-Board, etc) will facilitate exploitation since the generation and potential out licenses of IP increase. **Industrial partners can exploit direct technical improvements internally**. The following examples illustrate this: A solution provider (i.e. SME) can use the acquired know-how to shorten turn-around times from the project results to products – for example, in the parallel Big Data processing context – to reduce time to market and improve its business position or to outperform competitors through the quality of immediately forthcoming new products. NEURONS research Institutions can introduce and pioneer future computing paradigms faster than peers. SMEs can speed up the deployment of new computing technologies and new associated services and applications, resulting in new usage scenarios and new customers (i.e. Analysis of massive financial Data in real time, Cryptosystems, Cybersecurity, etc). **Industrial partners can also exploit direct technical improvements externally**. The prime objective here is to create new products and services for already existing or currently incipient markets (i.e. Big Data). Participation in the NEURONS project and the resulting acquired experience and expertise will provide an essential time-to-market advantage over competitors. The NEURONS project consortium partners will be better prepared for new markets, products, and services and can position themselves early on. They can also work towards the creation of new customer relationships by creating a community around their new offerings. Such direct transfer into new products might be particularly appealing for the SME partners who could, for example, rapidly exploit services and appearing educating the customers and business relations of larger organizations about the new technical possibilities and by developing attractive offerings. The NEURONS project foresees in the actions related to dissemination and exploitation of project results the organization of tailored webinars/workshops as well as the participation of specialized conferences of especially relevant stakeholder communities (i.e. Medical Systems Community, High Performance Computing community, Industrial Manufacturing,

etc). The exploitation goals of **academic partners** (i.e., universities and research institutes) are different yet complementary to those of industrial partners. **Innovation developments** will be integrated quickly into the teaching curricula and research agendas of the NEURONS consortium partners, giving themselves as well as their graduates and research scientists a competitive edge, especially with respect to other research centers and universities. Academic partners will also make sure that these developments are carried into future national and international research projects, deeply rooting NEURONS results in research and development activities (i.e. the technology developed by NEURONS will be immediately incorporated into the technology upgrading programmes of the ATLAS and CMS detectors at CERN). By publishing high-quality papers about the NEURONS results, academic partners will obtain improved international visibility and improve their position in attracting the best international PhD, Master and graduate level students to their institutions. The **strategic academic exploitation** naturally has a longer time horizon. It will allow preparing the future research agenda, based on the results achieved by NEURONS, and identify new problems which have to be solved to strengthen the NEURONS impact even more (i.e. New High Energy Physics avenues, Computer Vision, Artificial neural networks, etc). The long run result of the efforts of the academic partners will be to place the approaches developed in NEURONS in the mainstream of teaching in networking and communications systems.

These extremely ambitious exploitation goals are feasible because of the setup of the NEURONS consortium. The NEURONS consortium consists of leading organizations from the embedded computing and high-performance computing fields, a unique combination that will enable the exploitation of the project results, its replicating potential and have an established framework to transform this investment and participation into a substantial commercial and strategic innovative opportunity.

Section 4. Ethical Issues

ETHICAL ISSUES TABLE

None

	YES	Page Number
Informed Consent		
• Does the proposal involve children?		
• Does the proposal involve patients?		
• Does the proposal involve persons not able to give consent?		
• Does the proposal involve adult healthy volunteers?		
Biological research		
• Does the proposal involve human genetic material?		
• Does the proposal involve human biological samples?		
• Does the proposal involve human biological data collection?		
• Does the proposal involve human embryos?		
• Does the proposal involve human foetal tissue or cells?		
• Does the proposal involve human embryonic stem cells?		
Privacy		
• Does the proposal involve processing of genetic information or personal data (e.g. health, sexual lifestyle, ethnicity, political opinion, religious or philosophical conviction)		
• Does the proposal involve tracking the location or observation of people without their knowledge?		
Research on Animals		
• Does the proposal involve research on animals?		
• Are those animals transgenic small laboratory animals?		
• Are those animals transgenic farm animals?		
• Are those animals cloned farm animals?		
• Are those animals non-human primates?		
Research Involving Third Countries		
• Is any part of the research carried out in countries outside of the European Union and FP7 Associated states?		
Dual Use		
• Does the research have direct military application		
• Does the research have the potential for terrorist abuse		
ICT Implants		
• Does the proposal involve clinical trials of ICT implants?		
(IF NONE) I CONFIRM THAT NONE OF THE ABOVE ISSUES APPLY TO MY PROPOSAL	x	

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