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PEOPLE
MARIE CURIE ACTIONS

Marie Curie Industry-Academia Partnerships and Pathways (IAPP)
Call: FP7-PEOPLE-2012-IAPP

PART B

"FTK"

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B.1 LIST OF PARTICIPANTS

Please provide an overview of the consortium composition by giving details of the legal entity, the department carrying out the work and the person-in-charge of the project.

All Participants	For Commercial Sector Participants, please tick ✓	If SME, please tick ✓	City, Country	Legal Entity Name	Department /Division/ Laboratory	Scientist-in-Charge
Caen SpA	✓	✓	Viareggio Italy	Costruzioni Apparecchiature Elettroniche Nucleari S.p.A:	R&D Department	Stefano Petrucci
Prisma Electronics	✓	✓	Alexandrou-polis, Greece	Prisma Electronics SA	R&D Department	Konstantina Mermigli
University of Pisa			Pisa Italy	University of Pisa	Physics Department	Mauro Dell'Orso
Laboratoire de Physique Nucléaire et des Hautes Energies			Paris France	CNRS	LPNHE UMR 7585	Giovanni Calderini
CERN			Geneve Switzwerland	European Organization for Nuclear Research	TS-DEM Development Electronics modules	Betty Magnin
Aristotle University of Thessaloniki			Thessaloniki Greece	Aristotle University of Thessaloniki	Physics Department	Konstantinos Kordas

Data for SME participant(s):

SME name	Location of research premises (city / country)	Number of full-time employees	Type of R&D activities	Number of employees in R&D	Company web site	Annual turnover (approx, in Euro)
Caen S.p.A.	Viareggio/Italy	65	HV Power Supply and Front End Electronic	32	www.caen.it	10M€
Prisma Electronics	Alexandroupolis /Greece	42	Smart Sensors Wireless Network, Hardware & Software develop.	10	www.prisma.gr	3 M€

START PAGE COUNT

B.2 S&T QUALITY (maximum 10 pages)

- ***S&T objectives of the research programme.***

The Physics programme at CERN's Large Hadron Collider (LHC) has been extremely successful since the early phase of data taking in the year 2010. The LHC detectors were designed to search for new discoveries in the head-on collisions of protons of extraordinarily high energy. Among the most interesting searches are the origin of mass, extra dimensions of space, unification of fundamental forces, and evidence for dark matter candidates in the Universe.

Moreover, the LHC upgrade, currently called the Super LHC (SLHC), will provide continuously increasing instantaneous luminosity, and will widen our capability to search new phenomena that are beyond the scope of our current theory of matter and energy, the Standard Model (SM). In the next few years an impressive harvest of data will be collected at the LHC and at the same time R&D at the technological frontier will be pursued for SLHC. The proponents of this project are active essential participants of both events. These experiments will have a fundamental impact on physics and technology for the next 20 years.

There are good reasons to expect that these new areas of research will have heavy quarks as well as tau leptons – the so-called third fermion generation - in the interesting events. These third generation objects will be excellent probes to search for New Physics.

Tracking devices, and in particular the Silicon devices that are becoming the predominant tracking technology, play an essential role in the identification of the third fermion generation.

On the other hand the electronics required to process the signals from the detectors is taking a very important role, and it must be state of the art. The most interesting processes are very rare and hidden in an extremely large level of background. Implementing the most powerful selections in real time is therefore essential to fully exploit the physics potential of experiments where only a very limited fraction of the produced data can be recorded. A drastic real-time data reduction must be obtained. This makes on-line event reconstruction a critical component at any hadron collider experiment. The trigger must be extremely intelligent and powerful. A multi-level trigger is an effective solution for an otherwise impossible problem at LHC. The level-1 (L1) trigger is based on custom processors and reduces the rate from 40 MHz to ~100 kHz . The level-2 (L2) is based on standard CPUs. The L2 output rate is ~3 kHz. The Level-3 (L3) selection, called Event Filter in Atlas (EF) is performed by CPU farms, which write to tape about 200 events/s (at LHC L2 and L3 can also be called High Level Trigger, HLT).

This project directly addresses the main technological challenges of hardware, software and data analysis necessary to identify heavy flavour objects and jets with a tau lepton. These are tracking issues at detector and trigger level. Addressing the challenging physics goals at the terascale requires a high degree of sophistication from the detectors and significant technological breakthroughs especially in:

- New developments in Silicon tracking technologies for thin, radiation-hard sensors
- Sophisticated triggering and real time processing
- Use of very deep sub micron electronics

The high-occupancy environment experienced at the LHC and even more at the SLHC, will require a huge computing power to reconstruct the very complex events with hundreds of particles emanating from the proton-proton collisions happening every 25ns at the heart of the detector. The increase in luminosity of accelerators will require highly segmented and radiation-hard sensors. Given the difficulty to fully deplete the sensors under those conditions and considering the importance of material budget in the quality of track reconstruction, a new development of thin sensors is necessary. We propose a collaboration between research companies active in high energy physics and research institutions to face these challenging future conditions.

The first important goal of this project is the *realization* and *optimization* of the Associative Memory (AM) system to make it work in the FastTracker (FTK) processor for the Atlas experiment at LHC and its future evolution for new applications. FTK is a high-performance "super-processor" based on the combination of two innovative technologies: powerful

FPGAs (Field Programmable Gate Arrays) working with standard-cell ASICs (Application-Specific Integrated Circuits), the Associative Memory (AM) chips, for utmost gate integration density. Optimal partitioning of complex algorithms on a variety of computing technologies has been already proved to be a powerful strategy (see the next paragraph), which turned the past hadron collider experiment CDF at the Tevatron accelerator in the Fermilab Laboratory, near Chicago (USA) into a major player in the field of B-physics, on par with dedicated experiments operating at e+e- colliders.

A complementary and secondary goal is the participation to the development of new sensors and electronics for the upgrade of the Silicon tracker of the ATLAS experiment. The sensors should be able to provide a charge collection efficiency still larger than 50% even in condition of partial depletion at an equivalent fluence of 10^{16} neq/cm^2 (neq: neutron equivalent).

- ***Intersectoral issues***

There are important reasons, outside High Energy Physics (HEP), for the research proposed in the present program. Our approach to use powerful modern electronics is extremely flexible and its spread outside the realm of HEP would be extremely beneficial. The strategy of the "optimal
mapping of a complex algorithm in different technologies" is a general approach that can speed up enormously any calculation by providing a high degree of parallelism.
Handling complex electronics components (dedicated AM chips and FPGAs) is less straightforward than programming a multi-core CPU, since it requires availability of FPGA hardware and knowledge of computer-aided-design (CAD) tools. For this reason we think that the HEP development in this area is important to show the potential of these devices and to spread the skills needed to use them with top efficiency. There are already examples showing that the use of a tuned combination of CPUs and FPGAs could expand not only in physics experiments, but also in other academic and even non-academic fields, for example in financial applications. The “Workshop on High Performance Computational Finance” is an instance of the many occasions for discussing FPGA acceleration techniques in the financial domain.
These techniques could be very important in the area of medical imaging for real-time diagnosis, when the patient is under examination. The computing power is still a limiting factor for some high quality applications. High-resolution medical image processing, for example, demands enormous memory and computing power to allow 3D processing in a limited time.
The same approach could be very incisive for astrophysical and meteorological calculations, for robotic automation, and for security applications.
It could be essential for neurophysiologic studies of the brain. Recent advances in ICT and neuroscience allowed to study and model “in silico” a significant part of the human brain. The brain is certainly the most complex, powerful and fast processing engine and its study is very challenging. Understanding how the brain processes information or how it communicates with the peripheral nervous system (PNS) could provide new potential applications, new computational systems that emulate human skills (e.g. by using the directed fusion of diverse sensory information) or exploit underlying principles for new forms of general purpose computing. Significant improvements could be gained in terms of performance, fault tolerance, resilience or energy consumption over traditional ICT approaches.
The use of the associative memory processor for brain studies is particularly fascinating. The most convincing models that try to validate brain functioning hypotheses are extremely similar to the real time architectures developed for HEP. A multilevel model seems appropriate also to describe the brain organization to perform a synthesis certainly much more impressive than what done in HEP triggers. The AM pattern matching has demonstrated to be able to play a key role in high rate filtering/reduction tasks. We can test the AM device capability as the first level of this process, dedicated to external stimuli pre-processing. We follow the conjecture of reference [Punzi & Del Viva (2006) Visual features and information theory JOV 6(6) 567]: the brain works by dramatically reducing input

information by selecting for higher-level processing and long-term storage only those input data that match a particular set of memorized patterns. The double constraint of finite computing power and finite output bandwidth determines to a large extent what type of information is found to be “meaningful” or “relevant” and becomes part of higher level processing and longer-term memory. The AM-based processor will be used for a real-time hardware implementation of fast pattern selection/filtering of the type studied in these models of human vision and other brain functions.

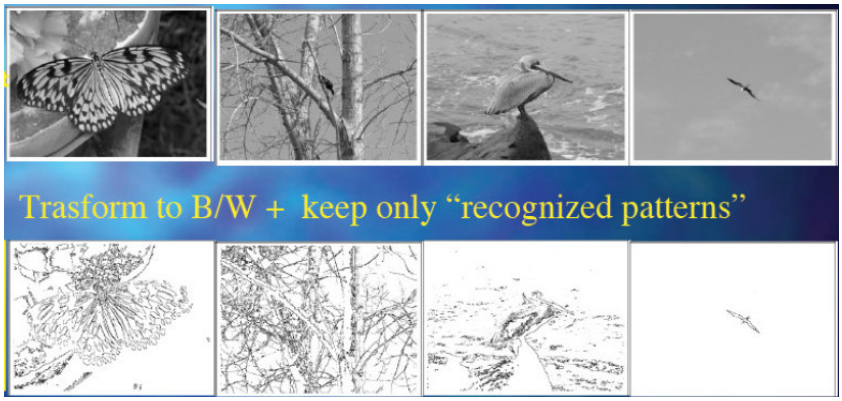

Figure 1

The second row of figure 1 shows the quality of the image when filtered accepting only the “good patterns” stored in the AM. We could apply this filtering function to medical images, to extract the salient features and apply fast but complex reconstruction algorithms to them. We would measure the extracted features in a very short time and automatic fashion providing a computer-diagnosis. The reduction of execution time of image reconstruction to be applied after the AM filtering function, would exploit the computing power of parallel arrays of Field Programmable Gate Arrays (FPGAs) as we do in FTK to find clusters of contiguous pixels above a certain programmable threshold. As we process them producing measurements that characterize their shape, we can measure quantities of interest in medical applications like the size of the found spots, how circular or irregular the spot is. The algorithm can be extended to 3-D images.

For what concerns the development of sensors and related electronics, one obvious inter-sectorial aspect is the medical physics. Solid state detectors have been used in medical imaging for many years for early diagnostic in cancerology. Digital images provided by this kind of sensors can also be processed with pattern-recognition algorithms to increase the diagnostic capability.

- ***Originality and innovative aspect of the research programme.***

The philosophy of performing almost offline selections at rates of the order of 100 kHz at LHC, or even more, is absolutely new. The idea of using dedicated mixed-technology Supercomputers is innovative in a world where the use of dedicated hardware has been strongly reduced. This is an important time to demonstrate to the high energy community the capability of the FTK online tracker. The very precise LHC silicon detectors, which contain hundreds of thousands or millions of channels, increase the problem of complete tracking in large numbers of high multiplicity events. With hundreds or thousands of particles produced by multiple primary collisions and traversing many detector layers in all directions, this is a formidable challenge even for off-line analysis. A complete high-quality tracking for real time event selection has been considered impossible in LHC experiments at very high rates. As a consequence, Real-time tracking is planned for a limited detector region or on a small subset of events, previously selected using other detectors. Many physicists dismiss a complete on-line tracking in LHC experiments because they see it as a too formidable problem. The goal of this research is to prove that up-to-date technology, exploited with suitable organisation and algorithms, permits the development of high-performance tracking triggers sensitive to secondary vertices and complex structures like taus. The search for new physics not

covered by the Standard Model requires to collect enormous samples of data in extreme conditions to improve the precision of future measurements. This gives increasing importance to parallel computing and dedicated real-time techniques.
The FTK strategy has a particularly relevant impact now that the LHC community is starting to consider the design of new architectures for the SLHC upgrade, especially for the L1 trigger. The FTK R&D project, developed in the past, has a significant impact on the discussion of future architectures.

Knowledge of the state of the art.

The CDF experiment at Fermilab was the best of the state of the art for triggering at a hadron collider. It had a very strong tradition in this field, since a large part of the trigger was implemented with dedicated hardware, and has been operational for many years, constrained to work within very short latencies (few μs). It has been upgraded several times during the 20-year life of CDF, to exploit technology advances. It has been equipped with powerful tracking processors at L1 (the L1 eXtremely Fast Tracker, XFT) and L2 (the Silicon Vertex Tracker, SVT). SVT was the most powerful trigger processor operating at a collider experiment so far and it is a perfect baseline for our project. Many proponents of this project were part of the team that had a leading role in its design, construction, commissioning and management. It performed online track reconstruction in the silicon detector (SVX) and the central drift chamber (COT) with sufficient accuracy, almost the offline resolution, to identify tracks from b-quark decays via their large impact parameter, IP>100 μm, where IP is the distance of closest approach to the beam line. SVT has been essential for the Bs mixing frequency measurement, the rare B-decay searches (B0s->mu mu), the observation of heavy baryons (Σ_b and Σ_b*), the first observation of the rare charmless decay modes of the B^0_s and Λ_b, the search for CP violation in D^0->hh di-hadron decays, and the evidence for charm mixing. These extremely challenging measurements would have been completely out of the CDF reach without the SVT. Since B-physics had a limited budget in terms of allocated trigger bandwidth, the better purity allowed CDF to increase by several orders of magnitude its efficiency for the hadronic B decay modes. Historically, B-physics events have been selected at hadron colliders by triggering on leptons produced in the decay of the away-side B. Trigger selections based on the reconstruction of secondary decay vertices greatly increase the b-quark identification efficiency and allow collecting otherwise inaccessible hadronic decay modes. The availability of the hadronic decay modes at CDF determined the quality of the CDF B0s mixing measurements. Also for high-PT physics CDF has demonstrated the possibility of successfully using purely hadronic channels in the study of the top quark, in Higgs searches, and even in the reconstruction of the Z0 boson, thanks to the secondary vertex b tagging. The 2009 W.K.H. Panofsky Prize was awarded to the SVT creator, Luciano Ristori, recognizing “the leading role ….. enabling broad advances in knowledge of the top quark, b-hadrons, and charm-hadrons….”.
The AM was already the central device of the SVT system at CDF. The AM shares some features with the Content-Addressable Memory (CAM), a special type of memory used in very high speed searching applications. Unlike the standard computer memory (RAM), in which the user supplies an address and the RAM returns the data word stored at that address, a CAM is designed such that the user supplies a data word and the CAM returns the addresses, if any, where the word is stored. The data word recognition unit was proposed by Dudley Allen Buck in 1955. He invented the technique of storing and retrieving data with no need to know the location of that data. The inquiry for data is broadcast to all memory elements simultaneously; thus data retrieval time is independent of the size of the database. Each individual memory bit cell in a fully parallel CAM must have its own associated comparison circuit to detect a match between the stored bit and the input bit. Additionally, match outputs from each cell in the data word must be combined to yield a complete data word match signal. The additional circuitry increases the CAM physical size, cost and power dissipation (every comparison circuit is active on every clock cycle). Consequently, CAM is only used in specialized applications where searching speed cannot be accomplished using

a less costly method. They are used for example into routers and more generally into computer networking devices.

Triggering at a hadron collider is a field where the speed and the high parallelism of the AM have been extremely successful. A major contribution to the required drastic real-time data reduction comes from the information available from the full event tracking. To this purpose, AMs and CAMs have been used to implement a pattern matching algorithm based on pre-calculated and stored track candidates, compared in parallel with the actual event. Pattern matching has been adopted in different ways, depending on the trigger level where it was used.

Commercial CAMs have been used in the H1 experiment at the unique positron-proton collider HERA, hosted by DESY (Deutsches Elektronen-Synchrotron) in Hamburg, Germany. Basically, each bit of a CAM word corresponded to a detector channel. The whole event, made of a single large word, had to be submitted to the memory bank at once, i.e. in the same clock cycle. In order to limit the number of channels to the largest CAM widths, usually smaller than 1000 bits, only a small detector section was analyzed. Detector data come in the form of a sequence of addresses of hit channels. Thus, additional hardware must reformat the incoming data before sending them to the CAM. When the used detector section is sizable, the number of bits per word becomes prohibitively large for this method. E.g. 15 bits to address a channel on each layer of an 8-layer detector would require a chimerical 2^3x2^{15} bit wide CAM. Here comes the major difference between the AM and the CAM. In the AM each pattern is also stored in a single memory location, but it consists of N independent words of M bits each. Each word refers to a different detector layer and represents the address of a possible hit channel on that layer (in the above example N=8 and M=15). Each word is provided with reserved hardware comparators and a match flip-flop. All words in the AM can make independent and simultaneous comparisons with the hit addresses serially presented to common buses. Any time a match is found, the match flip-flop is set. A pattern matches when a majority of its flip-flops are set.

The first AM chip was made with ASIC full-custom technology and was specific to the 5-layer CDF silicon detector. It is unsuitable for the complexity of the tracking detectors at LHC. Any redesign would imply a large investment in terms of time, personnel, and costs. For simple applications, we designed a low density AM chip based on the essential characteristics of the commercial programmable devices (FPGA). The use of FPGAs allows easy development and easy update of the project, but FPGAs devices are inferior to a full custom ASIC for what concerns the achievable logic density. If a high pattern density is required, using a standard-cell ASIC can be a very good compromise between the easy design of an FPGA and the logic density of a full custom ASIC. This strategy was chosen in developing the second generation CDF AM chip, a standard-cell chip for the SVT upgrade. Finally, a new full custom CAM cell was designed for use in a 65 nm standard-cell chip suitable for the LHC. The chip, submitted for production, is optimized for maximum pattern density, minimum power consumption and implements new power functionalities such as a variable, pattern-depending spatial resolution.

The silicon detector evolution has a comparable importance. The past decades witnessed the transition from small silicon devices used as vertex detectors (few tens of cm^2area) to larger size full tracking devices (7 m^2 at CDF) which now reach the 200 m^2 at CMS. The use of pixel detectors has been shown extremely relevant in reconstruction of the LHC high occupancy events. A new generation is already needed for the SLHC detectors. Low material budget, higher spatial (e.g. higher granularity) and momentum performance are key issues. New Silicon microstrip and pixel detectors, radiation hard (new n-on-p substrate as proposed for SLHC) and/or larger size wafers, thinned sensors, with triggering features already built in (smart detectors) are under study in the LHC collaborations.

Scientific quality of the joint collaborative research programme.

FTK is a second generation processor, much more ambitious than its progenitor at CDF. It reconstructs all events coming out of the L1 (100 kHz) to provide into few dozens of microseconds all the tracks with transverse momentum above 1 GeV to the L2. The power of

FTK is mainly based on the AM chip. The same AM technology can be used also at L1, even in much more adverse conditions. All the LHC experiments, ATLAS, CMS and even LHCb, are thinking to it for SLHC. Let's compare the Tevatron and LHC machines to explain the increase of complexity of events and, as a consequence, of the tracking detectors. The CDF collision rate was ~2 MHz and at the instantaneous luminosity (ILum) of 3×10^{32} cm^{-2} sec^{-1} the average number of soft, not-interesting interactions per bunch crossing (pile-up) was 6 (396 ns bunch spacing). The LHC environment is much more demanding: a bunch spacing of 25 ns at high ILum (10^{34} cm^{-2} sec^{-1}) produces ~25 pile-up interactions. The LHC upgrade (SLHC), with the recently proposed scenario of a 50 ns bunch spacing, will produce a pile-up of hundreds of events at the ILum of $5x10^{34}$ cm^{-2} sec^{-1}.
Today we can exploit a very important advantage to face the increased complexity: on the technological side, (a) the detector granularity is strongly increased (the SLHC silicon projects are an extreme result in this direction), (b) the digital electronics is becoming so powerful that the difference between the performance of the algorithms executed in real-time and in the offline analysis is significantly reduced, even in the extremely hard conditions of high data rates and limited processing time. Since the background suppression needed at trigger level is becoming similar to that of the usual offline analysis, the offline quality is required already at trigger level. Our goal is "online exploitation" of the full silicon detector resolution: it is challenging, but it is not a impossible.
The FTK tracking algorithm is subdivided into 2 sequential steps of increasing resolution. In step 1 the dedicated VLSI device, the AM, finds track candidates with low spatial resolution, called roads. In step 2, the real tracks are searched within the roads and fitted to determine their parameters with the best resolution (sigma(IP)=35 μm, sigma (1/PT) = 0.3 % and sigma(φ0)=1 mrad). Tracks with PT>1 GeV/c are finally selected to tag secondary vertexes or to search for hadronic taus or to perform high quality track-based isolation of muons, electrons and gammas.

The AM performs the most CPU intensive part of the pattern recognition, exploiting dedicated highly parallel structures. It exploits the idea of a pattern matching algorithm based on pre-calculated and stored track candidates, which are compared in parallel with the actual event. It has to solve a very difficult problem since the silicon detector has millions of channels and the number of track candidates is very large (~10**9). For this reason a high density dedicated chip has been developed for the AM.

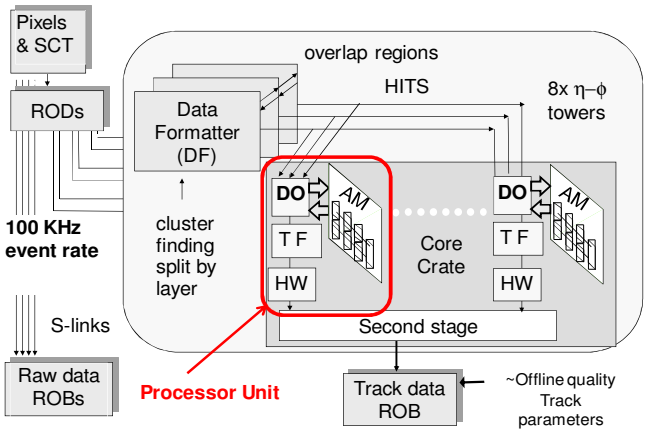

Figure 2

FTK includes important pre/post processing functions (see figure 2), complementary to the intensive pattern-recognition performed by the AM. Pre-processing corresponds to (a) cluster finding in the silicon data, performed by ATCA boards called Data Formatters (DF); (b) smart database for immediate retrieval of full resolution detector clusters associated to roads found by the AM, performed by Data Organizers (DO). Post-processing includes (a) the track fitting performed by Track Fitters (TF) and (b) duplicate-track cleanup performed by the Hit Warrior

(HW). The most important function is the track fitting, which refines the candidate tracks in order to determine the track parameters with the full detector resolution. The TF makes use of methods based on local linear approximations and learn-from-data techniques for online misalignment corrections. The fit calculation consists of many scalar products. The FTK simulation shows that the approximations introduced to maximize the speed do not significantly affect the fit performance.

The event processing is highly parallel into all online tracking processors, with the detector segmented into η-φ towers. Our main goal is to build the Processor Unit (PU, the red box in figure 2) that pipelines all the functions needed by a high quality real time tracker. This is the core of the processor. A full coverage online tracking for ATLAS at the LHC Phase 1 instant luminosity is estimated to require 8 9U VME crates with sixteen PUs each (128 PUs), using the best technology available today. In addition to that, two ATCA crates of Data Formatters are necessary to cluster the raw hits coming from the detector and to provide the correct data to each PU. The main DF processing device is the FTK Input Mezzanine, (FTK_IM), a data concentrator-processor for pixel and strip silicon detectors. It performs online clustering for uni- (strips) and bi-dimensional (pixel) detectors. Different clustering approaches will be studied and implemented on FPGAs.

The FastTracKer (FTK) has been approved recently by ATLAS for a Technical Design Report (TDR) submission in 2013 and to build a small demonstrator taking data in 2015. FTK is today mainly a collaboration between Italy and USA with a smaller contribution from Japan. If the demonstrator is successful, FTK will be enabled for a large production and will be a trigger upgrade for the LHC Phase1 (Phase I, up to $L = 2x10^{34}$ cm^{-2} s^{-1} and 40-80 pileup events). The Italian funding agency, INFN, has taken the responsibility to fund the PCBs and chip costs for the AM system in the demonstrator, but no money is provided for hardware/software development, neither for future tests and commissioning periods, neither for further developments. The EU funds would provide the complementary contribution to push further this research, involve new Institution and Companies in a area that is in quick expansion, where new manpower and organization capabilities are strongly needed.

In parallel we need to gain experience on the modern TDAQ systems to face early the integration problems such a complex device could meet. Atlas is allowing us to test the integration of the FTK functions in the experiment, today, well before production. We plan early parasitic commissioning (no impact on normal ATLAS data taking, thanks to a duplicated additional output fiber provided for FTK by the tracking front-end) of a small proto-FTK, based on existing prototypes and able to reconstruct tracks inside a narrow azimuthal slice (tower) of the detector. The FTK output can be written to the calibration stream for offline studies. We call this proto-FTK a “vertical slice” because it will be small (operating on a slice of the detector) but functionally complete from the detector inputs up to the track output available for the L2 CPUs. The vertical slice will continue to exist as a test stand for new prototypes while the FTK demonstrator will start to take data in 2015.

In addition a new R&D is planned for the FTK evolution necessary for the many new foreseen applications, like online tracking at L1 and use of the AM for image processing. Time for FTK production after the TDR approval will be quite long, because of the LHC schedule, so even the FTK final production could profit of the electronic and algorithm advancement we plan to pursue in the next years. While the demonstrator will convince the collaborations of the FTK capabilities, we will provide modern, much more powerful prototypes (AMBSLP), fully tested in the vertical slice, ready to substitute the FTK default one (AMBFTK) in the final production.

The Serial Link Processor (SLP): a new Processor Unit for many different uses.

In the R&D area our goal is to build a new Processor Unit called "Serial Link Processor" or SLP. The SLP has many points in common with the past developments: it pipelines all the functions needed by high quality real time tracking (AM, DO, TF, HW); it will occupy a single VME slot, and will consist of a 9U VME board, the AMBSLP, along with an AUX card on the back of the crate, built by the USA FTK collaboration. The two future boards will exchange data through the P3 connector as shown in figure 3.

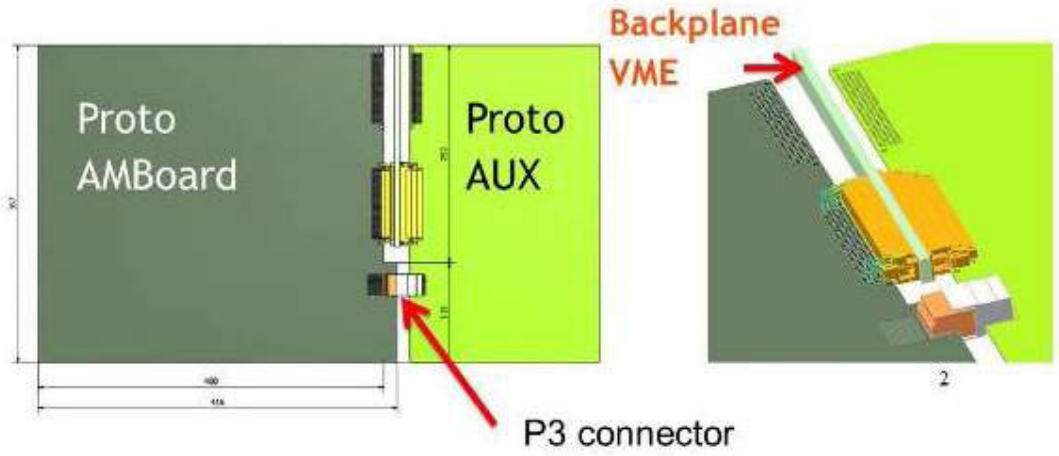

Figure 3

The AMBSLP, the object of the European research, will perform pattern recognition (128 AMchips on it). The AMBSLP has the same modular structure of the AMBFTK. It consists of 4 smaller boards, the Local Associative Memory Banks (LAMB). Each LAMB contains 32 AM chips, 16 per face. The AM chips come in LQ208 packages, and contain the stored patterns with the readout logic. They are connected into eight 4-chip pipelines on each LAMB. The found roads flow down in the 8 pipelines and are collected and merged into 4 parallel output streams by two readout logics called GLUEs. The SLP has a flexible control logic placed inside powerful FPGA chips (Xilinx). The FPGA flexibility allows to use the same architecture in different applications characterized by short- or long-latency trigger decisions, with the only exception of the LAMB, which needs to be specialized. In the case of long-latency (L2 application or seeding of the offline tracking or image processing) very large associative memory banks can be obtained pipelining boards and AM chips. For low-latency applications (L1) we reduce the pipelines as much as possible. We will develop a unique motherboard for all possible conditions. Two type of different LAMBs will be developed, one for long-latency and one for low-latency applications. In the second case GLUE chips will be placed in the center of “stars” of AM chips directly connected to them, reducing significantly the latency for the road readout.

The SLP innovation consists in the use of high speed serial links everywhere in the system. This new feature determines the name of the new computing device (Serial Link Processor). The AM system is today overloaded by the enormous traffic of words flowing to the AM chips. Eight TTL 15 bit buses bring hits to the SLP with a consequent enormous fan-out problem (128 AM chips) . This is made even more complex by the board output traffic that in the LHC very high luminosity will become extremely demanding and will require a larger number of output buses (16), of larger words (32 bit). A redesign of the boards and a new AM chip equipped with serializers, deserializers & differential I/O are required. The chip development is funded by INFN. The use of serial links will have several important advantages:

1. The system would gain in flexibility, since data words with variable size could be delivered and collected without any change to the boards. It would gain also robustness, since the LVDS connection is much more robust against noise and cross talk.
2. We can push the transmission frequency into new ranges, far from what we faced in the past.
3. The board routing will be optimized and much less crowded. In particular the LAMB reorganization for L1 application, where direct connections are required between the many AM chips and the readout controllers (GLUEs) would not be possible using a large TTL road bus for each AM chip.
4. The necessary number of pins for signals in the AM chip package will be reduced. This is important because the AM chip silicon area has to be increased in the future by a factor of 10, to contain a much larger number of patterns, with no change of the package.

Unfortunately also the needs of the chip in terms of voltage and ground pins will increase correspondingly, while the package we have now (LQ208) is totally occupied by the many necessary TTL input buses. Using serialized inputs/outputs will provide space for VCC and GND pins.

5. The connection between the AMBFTK/AMBSLP and the AUX board is implemented with a very compact, high performance P3 connector (see figure 2), while in the past the AMBoard needed complex connections with the other boards. No backplane is anymore necessary.

- ***Appropriateness of research methodology and approach***.

Our research methodology is based on the idea of a "*continuous evolution"*. Our final goals are very challenging, so it is important to advance per steps. For this reason we organize our work in such a way that design, tests and commissioning are performed in parallel, instead of executing them sequentially as usually is done. It is important that results on tests and commissioning provide a feedback on design before the system is frozen for a large production.

This working plan is extremely ambitious. The methodology of parallel design, tests, commissioning and future R&D is very demanding in terms of manpower and infrastructures. In addition the interest for this technology, as explained above, is quickly expanding. New studies are necessary for L1 and outside-HEP applications. It is particular relevant to have the possibility to involve new institutions and new companies that can learn about the project in the development phase and be fundamental in the future at the production and running time. The work is organized in 5 areas, or work packages.

The first one, "Prototype Production", includes board design, FPGA firmware development, PCB construction and assembly, standalone test for a first validation. It is particularly important that the designer can participate also to the first tests, before his product is integrated on the complete system. The board design is based on the Cadence tools while the fimware is developed with the Xilinx CAD. The board assembly is complex, especially for the LAMB mezzanine that holds 32 AM chips, 6 xilinx FPGAs and CPLDs, and 8 devices for clock distribution in a very small space. In addition to the LAMBs, the motherboards and the FTK_IM mezzanines will be produced.

The second work package, "Infrastructures and Integration", first of all takes care of the crates, the power supplies and the space for integrated lab tests. We use 9U VME crates with custom VME VIPA backplane. We use 48V power source to provide the needed power for 128 AMchips per board. An extension of the board in the front has been necessary to allocate large DC-DC converters from 48 Volts down to 1.2 V, the core AMchip voltage. The board has 4 DC-DC converters, each one providing a maximum of 25 A at 1.2 Volts, for a total of 100 A and a maximum power of 120 W. Each AM board has a weight of 2 Kg, so the crate has to support a total weight of 40 kg. Cooling and mechanical tests will be performed. The air flow must be sufficient to keep cold enough the boards. Each rack will contain two crates, each one provided of its own power supply. The power supply has to be transparent as much as possible to flux of air. The whole system will be collected in a single place, including parts developed outside the collaboration. There realistic experimental conditions will be reproduced and tests enough complex will be performed with Monte Carlo data to guarantee that the hardware is complete and can run flawlessly. Software will be developed for monitoring and control of the processor. In the laboratory the detector data will be produced by a "pseudo front-end" (a CPU). Data will be delivered via S-link from a mezzanine inserted in the CPU (Quest).

The third work package, "Commissioning", closes the research path described above. After tests in the laboratory, the new hardware will be moved to the experiment and will spy real data during normal data taking. In fact commissioning implies the insertion in the experiment, the development of monitoring and control software compatible with its rules, long tests to validate the system, data taking and data understanding.

The forth work package is "Architecture Simulation". It is just software, but it has an important impact on hardware choices. A complex package, FTKsim has to simulate the hardware on Monte Carlo data, or real data. It is used to optimize the hardware design, to specify, build and test the internal data paths needed for the LHC high luminosity, to

determine the optimal size of the AM system, to produce the Physics case. The simulation is an essential part of all tests since it allows to predict the hardware output, starting from the inputs, to validate the hardware (sometime the simulation) functionality.

The fifth work package, “Image Processing”, is a new very interesting atypical working area. We will use our AM-based Processor to process static images and movies in real time. We want to check the capability of the AM to be able to extract from the images and from a movie the relevant features and substantially suppress the not-relevant information. The images have to be formatted in the right way to send data to the AM system. For static images groups of 3x3 pixels (black and white) are detected in the images and each particular configuration constitutes a 9-bit pattern. All found patterns will be sent to the AM and their frequency will be measured by the FPGA that controls the board. The pattern frequency is the determinant feature to decide if a pattern is relevant or not. After this learning phase, the relevant patterns will be downloaded in the AM bank and the processor will be ready to filter the static images selecting only ~5% of the input data. For films we need to add a third dimension, the time, so the patterns becomes 3x3x3, made of 27 bits (128 million possible configurations). The learning phase will find the frequency distribution of these patterns and the selection of the good ones will produce the content to be downloaded in the AM bank (a maximum number of 1.5 million patterns can be downloaded today). The AM system will always monitor the pattern frequencies and if the distribution will change the list of good patterns will be updated. The computing power of the mezzanine FTK_IM, developed to process bi-dimensional pixel detector data, could also be exploited to process the output of the AM, that is the filtered image.

The sixth work package is “Silicon Detector R&D”. In our application it has a reduced role compared to the electronics tasks, however it provides a solid link with the evolution of the ongoing R&D for the silicon sensors and the front-end readout electronics in view of the high-luminosity upgrade of the LHC. This link is important for FTK since a constant dependence connects the evolving features of the future tracker (segmentation, geometry, expected hit efficiency, noise, readout speed) with the future of the FTK architecture. CAEN will collect together competencies about the different aspects of the detector and the processing system. To resist in the high-radiation environment of the SLHC interaction region, new pixel sensors are being developed. The p-type bulk is being investigated and this is expected to improve the radiation tolerance (no type-inversion) and the cost of the process. In facts the layout of n-in-p pixel sensors requires the guard ring region to be on the same face of the pixels, basically giving a much cheaper single-side process with respect to the sensors presently used. After radiation damage, the maximum achievable depletion region will be reduced to a fraction of the detector thickness and consequently the signal size will be reduced. The sensors will be back-thinned considerably (well below the 300um, and possibly even below 200um if the technology evolution will allow to reach this in the next few years). The sensors will be operated at below-zero temperature to keep the leakage current to a still acceptable level of a few uA per sensor at -10C. The segmentation will also be reduced. The phi coordinate will follow closely the limit given by the interconnection technology (the present pitch is 50um but this will be reduced to at least 35um) while the pixel length in eta will probably be constrained by the consequent area of the cell and the component density of the readout electronics. Prototypes of a chip in 65nm CMOS process are being developed for the readout chip, to increase the component density of the readout chip and to allow a further reduction of the sensor pixel size. In all this, the power dissipation will play an important role and the high voltage distribution system will be one of the key ingredients in the evolution of the detector design. Even if the detector is operated at a below-zero temperature, a power supply system able to provide 1KV tension at a maximum current of about 10mA per channel will be necessary, with excellent temperature stability and excellent ripple/noise specifications even at full current. The test-stand for the module evaluation will be assembled at CAEN in Viareggio, Italy, to test how the CAEN devices can perform in these difficult conditions. The silicon sensors with their readout electronics will be used with the CAEN high- and low-voltage distribution system. CAEN has a long-tradition as one of the leader producers.

B. 3 TRANSFER OF KNOWLEDGE (maximum 6 pages)

Transfer of knowledge program. Consistency with research program

In this section we describe the transfer of knowledge offer both in the research and training sectors. There is a very large exchange of knowledge in the research work already, as explained in detail in section B.4, since this application is generated by the growing interest on this technology and the enlargement of the FTK collaboration. We have a very rich program of secondments. Our secondment plan has some peculiarities. First of all many physicists and engineers will be exchanged among the participant institutions, some of them working on the same items. This is justified by the fact that the project is complex and an important goal of this application is the training of a new team that should be strong enough to support all the new applications and developments. The new components of the team have a first period dedicated to learn the technology, followed by a second period where they will become the leading actors of a new application or a working package. The new teams need a significant number of participants to face the effort of the development of a new application. A second feature of our plan is frequent splitting of secondments in multiple periods. This is justified by a scientific program with multiple phases of design,construction,test and commissioning. Transfer of knowledge is optimized with multiple periods, as explained below. The multi-return-mechanism will ensure each time efficient transfer of knowledge back into the organisation of origin of the seconded staff, spreading the experience to the whole group.

Relative roles of secondments and recruitments

Here we describe the need of transfer of knowledge inside each WP keeping into account the project schedule described in section B.4 (see Schedule Table).

WP1 production & development (green in Schedule Table) – A flux of information is necessary inside the WP1, from the institutions already expert of tracking, as UniPi, to the new collaborators, AUTH, LPNHE and the Prisma SME. The new Academia collaborators were mainly involved in detector construction in the past (AUTH for muon detectors, LPNHE for silicon detectors). Now they are interested to start their activity in the trigger sector and in particular in the real time track reconstruction applied to their detectors. Also PRISMA manufactured electronics for CMS and did not have specific experience in online tracking in the past. On the other hand AUTH and LPNHE have been in ATLAS for a long time, and Prisma had experiences in CMS, while the UniPi FTK researchers only recently joined the ATLAS collaboration . The experience of AUTH, LPNHE and Prisma about the LHC experiments will be valuable for the new group that has to integrate a challenging device in the already installed and working detector. PRISMA offers also a wide experience in electronics design & development as well as in manufacturing prototypes and/or mass production, in particular for space, defence and CERN applications, that is electronics constructions to function in hard environments. This could be a unique training opportunity for secondments and recruitments visiting PRISMA. Also AUTH and LPNHE have a strong electronic division with significant FPGA expertise, so exchanging design experiences will certainly be worthwhile. This large availability of different design skills will increase the initial FTK project goals, the research quality and the overall RTD capability and competitiveness of all the partners.

Contacts among the research institutions and the Prisma SME are guaranteed by the large number of secondment months. UniPi experienced personnel (Piendibene and Donati) has planned some months of the first year at Prisma to (a) start the prototype production, (b) install the FTK test stand to check the assembly quality before the delivery of boards to integration (c) and also to collaborate on firmware and PCB design for the SLP2 prototype. They will also come back to Prisma in the 3rd and 4th years for the final FTK small productions after the FTK demonstrator success. The seconded ERs will bring back to UniPi their experience and will share it with other researchers opening their minds towards new opportunities, becoming familiar with practice in industrial routine.

Similarly young personnel will be seconded from AUTH to Prisma and viceversa. Prisma and AUTH will collaborate for the design of boards and also the development of

firmware. Prisma secondments to Pisa will have the same goal. During the first year they will work on the system for L2 (SLP2) with the help of UniPisa and after that they will apply their acquired knowledge to L1 (SLP1), starting from the last quarter of the 2nd year. Prisma engineers will profit of the high level tools (Cadence) available at the Universities and CERN. Coming back home they will transfer the knowledge to the company to reinforce it in its leading role of the WP1. Secondments dedicated to a certain job are split among collaborating Institutions to increase the connections among all the participants . For example the PCB design of the SLP2 will start in UniPi with the secondment of Sakellariou from Prisma to work with Piendibene It will continue at Prisma with the collaboration of both and Konstantakos from AUTH. The same will be done for the SLP1.This scheme is certainly the best way to reinforce the collaboration of the team, trained on a strong common background. The designers will spend time working together in different places, practicing different realities.

CERN wiil have a particular role for the prototype design since they will provide important trainings. The Electronic Service at CERN belongs to the accelerator sector but it has the typical organization of a company. They provide very professional service for board design based on the Cadence tools. Designing with them the future FTK boards will be a wonderful opportunity to learn all the Cadence details/functionality. This is the goal of the recruitment there. The Electronic Service will recruit a young engineer (ER, less than 10 years experience) with advanced experience in the area of hardware real time tracking processors and initial experience of Cadence board design. The engineer will work in the electronic service, learn at the best level the use of Cadence tools and transfer the acquired knowledge about the tracking project. He/she will work also for the tests of the prototypes and will also gain commissioning experience. His/Her career will certainly profit from this valuable experience at CERN.

Also AUTH will recruit one ER (less than 10 years experience) to work on online pattern recognition applied at Level 1 for the muon upgraded system. He/she will have to be expert of AM technology and its simulation, to reinforce the AUTH expertise in this field.

WP3 – Commissioning @ CERN (blue in Schedule Table). Commissioning of such a complex device in such a complex experiment & hard environment, already built & running is new for everybody within and also outside our collaboration. For this reason it is important to start early and proceed with small steps. All of us will learn gradually from the experience in the experiment. However CAEN has much more experience than the others, as far as infrastructure installation, security rules and procedures are concerned. CAEN will provide valuable support to researchers that will work there. At the same time CAEN will directly experience on the experiment the new field of application of advanced parallel and dedicated computing. It will acquire all the necessary expertise to help maintaining and expandinding this system in the future years of LHC data taking. This continuous exchange of expertise will be achieved with the secondment of Petrucci, high qualified CAEN personnel. He will participate to the 3 commissionings in the last 3 years. PRISMA engineer (ESR) K. Mermikli will be trained both by CERN and UNIPI experienced personnel and she will participate to the design of FTK tests and commissioning.

WP2 – WP4 Integration at CAEN & simulation (red and black in Schedule Table). This is a real training for all participating institutions. The exchange of experience and knowledge is maximum: we will collect all the results of all tests performed at each individual Institution to test the entire system of boards working together. This is the synthesis of all the individual efforts. For this reason we schedule a large number of secondment months there from all the research institutions involved in WP1 except CERN that will offer similar experience in commissioning. The secondment includes both experienced researchers (Piendibene, Donati, Crescioli, Kordas, Sampsonidis) and a younger team. The experienced staff will guide and supervise the young ESRs and ERs work. We will have a significant group from AUTH coming the 1st and 2nd years to work with Piendibene. After the experience of the first year on the AMBFTK, the second year they will become expert of serial links in the SLP2 and they will be able to discuss L1 architectures. Crescioli will advance in the tests in alternative periods, working with Piendibene that will guarantee the contact with the previous

experience. The 4th year the AUTH group will come back for the SLP1 tests. This will complete their effort and the success of these tests will be the transfer of knowledge. CAEN offers large enough infrastructures to allow this effort and will provide its competence to lead it. The integration will provide a common experience and background that will be brought back home to prepare a competent and coherent collaboration, ready to produce powerful super-processors. The secondments at Prisma and CAEN will also be ideal to exchange information about simulation studies and developments. UniPi will recruit an ER (less than 10 years experience) with software (C++), GRID and online hardware dedicated tracking expertise. He/she will have to be expert of FTK simulation, an item that is not currently supported at UniPI.

WP5 – Image processing (violet in Schedule Table) Finally the AM system will be used by UniPi for Image Processing. An ER (less than 10 years experience) with specific expertise in this field will be recruited by UniPi the last year. He/she will have to be expert in C++ software and AM technology to adapt the existing AM system to the need of this application. The collaboration with CAEN in this work package is conceived to transfer knowledge to a company that could be interested in future applications if the system turns out to be successful. AUTH is also interested in WP5, since their electronic division is expert in image processing., However, given the complexity of the L1 system they plan to build for muons, they prefer to not officially participate to this WP.

WP6 – Silicon Detector R&D (pink in Schedule Table). This package foresees secondments of Calderini to CAEN to test CAEN power supply market for silicon detectors at SLHC. The work is diluted in the project 4 years, even if it could be executed in a much shorter time. We choose this strategy because the main goal of this work package is to keep the FTK collaboration, in particular CAEN, in contact with the detector R&D evolution, that will be important in all the years of our project, given the fact that this detectors are studied for LHC Phase II, scheduled after 2020. For this reason Calderini's secondment is split into 4 years, even if in total it amounts to only 4 months. An ER with more than 10 years experience will be recruited the second year by LPNHE to work on both subjects Silicon R&D and online tracking. He should have expertise of silicon detectors and of hardware for online tracking. He will participate to the pixel R&D and the running of the FTK test stand that will be installed at LPNHE to allow firmware and test developments in Paris.

Importance of the transfer of knowledge in terms of inter-sectoral issues

The FTK project has been developed in a very long time (R&D started in 1989) with a very low budget per year. One reason for such a slow increase of budget has been the large diffusion of the CPU-farm based trigger strategy at LHC. The FTK research field had to compete with the predominant idea that commercial devices were the best choice to perform the FTK tasks. FTK was never allowed to assign part of the design to a company, because of the high costs. CAEN itself never participated to FTK in the past, even if it would have been natural given its experience in the field and its small distance from Pisa, the place where FTK was born.

The LHC data taking and the machine working conditions changed this scenario. The large number of secondary interactions (high pile-up) that characterized the 2011 run and will increase in the future favour the FTK very powerful parallel architecture. Today It is accepted that FTK can widen the physics prospects of future collider experiments, particularly in the search for new physics beyond the Standard Model. The increase in precision necessary for future measures requires to collect huge samples in extremely hard conditions. This gives increasing importance to parallel computing and dedicated real-time techniques. Not only was FTK recently approved for the TDR, but even more ambitious applications are now conceived. FTK has to evolve from its status of R&D. Now that the project is slowly moving from design and prototyping to production we really need the collaboration of companies with a wide experience in test, integration and commissioning of many complex boards. The complexity increase of FTK compared to SVT at CDF, requires this level of organization also for future possible expansions at CMS or LHCb and spin off outside HEP. In addition a new market is opened to these companies. Intensive, parallel computation based on FPGAs and

specific VLSIs is again a field where electronics has an enormous potential. This is obviously very interesting for the SMEs participating to this network.

Adequacy of the role of researchers exchanged and recruited from outside the partnership with respect to the transfer of knowledge program

The transfer of knowledge will be guided by experienced researchers (physicists and engineers). They have wide experience in HEP experiments and in particular in electronics development as well as trigger and data acquisition (TDAQ). We report here a short description of the personnel that will be seconded, their role in the transfer of knowledge plan and more in general in the project. Additional qualified personnel, that will participate without requiring secondments, is described in section B.4

From **UniPi**, M. Piendibene (laurea in 2003 at the University of Pisa) is the responsible and most expert engineer of the AM system. He worked for several years to the SVT upgrade design, its test and commissioning and after that to the development of the 3 second generation prototypes designed for FTK. The AMBFTK board, currently under design for the new FTK AM chip, is the third existing prototype and will be used in the FTK Demonstrator. S. Donati is an experienced physicist that had an important role in the construction, commissioning and operation of SVT at CDF where he was also the trigger coordinator during the last years of data taking. Piendibene and Donati will transfer knowledge of the FTK project outside UniPi with their secondments, in particular to PRISMA to make them sufficiently expert to lead the Production of new prototypes.

The other key person holding a large experience on SVT and FTK is F. Crescioli (Ph.D. in Applied Physics in 2010 at the University of Pisa). He was very recently recruited by **LPNHE**. He had an important role in the SVT upgrade. He was the person responsible of the Giga Fitter, a single board that replaced the old 12 Track Fitters (9U VME boards) and performed 10^9 track fits per second. Crescioli had also a key role in developing the FTK simulation package, designing the AM chip , and organizing the vertical slice environment for tests.

From **AUTH**, SAMPSONIDIS D. (Ph.D. in 1995 Experimental Particle Physics at AUTH), Assistant Professor and KORDAS, Konstantinos (Ph.D. in Experimental Particle Physics from McGill University in Canada in 2000), Lecturer, are the two expert physicists that will be deeply involved in the Micromegas detector for the upgrade of the muon spectrometer at SLHC, including the Level 1 trigger application. Their curricula below demonstrate the quality of their research, their interest in the ATLAS upgrades, but also their need of learning in the area of FTK applications. Sampsonidis worked as Research Associate at CNRS at Strasbourg,France, and at CERN. In 1996 he joined the ATLAS group of Thessaloniki and worked on the construction of the muon chambers of the muon spectrometer. His research activity is focussed in detector instrumentation and GRID applications. He is actively involved in the ATLAS b-physics group . The results of his research have been published in more than 150 papers in international scientific journals and conference proceedings. KORDAS worked at the CDF experiment at Fermilab, searching for penguin decays of B mesons (after implementing a dedicated penguin trigger at L2 and L3). In 2000 he started his involvement in the ATLAS experiment at CERN, as a Research Associate at LAL, Orsay, France, working on the simulation of the electromagnetic liquid Argon calorimeter. In 2002-2004 he went back to CDF as a Research Associate with the University of Toronto, where he measured the mass of the top quark. Since then he has been working on the ATLAS TDAQ system; initially as a Research Associate at the INFN Frascati Laboratories in Italy, and then with the University of Bern in Switzerland. Since 2010 he has been a faculty member at the Aristotle University of Thessaloniki in Greece. He is still working on the ATLAS TDAQ and participating to physics analyses with an interest in Diboson, and Higgs and physics beyond the Standard Model. Since December 2011 he has been the coordinator of the ZZ->4 leptons analysis. He is interested in being involved in the upgrade projects in the TDAQ and in the detector activities (Micromegas) of the group.

The last experienced researchers that will participate to secondments are the engineer Stefano Petrucci from **CAEN** and the physicist Giovanni Calderini from **LPNHE**. Stefano Petrucci started his activity in electronics in 1997 as power supply designer for nuclear

physics in CAEN; in 2000 he became vice-coordinator of the power supply system design for LHC experiments. In 2004 he became the person in charge for the entire power supply system of all the 4 LHC experiments. Since 2009 he has been the CAEN responsible for regional, national and international funded projects. He has the perfect background to learn about FTK, to lead the integration WP and to help in the commissioning phase at CERN.
Giovanni Calderini, the ATLAS/SLHC LPHNE group leader, had a leading role in the Babar silicon vertex design, test and commissioning.
In addition a team of young researchers will be seconded together with the experienced group. They will provide the manpower necessary to face the big effort of the project. FTK will be a great opportunity for them to gain an important position in this emerging technology that will offer a lot of opportunities during its expansion in ATLAS and to other experiments. This list of curricula shows the young research group quality and background.
From **AUTH Atlas group**:
SIDIROPOULOU O., MS student, studied two years Information Systems and Web Development in a Business and Computing School in Thessaloniki. She also studied Natural Sciences in the Hellenic Open University of Greece from 2006 to 2011. Her BSc thesis subject was “Development of a Data Acquisition System using the GPIB protocol with Labview”. The application was implemented in the Nuclear Physics Laboratory in the Aristotle University of Thessaloniki. She is currently a MS student in Computational Physics in the Aristotle University of Thessaloniki.
From **AUTH electronics group**:
VOUDOURIS L., Ph.D. student, graduated from Physics Department of Aristotle University of Thessaloniki in 2005. In 2008 he received his M.Sc. in Electronic Physics (Physics Department, same University), specializing in Electronic Circuit Technology. His M.Sc. thesis subject was “Design of Reconfigurable Processors”. Presently he is a Ph.D. candidate in the Physics Department, on the subject of “Development of optimal digital systems design methodology on reconfigurable devices”. His research interests include optimal design on reconfigurable devices and real time image/video processing applications.
SOTIROPOULOU C., Ph.D. student, graduated in the Physics Department of the Aristotle University of Thessaloniki, in 2005 with a CGPA 8.88/10. She received a M.Sc. Diploma in Electronics (specializing in the Technology of Electronic Circuits) in 2008 (CGPA: 9.08/10) in the same university. She is a Ph.D. candidate. Her research lies in the area of multiprocessing systems design and methodology for application implementation and hardware/software co-design. She works as a primary researcher for the Greek Ministry of Development and EU funded research project "Corallia LoC: Lab On Chip" as well as the EU funded project “JEWEL: Jordan Europe Wide Enhanced Links in ICT”. She is an experienced programmer in C/C++ & hardware description languages (HDLs).
KONSTANTAKOS V., Adjoint Lecturer, received his MSc Diploma in Electronic Physics (Radioelectrology) in 2005 from the Physics Department of Aristotle University of Thessaloniki, and his Ph.D. degree on the same institute in 2010. He is currently working there as an adjunct Lecturer. He has published about 15 papers in conference proceedings and journals. His research is related to system design of automated low power instrumentation systems, measurements and techniques for the energy consumption estimation and the evaluation of the good operating condition of electronic circuits based on energy measurements, and sensors technologies, including PCB implementation.
From Prisma:
A. SAKELLARIOU, Electrical & Computer Engineering, Aristotle University. Member of the R&D Sector of Prisma Electronics since 2009, experienced in design/simulation of Low-Noise Amplifiers in high frequencies, in design of VLSI subsystems and in the examination of RF amplifiers (CADENCE, Spice, Agilent ADS). Performs schematic capturing and physical layout, of multilayer PCBs, simulation of RF structures, like analog transceivers. Participates in national and EU research programs: NextGenMiliWave (design and development 60GHz communication), Hypersol (developing of hyper-fine solder powders for miniaturized consumer electronics), Nanorganic (development of organic photovoltaic systems).

Dimitrios Dimas Physicist in AUTH and MSc in Electronics Physics in 2008, currently working on his Ph.D. thesis on the development of photonic sensors for wireless sensor networks. Researcher of the R&D sector of Prisma Electronics since 2009. He is mostly involved in software and hardware development especially for embedded devices and firmware. He participates in national and EU research projects: MEMSENSE (Development of Innovative Sensor Systems Offering Distributed Intelligence), MEDOUSA (Autonomous fiber sensors for aquaculture quality control), WELCOM (Wireless Sensors for Engineering Asset Life Cycle Optimal Management), VASIS (Value Added Services Integrated System Based on Optical Sensors of FTTH Infrastructure).
K. I. Mermikli, Electrical & Computer Engineering, AUTH. She has been a Researcher in Prisma Electronics since 2010 involved in EU and national R&D projects. Embedded software development Capabilities. She has very good knowledge of C, C++, C#, Java, Assembly, Matlab, Linux, Mac OS X, MS SQL Server, Oracle SQL Developer, SPICE, SPSS. Project Manager in all CERN projects. Currently involved in CERN ATLAS WPSS project.
Kalaitzidis Panagiotis, Electrical & Computer Engineering, Democritus University of Thrace (DUTH). He has been a member of Prisma Electronics since 2007 as Production Manager. He undertakes all Space & Defense complex projects as well as CERN productions. Experienced in production materials and electronics board behaviour in hard environment. Highly skilled in setting up test kits and run functional tests on PCBs and/or electronic devices. He has very good knowledge of Embedded programming (C, C++) and programming with PHP. Currently involved in CERN RD51 manufacturing and test project.
TRAININGS: in addition to the scientific and technical transfer, broader trainings (e.g. communication, language training, and managerial skills) will be naturally available at our participant institution. In particular some specific trainings are planned in the network to benefit the personnel of the participating institutions. They are described in Section B.4.

Seconding/recruiting will be done under an employment contract with full social security coverage (Type A), with some exceptions of secondments of ER Researchers that are permanent staff, will have multiple short secondment stays during which they will continue to receive their usual salary from the home organisation. These researchers will be seconded under a status equivalent to a fixed amount fellowship (Type B, identified in table B.8).

	Secondments						***Newly Recruited Researchers***			
	Early-Stage Researchers (0-4 years)		***Experienced Researchers (<10 years)***		***Experienced Researchers (>10 years)***		***Experienced Researchers (<10 years)***		***Experienced Researchers (>10 years)***	
	Researcher-months	*Researchers*	*Researcher-months*	*Researchers*	*Researcher-months*	*Researchers*	*Researcher-months*	*Researchers*	*Researcher-months*	*Researchers*
1 Unipi	4	2	6	2	0	0	38	2	0	0
2 CAEN	6	1	17	3	28	5	0	0	0	0
3 CERN	2	1	0	0	6	1	12	1	0	0
4 AUTH	0	0	6	3	0	0	24	1	0	0
5 PRISMA	0	0	8	2	6	2	0	0	0	0
6 LPNHE	0	0	0	0	0	0	0	0	12	1
Total	12	4	37	10	40	8	74	4	12	1

B.4 IMPLEMENTATION (maximum 10 pages)

Expertise / human resources / facilities / infrastructures to achieve the research and exchange of know-how and experience. Fit between capacity of host and size of support requested. Adequate exploitation of complementarities and synergies among partners in terms of transfer of knowledge.

Complementary competencies are distributed among the participants and these competencies reflect to their participation to work packages, summarized in the table below.

WP participation Table

	wp1	wp2	wp3	wp4	wp5	wp6	wp7	wp8
	Prototyping	Integration	Commissioning	Simulation	Image Processing	Silicon R&D	Outreach	Workshops & Trainings
PRISMA	✓		✓	✓			✓	✓
AUTH	✓	✓	✓	✓			✓	✓
UNIPI	✓	✓	✓	✓	✓		✓	✓
CAEN		✓	✓		✓	✓	✓	✓
LPNHE	✓	✓		✓		✓	✓	✓
CERN	✓		✓				✓	✓

We describe here the expertise of each institution and their participation to the activities. The transfer of knowledge among them is fully described in Section B.3.

(1)- The **University of Pisa** (UNIPI), tightly collaborates with INFN Pisa and had a leading role in the Associative Memory technology since the beginning of its story in 1985. The collaboration coordinator, Prof. Mauro Dell'Orso, was one of the two original proponents of the Associative Memory (M. Dell'Orso and L. Ristori, NIM A 278, 436, 1989: VLSI Structures for Track Finding). He also was the creator of the FTK processor for LHC with Paola Giannetti (INFN director of research) . Mauro Dell'Orso, managed the AM chip and the board production for SVT at CDF and did the same job for the SVT upgrade in tight connection with INFN Pisa. This involved the production and assembly of hundreds of boards and thousands of AM chips. He has the scientific and management competence for the proposed scale of the project. Many different 9U VME boards were developed for the original SVT processor, strongly based on the use of Field Programmable Gate Arrays (FPGA) and Complex Programmable Logic Devices (CPLD). The test procedures to validate the chips and the boards were developed and performed in Pisa. The Pisa group installed the system at Fermilab and developed the software for its running, monitoring and diagnostics. The group developed the physics case for the SVT proposal and a realistic simulation of the system to predict the SVT prospects to produce B-physics results. The performance of the real system was as good as expected from the simulation. The system was installed without particular problems at CDF. The original SVT system has been taking data since the year 2001. The Pisa group participated actively in the data taking, the b-quark trigger definition and evolution and finally to several B-physics analyses. In conclusion, the group had a leading role in b-quark physics at the Tevatron and in the related technologies. It had wide experience in all phases of this project. M. Dell'Orso with P. Giannetti created and still have a leading role in FTK: P. Giannetti is the Deputy Project Leader and responsible of the Italian funds, working together with Mel Shochet (University of Chicago) the Project Leader and responsible of the USA funds. M. Piendibene, whose role and expertise is described in section B.3, is the engineer responsible of the AM system since the CDF developments.

Giovanni Punzi and Simone Donati belong also to UNIPI. Both had an important role in the SVT project and the physics produced by the device. Giovanni had, with Michela Del Viva

(University of Florence), the original idea of the use of associative memories to emulate the brain work. Giovanni Punzi and Michela Del Viva will work together on the application of the AM technology in this area (WP5) involving CAEN that will learn about this new field for possible future applications. Giovanni Punzi is also leading a collaboration that is studying the possibility to apply the AMBSLP to LHCb L1 trigger. Finally Chiara Roda is the group leader of ATLAs in Pisa.

(2)- The **LPNHE** Laboratory in Paris has a long tradition in silicon detector development. Giovanni Calderini, the ATLAS/SLHC group leader, had a leading role in the Babar silicon vertex design, test and commissioning. The group has been involved in R&D for the SLHC detector upgrade and in the production for the IBL layer that should be installed in 2013 inside ATLAS. The LPNHE has important responsibilities, as the coordination of the ATLAS planar pixels test-beams and the pixel device simulations. Very recently the LPNHE recruited Francesco Crescioli who was part of the FTK Pisa team and will join Paris in May 2012. Paris will join FTK exploiting Crescioli experience. Crescioli had a very important role in the SVT upgrade at CDF, where he acquired all the necessary expertise. In FTK he is one of the main designers of the new AM chip and he has been up to now the person responsible of the Vertical Slice, the first, small FTK prototype that will be installed in 2012 in ATLAS. Inside this proposal LPNHE (a) will learn on FTK with the contribution of Francesco and the Pisa colleagues (b) will participate to the system design, integration and simulation (Wp1, Wp2, Wp4), in particular with Crescioli's secondments to CAEN (c) will pursue its detector development and tests activity coming in close contact with CAEN for the installation of the silicon sensor test-bench and the parallel development of power supply products and test stand tools. This will allow future involvements of CAEN in the long term SLHC upgrades. This will be supported by Calderini's secondments to CAEN. In addition an FTK test stand will be installed also in Paris to allow further developments there.

(3)- **CAEN** has a very wide experience in developing instruments and electronics devices for high energy physics. It had a very important role in the development of the readout and power supplies for the LHC detectors. Stefano Petrucci, the Scientist in Charge in this project, has 15 years of experiences in CAEN power supply projects design and organization, being the head designer of several PS modules currently used in LHC and the vice PS office head for many years. Now he is the Caen Innovative Projects Division Manager. This proposal is the opportunity to build this new collaboration and make CAEN an important center where (a) we integrate all the already available prototypes (the already existing AMBFTK) to exercise the collaboration and prepare the demonstrator, (b) we integrate the new boards (developed in Italy and in USA) as soon as they are available, (c) we test them, (d) we develop the needed firmware and software. After the demonstrator successful implementation, the FTK system detector coverage will have to grow and after that the computing power of the system will have to grow again, following the needs imposed by the growing LHC instantaneous luminosity. This means that production of new boards can be divided into steps of production that will be followed also by steps of commissioning at CERN. UNIPI & LPNHE will transfer their knowledge about the project to CAEN and collaborators that will come there to work on the integrated system. CAEN will offer its experience on large scale system integration and will develop custom power supplies for the FTK core crate that should house boards for a total weight of 40 kg, provide a very large power for the AM system (~5 kWatt per crate) and very good transparency to air for racks where cooling should be very efficient.
CAEN will also collaborate with the LPNHE on the development of special low-noise power supplies boards for the SLHC pixels. One of the problems of the trackers in the SLHC phase will be the fact that after radiation damage the system will need to be powered to increased tension, larger than 1000V, to preserve the charge collection efficiency. Even at below-zero temperature, such bias voltage will determine a leakage current of many uA, which the high-voltage board needs to sustain.

(4) The **University of Tessaloniki** (AUTH) is joining the FTK project in 2012. They will have to learn almost everything about FTK but on the other hand they are perfect collaborators since: (a) The ATLAS group, led by Professor Chariclia Petridou, is very interested to learn the AM system functionality. They would like to use this technology for triggering at L1 on upgraded muon chambers for SLHC Phase 1; they are part of the RD51 collaboration for R&D on gaseous micropattern detectors and of the MAMA project for the ATLAS muon upgrade using micromegas. They provided a sizable contribution (over 10%) to the past construction of the precision tracking muon chambers of ATLAS and now they are involved in the muon detector upgrade, in particular to the micromegas technology. They also have a wide experience of the ATLAS TDAQ system and very strong competencies in related software. Kostas Kordas, the Scientist in charge of AUTH, has worked in the event building software with multi-threaded C++, online montoring of the data collected from the muon detectors. The group has a good laboratory infrastructure and access to the Grid facilities of the University, in addition to very good experience in software simulation; (b) Moreover, a group from the Division of Electronics and Computing, led by the Associate Professor Nikolaidis, will participate. NIKOLAIDIS Spyridon is the demonstration of the high level research capability of the AUTH participant in the electronic sector. Employed in the area of digital circuit and system design, his current research interests include: modeling the operations of basic CMOS structures, development of analytical expressions for the propagation delay and the power consumption of CMOS structures, design of high speed and low power digital circuit and embedded systems, modeling the power consumption of embedded processors. He is author and coauthor of more than 130 scientific articles in international journals and conference proceedings while his work has taken more than 400 references. Two articles presented in international conferences were achieved honorary awards. He also contributes to a number of research projects funded by European Union and Greek Government and in many of them he has the scientific responsibility.
His group has wide experience in (a) high speed and low power system level digital design and FPGA system integration, (b) hardware design and verification (VHDL) as well as (c) Hardware/Software co-design (EDK Xilinx environment) for the implementation of DSP and computationally intensive image/video processing algorithms. The group has developed in house machine vision applications targeting FPGA devices. It is also involved in research in the field of multi-core implementations, design space exploration and application mapping, as well as development of Integer Linear Programming (ILP) models for optimizing multi-core architectures. Their research also targets ASIC design (Cadence) for even higher performance and modelling the power consumption in microprocessors. In conclusion AUTH has all the necessary skills to work (a) on developments (WP1) with UniPi, LPNHE and Prisma. After a kickoff workshop and training in Pisa where the four institutions will meet , secondments between Prisma and AUTH will provide the communication necessary to collaborate on firmware and board design; (b) will offer complementary skills to the FTK integration task since the ATLAS group component is more expert of the TDAQ structure (WP2). Secondments to CAEN will provide the necessary transfer of knowledge; (c) will be valuable in the simulation effort (WP4) given their Grid experience. The two Greek partners AUTH and PISMA will reinforce the FTK collaboration with also an excellent team of young researchers (see section B.3) increasing the design and testing capabilities and allowing further and new applications.

(5) The **Prisma Electronics** (PRISMA) company has a long experience, like CAEN, of electronics development for CERN. They are very active and very interested in all the technical aspects of the project and, as already underlined for CAEN, they could become after these 4 years of common experience in design and small productions, an important reference company to face large productions and the expansion of the technology in more difficult areas like L1 applications. They offer to our collaboration their high quality capability for board assembly, but they will also participate to board design and to firmware development and tests (WP1), collaborating with CERN, AUTH, LPNHE and UNIPI. Prisma will collaborate also to WP4 with firmware simulation, that is very important for debugging.

During our progressive small production steps they will provide board assembly and a first round of simple tests to guarantee the result before sending the material to CAEN for integrated tests. In particular the vertical slice, the FTK test stand, will be provided by Pisa to perform at the company the simple tests of boards just assembled: (a) the motherboards (AMBFTK first and AMBSLP after) for the AM system, (b) the LAMB mezzanines where AM chips will be placed, (c) the FTK_IM mezzanine for receiving and clustering hits from the detector. Each board will need its own setup and user-friendly software at the company. Personnel from Pisa will visit the company at the beginning to transfer all the necessary knowledge and install the test stand. Periodic visits will follow during the progressive production of different boards to collaborate.

(6) Finally **CERN** has a very natural role for commissioning (WP3). It will be the final destination where the hardware will be installed. A period of commissioning will follow each step of partial production. Stefano Petrucci from CAEN will be seconded to CERN in these periods for commissioning. CERN is, however, an interesting collaborator also for a different reason. The TE-MPE-EM section (Technical Engineering Department – Machine Protection and Electrical integrity - Electronics Modules) provides CERN-wide support for the layout, production and assembly of printed circuit boards, flexible circuits, hybrids and fine pitch detectors. The group has three areas of interest: (a) Electronics Design Office, (b) Photolithography & Microconnectics Technologies and (c) Assembly Workshop. F. Formenti is the TE-MPE-EM Section Leader, Betty Magnin, our scientist in charge for CERN, is the Design Office Leader.

The FTK collaboration has commissioned in the past the placing and routing of our boards to the CERN Electronic Service that uses the same CAD (Cadence) used in FTK collaboration. This Service is really excellent. The personnel there has a very advanced knowledge of the Cadence tools. For this reason we aim to collaborate again in the development of our future boards that are much more challenging than in the past. As described in section B.3 a recruitment will be done to obtain this transfer of knowledge and at the same time to get professional designs for our prototypes.

The research funds associated to ER's contracts and secondments will be used to pay (in addition to standard EU collaboration activities, like training, networking, dissemination, outreach, note that all Institution will participate to WP7 and 8) for design at the companies, (firmware, boards, power supplies), CERN electronic service Cadence support. In addition to that PRISMA is applying for 10% of the budget as a contribution to succeed to buy Cadence for board design (Category 6: Small Equipment, for SMEs only).

Schedule, work packages, deliverables, milestones

Here we summarize the list of work packages, including the outreach and transfer of knowledge activities. We give the details of the schedule (timing development), the deliveries and milestones (see also the following tables).

Schedule Table

Year 13	Year 14	Year 15	Year 16
Demons. Prod.+Integr.	Demons. Commiss & Run..	Product. & Commiss.	Product. & Commiss.
SLPL2 production	SLP2 Integr. & Commiss.		
	Study L1 architectures	SLPL1 production	SLP1 Integr.
Simul. for Demo tests	Demo perf. prediction	Simul. for L1 architect.	Simul. for SLP1 tests
		Static Image Process.	Movie Image Process.
Setup CAEN teststand	Test of undamaged FEI4 devices	**Optimization of PS with irradiated Devices**	Test with optimized Powe Supplies

To clarify the schedule we remind that we will work in parallel on different versions of our Processor Unit (PU), corresponding to different stages of complexity and computing power.

The FTK Demonstrator is the first important development. The tested prototypes will be reviewed by ATLAS and subject to approval in 2013 (Milestone N.1 corresponding to the TDR submission in June 2013). It is also expected to be installed and take data in ATLAS after the long LHC shutdown in 2013-14. This data taking will be reviewed and if successful it will enable the construction of the whole processor, that will grow by steps following the LHC instantaneous luminosity grow. This corresponds to the first important set of deliveries (see table B4.2). The integration of the Demonstrator will be an important training activity for the whole collaboration and a very important period to transfer knowledge from the UniPi/LNPHE groups to the rest of the participants, providing a strong common experience to all of them.

Table B.4.1 Work Package List

Work package No	Work package title	Type of activity (e.g: research, training, transfer of knowledge, dissemination, etc.)	Lead beneficiary No	Lead beneficiary short name	Person-months (only ESR, ER)	Start month	End month
WP1	Prototype Production	research	5	Prisma	60	1	36
WP2	Infrastructure &Integration	Training	2	CAEN	48	1	48
WP3	Commissioning	research	3	CERN	24	12	48
WP4	Architecture Simulation	research	1	UNIPI	36	1	48
WP5	Image Processing	research	1	UNIPI	24	25	48
WP6	Silicon Detector R&D	research	6	LPNHE	12	1	48
WP7	Outreach	dissemination	4	AUTH	12	1	48
WP8	Workshops & Trainings	Transfer of Knowledge	4	AUTH	12	1	48
				TOTAL	228		

The design of the SLP2 for Level 2 applications is strongly based on intense exploitation of the modern high performance serial links. It will be performed in parallel exploiting the most update FPGAs, to be ready after two years to compare the two developments (AMBFTK and AMBSLP2) before starting to enlarge the FTK detector coverage in ATLAS with the following productions/commissioning periods. A relevant Milestone is related to this important decision: which will be the final PU to produce the full ATLAS processor. The following production and commissioning phases will complete the tracking coverage and the computing power if requested by the increasing detector occupancy and instantaneous luminosity (more PUs in the system).

The simulation of the hardware functions will be necessary in all phases to provide a powerful tool for validation. The simulation predicts the PU output as a function of its input and this prediction is compared to the hardware output until they are perfectly equal. Multiple deliverables of this task are foreseen for the various different integration periods.

After two years of integration/design/commissioning the collaboration will have acquired a strong common background and will be able to move to the much more complex Level 1 application. During the first two years the experience on L2 will be used to study possible architectures for L1. Simulation of the chosen architecture (SLP1) will be fundamental before and during the hardware development.

Table B.4.2 Deliverables List

Del. no.	Deliverable Title	Work Package no.	Person months (ESR/ER)	Nature	Dissemination level	Delivery date
2.1	FTK demo Integration	WP2	24	P	PU	12
3.1	FTK demo commiss.	WP3	6	P	PU	24
1.1	SlpL2 production	WP1	24	P	PU	12
2.2	SlpL2 integration	WP2	12	R	RE	18
3.2	SlpL2 commissioning	WP3	6	P	PU	24
1.2	FTK production	WP1	6	R	RE	32
3.3	FTK commissioning	WP3	6	P	PU	36
1.3	FTK production	WP1	6	R	RE	42
3.4	FTK commissioning	WP3	6	P	PU	48
1.4	SlpL1 production	WP1	24	R	RE	36
2.3	SlpL1 integration	WP2	12	P	PU	48
5.1	Static image process.	WP5	12	P	PU	36
5.2	Movie processing	WP5	12	P	PU	48
6.1	Setup of the testbench and standard characterization	WP6	2	P	PU	24
6.2	CAEN Power supply tests and detector characterization	WP6	2	P	PU	48
4.1	Simulat. ready for tests	WP4	18	R	RE	12,24,48
4.2	Expected Process. Unit performance prediction	WP4	18	P	PU	24, 36
7.1	IAPP project open day	WP7	4	E	PU	7, 19, 31, 43
7.2	Workshop day	WP7	4	E	PU	5, 17, 29, 41
7.3	Summer school Week	WP7	4	E	PU	6, 18, 30, 42
8.1	FTK Workshop	WP8	6	E	RE	1, 13, 30, 46
9.1	Trainings	WP9	6	E	RE	1, 5,9,19, 29, 47

R = Report, **P** = Publication, **E** = Events, **PU** = Public **RE** = Restricted to a group specified by the consortium (including the Commission Services).

In the last two years the most important decision will be taken for the processors dedicated to HEP. We will spend time using the original system, the vertical slice produced by Pisa in the past, to study the image processing application. We have two important deliveries in the work package 5 corresponding to two publications showing that the AM system can reproduce the low level brain function dedicated to input data strong reduction maintaining all the relevant image information. The first publication will be for static images and the second one will be for movies that should be processed in real time. The relative milestone will be considered attained if publication of the results are accepted on peer reviewed Journals.

The time evolution of WP6 (Silicon R&D) is diluted in short periods covering the four years to allow the FTK collaboration and CAEN to keep in contact with the ATLAS work of the silicon R&D during the whole time of the project. For this reason the first year Calderini will simply install the LPNHE test-stand at CAEN (Viareggio, Italy) and will perform its characterization using standard pixel sensors already tested during past ATLAS test beams. This will allow to reproduce the results and will provide a benchmark, complete of a set of measurements (first deliverable), to be compared to what can be obtained with the CAEN power supply products. The second deliverable is represented by the results obtained after an optimization of the system powered by CAEN instruments. Calderini will install them in the test stand and will perform the characterization of the same pixel modules with the new hardware. Special tests will be made at different temperatures and using irradiated sensors, to study the behaviour of the new hardware when connected to damaged detectors. The power supply optimization and installation will be done during the third year, while the program of measurements will be completed during the fourth year.

Finally we have two work packages dedicated to the outreach, transfer of knowledge and training activities. We plan one annual occasion for each of the listed corresponding deliveries:

IAPP project open day: the FTK labs will be open to the public to show the racks, crates, boards and chips developed by the collaboration. Teachers (the fellows in particular) in front of posters in the lab will describe the importance of the real time analysis performed on FPGAs (a new type of computing) to make sophisticated decisions in few microseconds, for HEP experiment triggers as well as for other applications outside HEP. The programmable logic power based on real time parallel computing will be described with examples. The importance of “pipelining” and “parallelism” will be described in detail with examples as being the key features of our computing model. Simple CAD stations (Xilinx and Altera systems) will be provided to visitors to develop their own simple logic. Logic examples already done will be provided for people interested only in the implementation inside the chip, not in the logic development. The goal is to let them understand how easy and powerful the use of these tools is.

FTK Workshop day: a set of seminars and lectures will be provided to university students on trigger for HEP experiments and FPGA applications outside HEP. This will be also the occasion to announce the *Summer school week* plan for the year. Few students will be allowed to spend a week during summer in one of the partner laboratory, in particular at CERN.

Finally Trainings and FTK Workshops will be activities devoted to our collaboration. Each institution will offer some trainings to the community:

UniPi: “The AM system”. At the beginning of the first year, as the opening event of the network, a set of seminars will be given on (a) global architecture and data rate problems, (b) specific logic and existing boards analysis, (c) AM chip status and future evolution, (d) existing tests, laboratory tools and test stands, (e) knowledge of the collaboration (f) career opportunities and importance of managerial skills inside the FTK project. This is also a nice

occasion to meet all together at the very beginning (kickoff workshop followed by a more detailed kickoff training).
PRISMA: **"**overview of the Prisma projects". Prisma will offer trainings based on its project experience. It is specialized on intelligent sensor wireless networks and develops innovative products for condition based maintenance in industrial and maritime environments. It develops embedded devices for data collection, analysis and data acquisition software with Novelty detection algorithms. Prisma expertise is focused in signal analysis algorithms for embedded devices, novelty detection systems, self learning algorithms, power autonomous systems with micro generators and organic photovoltaic, developing optical sensors connected to wireless networks and implementation of new transmission and communication protocols.
CAEN will offer 3 trainings: "Silicon Photomultiplier read out – SiPM", **"**past experience at LHC" and "overview of EU projects ongoing at CAEN".
LPNHE: "Experience on silicon detectors: evolution from LHC to SLHC" with visit to the lab and learning to work in clean rooms
CERN: "Technology: (a) CERN practical experience for the development of high density electronics boards, (b) kow-how for quality assurance practices in board manufacturing", with visit to the TE-MPE-EM infrastructures.
AUTH, based on the experience of the electronics division, will offer these trainings: (a) a training on FPGA technology and its applications with topics such as "Embedded System Design Using FPGA Technology", "VHDL Verification Techniques" and "Design Exploiting FPGA Resources". The training will include laboratory sessions using the existing equipment of the electronics division, such as training FPGA boards and design suites; (b) a training on "Machine Vision Implementations for Lab-On-Chip applications". The electronics division plans also to present the FTK project in an International Workshop organized by the group in Thessaloniki on Modern Circuits and Systems Technologies.
We will try to introduce an exercise with AMs in the programme of the yearly winter school ISOTDAQ (International School on Trigger and DAQ), so as to difuse the technology to the young generation in our field

The common Milestone for the two working packages WP7 and WP8 is a complete set of web pages dedicated to the FTK collaboration activity description, part of it open to the large public. It is expected that this page will be updated in three occasions during the project.

Table B.4.3 List of Milestones

Milestone number	Milestone name	Work Package(s) involved	Lead Beneficiary	Expected Date	Comments
1	FTK TDR	wp1, wp2	5, 2	20	FTK prototypes approval
2	Demons. Success	wp3	3	24	Demonstrator running flawlessly
3	SLP/Demo	wp2	2	24	Compare & Choose technology
4	SLP/Demo simulation	wp4	1	24	Ability to reproduce the hardware functionality
5	SLP1	wp1,wp2	5,2	48	Tested PU for L1
6	Image proc. Ok	wp5	1	48	AM demonstrated able to filter natural images
7	Silicon R&D	wp6	6		
8	Web site	wp7,wp8	4	6,18,30	Web site for dissemination

We will create and maintain a dedicated webpage also for the ongoing research. All our meetings will use the Indico software. Secure access to both the webpage and the Indico pages is guaranteed. In addition, the communication among the partners is assured through telephone-conferences, videoconferences and a dedicated e-mailing list. All these tools will be extensively used throughout the execution of the project. The communication among the members of the partner institutes will be further enhanced during the various workshops and tutorials, which will bring together many experts from different institutes. Once per year, a conference-like meeting will take place with a wide participation of the network partners and presentations of latest results. The young members of the network will be especially encouraged to contribute in the organization of these events.

Management plans: demarcation of responsibilities, rules for decision making.
We propose a management scheme of the network that consists of two boards: the *Steering Committee* that will be primarily responsible for the financial and administrative aspects of the network and the *Scientific Board* that will be in charge of the scientific operation of the network, the implementation of the training program and the recruitment processes in consultation of the *Steering committee*.

o *Steering committee* (SC): it will be responsible of the financial management of the project and the dissemination issues. They will play a consultant role in the selection of the network researchers. One member of the *Steering committee* will be appointed as gender officer. The gender officer will also be present during the selection procedure of the researchers. Each partner will appoint their representative to the SC who will be chosen to have a longstanding experience and international reputation in leading research teams and multi-institute projects, in order to guarantee the smooth operation of the network. The *Steering committee* will meet twice per year to deal with administrative issues of the project.

o *Scientific Board* (SB): the *Scientific Board* will (a) ensure the implementation of the network's scientific and training program, (b)monitor the progress of the research teams, (c) ensure good communication and exchange of information among the teams (d) be responsible for the recruitment process in consultation with the SC. The composition of the SB will consist of the representative of each participant institution and the work package managers (see below). The SB will meet regularly every four months to assess the progress in the research and training aspects of the project and communicate the results of the closed sessions to all members of the network. The SB will submit a report on project progress to the SC, after each SB official meeting (each 4 months)

o *Work Package managers*: for the implementation of the milestones and deliverables of each WP, one manager per WP is appointed. The WP managers will report regularly to the SB on the progress of the project paying special care to match milestones and deliverables.

The *Steering committee* will be chaired by the project coordinator and will vote for a deputy coordinator.

Recruitment / secondment strategy - The recruitment of the ERs will follow the European Charter for researchers and the Code of Conduct for their Recruitment. The posts will be widely advertised to the international scientific community via scientific magazines and websites. The positions profile are already established within the network by the project very well defined needs and will be centrally advertised. The announcement of the ER posts will take place as soon as the negotiations of the contract start.

o ER recruitment: We plan to hire the ER as established by the table B.8 table following the schedule of the project. The required expertises are fully described in Section B3 for each recruitment. The curriculum vitas of the candidates will be circulated to all members of the Institute Board and a short list will be drawn based on their input. The short- listed candidates will be invited for an interview either to the host institute or to CERN, whichever is less costly. We will try to group the interviews when possible, to minimize traveling costs, or perform them via telephone conferencing.

Career development strategy: the ERs will have a personal supervisor, with whom they will discuss and establish a career development plan, which will be followed up, discussed and updated regularly. Given the healthy participation at each institute in the network of the experienced staff, the good supervision of the young researchers is guaranteed.
The progress of ERs will be followed closely and the supervisor, in the spirit of maximizing their career prospects, will make suggestions/corrections. They will be strongly advised to take an active role in training activities. A 6 month planning of their work is foreseen and a yearly report to the institute on their progress will be given. As described in the previous sections, distinct tasks and responsibilities will be attributed to each of the ERs of the network. On the limit of the finality of the recruitment, the tasks will be assigned to the ER's taking into account their personal preference. The supervisor, in consultation with the local coordinator and on the basis of the importance of their scientific results, will advise on the ERs participation in workshops and conferences and on the presentation of the scientific results. High priority will be given to ERs to present the results achieved within the network in collaboration meetings and international conferences. The aim is to give the experienced researchers the necessary visibility that will help them in their future career.

Working conditions
Organization and continuous scientific discussions are the bases of the high research productivity of the relatively small, but excellent research groups participating to this network. Each member has individual responsibilities and is required to discuss its work weekly with the rest of the correlated group. Seminars in front of the whole scientific community of each institute are periodically required. This style is a strong stimulus to acquire clarity, independence, management capability, and presentation skills. We care to provide a continuous stimulus to improve "leadership capability". Presentations at conferences are strongly encouraged, even the dissemination of ideas and results not currently popular in the HEP community (FTK, for example, suffered for a long time of the large LHC online farms competition). All the participating institutions are intellectually very active and offer seminars and possible interactions on a wide range of topics in high energy physics, technological areas related to the experiments/accelerators, and also in totally different fields. The fellow work will have the opportunity to be presented to a large and international scientific community. Independence and management capabilities are strongly encouraged and rewarded.

IPR strategy –
Most of the work performed in this project is just for research, to produce hardware that will be installed into LHC experiments and will not go to the market. There are few exceptions, very easy to handle since in these cases the work is done by a single institution and the intellectual property belongs to it. An example is the CAEN power supplies developed in this project for the FTK crate and for the high voltage bias of the silicon sensors. It will be CAEN property and will be offered also on the market.
A particular case is the AM-based image processing activity, since it could bring to interesting applications that could in the future go to the market. The intellectual property of the idea belongs to Giovanni Punzi (Univrsity of Pisa) and Michela del Viva (University of Florence), as demonstrated by past conferences and publications. The work performed in this project will be only a proof of feasibility, whose intellectual property will belong to UniPi and Michela del Viva that will collaborate on it. It will also be tested at CAEN in the integrated system, for transfer of knowledge to the other participants. No application will be pursued in this call but the collaboration with this project could develop a strategy for possible future applications of it. The intellectual properties of future developments will be treated into eventual future projects.

B.5 IMPACT (maximum 4 pages)

Impact on the innovation potential of the European Research Area; in the relevant fields, description of potential applications

The impact will be extremely important on the innovation of all the LHC experiments data taking. An innovative paradigm in real-time analysis (few microseconds latency) of complex events is slowly emerging in a field where large farms of CPUs have been believed for years the only solution. Our new strategy has a big impact because shows a widening of the physics possibilities in future collider experiments, particularly in the search for new physics. The search of new physics becomes each year more difficult since the Standard Model has been continuously reproduced with increasing precisions. To find deviations is becoming a really challenging task.

The LHC detectors are ideal for the study of physics that includes heavy objects such as top and bottom and tau, the so-called third generation, important in the search for new physics. Thanks to the precise measurement of the momenta of the charged particles and the identification of vertices of decay of quark b a few hundreds of microns from the primary vertex, efficient selections are possible with large factors of suppression. Unfortunately, up to now this wealth of information is seldom used on-line, where it would be invaluable. Any inefficiency in level 1 or 2 will be unrecoverable and can heavily influence the richness of the samples. In fact, the high rate of event production in hadron colliders, coupled to a much lower data acquisition bandwidth requires tight selection criteria from the very beginning. Complete tracking at very high rate is totally missing today into those experiments, while the pile-up environment is clearly demonstrating the importance of it to realize these tight selection criteria maintaining high efficiencies. Sometimes the experiment decides to apply bland low level selections to avoid losing too much efficiency, but this approach also requires huge and prohibitively expensive CPU farms. This kind of problem is already evident at the LHC, and will be much more relevant in the next generation of experiments (LHC upgrades), to become one of the main limiting factors in the production of physics results. This research shows that current technology allows the researchers to design a high performance trigger, based on intensive track reconstruction, sensitive to secondary vertices, cost effective and affordable for all latencies allowed.

The achievement of the planned objectives requires an integrated approach of various disciplines in constant interaction with each other. Advanced hardware and software design, expertise in Physics at the frontier of current knowledge are involved. The overall result of such convergences is constituted by an analysis model that is sophisticated, flexible and able to adapt to a wide scenery of applications. The expected improvement in the ambit of real-time performance stems not just from a purely technological aspects (construction processes, integration), but also from a critical review of the well established architectures. This leads to solutions of great interest for the advancement of knowledge in specific fields and in Fundamental Physics, with potential original deployments in many areas of the Enabling Technologies. In the following some specific expected results will be described, and then the innovative potential of this project as a whole will be illustrated.

The overall result requires a specific number of successes on various fronts. In particular for what concerns more closely the hardware, we plan to build a prototype of the SLP, reliable, capable of supporting even the first level latency of selection in ATLAS and other experiments. The processor will have a modular, expandable and configurable structure, depending on the latency of the experiment. To be effectively used at its best, the power of SLP must be accompanied by an I/O architecture adequate to the huge flow of real-time data. Serial connections are a relevant item to this project. An important result will be the test of serial channels present in the FPGA, pushing the limits of current technology. Future developments could provide us real-time serial links with bandwidths of 10 Gb/s. This figure could double with the availability of new generation devices. The expected results are the validation of algorithms aware of the internal structure of the device, able to moderate the effects of the radiation and able to increase by orders of magnitude the overall reliability of the circuits.

However, even with the use of highest speed serial channels, the I/O poses severe limitations to the overall performance of SLP in applications with high data flow, such as those on the pixel detectors of new generation. One of the most interesting expected results is the validation of highly parallelized implementations of cluster-finding and adaptive algorithms to reduce in a smart way the amount of data to be transferred (FTK_IM). As far as the adaptive algorithms are concerned, those adopted by the visual system and then optimized by the natural evolution, are expected to automatically select the salient features of the clusters being in the midst of all the possible patterns generated inside the detector. Today we implement the cluster finding inside the FPGAs (the FTK_IM) and we optimize it, but the natural evolution for Phase II at LHC would be the transfer of these algorithms inside the detector itself. This will be a fundamental step in the direction to have an "intelligent" experimental apparatus, in which electronics is not limited to the reading, compression and transfer of data, but play actively in the clustering, in the selection of tracks, and potentially in the detector projective schemes on the basis of the phenomena of interest.

The architecture of the SLP is based extensively on the serial link to make the associated database expandable and adaptable to the particular cases of interest. The availability of high-speed serial links and resources measurable in millions of logic gates in modern FPGAs opens the possibility to the development of embedded processors that include in their set specialized instructions for conducting remote operations. This would virtualize access to hardware resources available on other chips, beyond the conventional concept of network. Such an architecture would bring the processing back on the detector, entrusting a semi-remote cloud for the more challenging tasks. Such a scenario is similar to the pervasive computing models currently used by smartphone. Their more complex features (voice recognition, OCR, translation, ...) are carried out by clusters of networked servers. Similarly it could happen in real-time applications, with the availability of real-time connections, such that resources belonging to another processor are made accessible in a transparent and deterministic way. The concept is a sort of extension of the hyper-threading, used in conventional microprocessors. In this case the concept would be extended to distributed architectures linked with real-time connection. These results are prosecuted within our project, but the project set the basics and can assess the feasibility.

We want to emphasize that some results are also important for recovery of corruption of configuration logic in devices, like for example FPGAs. The correction of corrupted segments of the configuration can be fixed through an associative search not dissimilar to the one made by SLP for the selection of tracks. With a proper database and observing tight protocols for use of internal resources, it would be possible to compare the corrupted segment with a portfolio of legal cases, allowing immediately to restore the proper configuration. The analogy with genetic applications is obviously very strong and it calls for an accurate analysis of possible applications of SLP and AM in this area.

Last, and most interesting test of our computational power, is in the field of vision: to create a device that can automatically analyze and without external supervision static natural images and movies in real time, extracting highly compressed (over 95%) representations but still full of all the salient features of the original image. The realization of such a device is important for the validation of the algorithm for the extraction of features proposed and to prove its effective chance of implementation. In fact, the hardware implementation of a model of visual analysis is not a standard practice in the study of vision. Models are in general accurate and elegant, yet very hard to implement. The realization of a hardware device based on the proposed model would also be an important step towards automatic analysis of the salient features in artificial images such as x-rays or satellite images. These images normally require a long training and expert supervision, while our algorithm allows for an automatic tuning and continuous adaptation. These studies will provide inputs to researchers that aim to understand the type of information and neural mechanisms involved in early stages of visual analysis in humans, essential to trigger automatic responses and behaviours to adapt and to move towards potential interesting or dangerous stimuli. The application of architectures born to perform pattern-matching to the study of these mechanisms represents

a powerful tool to better understand nature and function of human physiology, giving a boost to this field.

Finally, as already mentioned in section B2 “Inter-sector issues”, these computing techniques could have applications in all the fields where a huge computing power is necessary for fast real time results. Some examples are medical imaging for real-time, fast diagnosis, astrophysical and meteorological calculations, robotic automation, and security applications.

Provision to develop new and lasting inter-sector collaboration. Extent to which SMEs contribute to the project.

As already explained before, the FTK project exists since 1998. It had a long R&D life with very low budget that didn’t allow scientific contacts or collaborations with the commercial sector. This European project would give the scientific sector the capability to meet for the first time with the commercial one. We will build a new team with complementary expertises able to optimize the past year efforts and to bring to production and commissioning our FTK processor first and more complex evolutions after FTK. In fact this collaboration will be ready to export the technology in new more challenging directions. The use of associative memories for level 1 muon selection in the micromega chambers will be faced already during our project, thanks to the interest of the AUTH participant. This effort can be used for the more challenging task of full tracking at level 1, an item to which CMS and LHCb are seriously thinking already today.

Prisma and CAEN have a strong participation in this project since they are interested to gain an important role not only for the production and commissioning of FTK in Atlas, but also for the possible following evolutions. CAEN becomes the integration heart and participates to the commissioning, while Prisma, in addition to the CAEN activities, joins also the board and firmware developments. PRISMA will have the opportunity to become familiar with new software design tools, to cooperate with experienced engineers from all academic institutes, to learn more on designing PCBs to be used for hard work in a complex environment, to find out on new components functionality (AMs), to produce prototypes cooperating and training researchers and to design-perform high specs functional tests.

Moreover, PRISMA sees a unique opportunity to establish partnerships and pathways with institutes and industry participating in the project for future cooperation. Actually both the two SMEs will have the opportunity to become the main places where assembly and preliminary tests will be performed for all future productions, they will be also able to produce firmware and test procedures, and the maintenance of the hardware (a lot of boards if there will be the transition from Level 2 to Level 1 full tracking).

The WP6 open also a new opportunity for CAEN, if its power supplies will be easily adapted to silicon detectors in future SLHC applications.

Strategy for the dissemination and exploitation / commercialisation of the results

It is important for us to communicate our results in these specific areas, because the outcome of the dissemination could provide new applications and new research activities, that will also reinforce our team. Some examples are listed here:

(a) LHC experiments: we continuously disseminate our developments in workshops, conferences, publications, proposals, fighting to let understand people the importance of our new computing technology. The availability of data and the high pile-up LHC events clarify the importance of new technologies. This is a particularly favourable moment to demonstrate on benchmarks the advantages provided by FTK-like structures. We will continue to participate to debates and conferences showing (a) our “almost offline tracking performances” obtained in a average full event processing time of ~30 microseconds (b) our very good capability to reconstruct taus, bs, isolated leptons with high efficiency and very good rejection power of background.

If the processing of static images and movies by our associative memory will be successful we will look for possible applications in some directions, disseminating our results:

(b) Medical applications: we will look for medical images to be processed by our associative memory. We want to see if the relevant features can be extracted efficiently with a large compression of information.
(c) Satellite or video-camera real-time image processing to diagnose possible accidents or dangerous situations in critical positions, continuously monitored. The processor, attached to the video-camera could be able to recognize immediately a movement or a change in the image and set an alarm. We plan to disseminate our results to understand the possible applications as real time alarm for our processor.
(d) Programs searching a large database to recognize features like for example faces or monuments are today quite slow. Providing the compression of information offered by the associative memory to all the images on data bases, would probably make these programs much faster. We will discuss our results with researchers of information science working in this field to understand their possible interest.

Facilitation of sharing knowledge and culture between the participants and external researchers (including international conferences, workshops, training events)
The major innovation of this research project is that research training will be performed in the framework of the development of an advanced technological system. The researchers in the FTK project will have the opportunity to be trained in UNIPI, AUTH and CERN in a peak technology subject, cooperating in a multinational environment. In parallel, they will get the satisfaction to watch part of their individual effort to become part of a prototype, in the advanced production environments of PRISMA and CAEN, that will be commissioned at CERN ATLAS experiment and then to become a product to be used in other Detectors all over the world. The outcome of the researchers effort will be in high level and in multiple dimensions beneficial for both Academia and Industry. Having about 500 institutions, active partners around the world, CERN provides momentum to a more coordinated approach to research training as well as to international recognition of the training and qualifications offered that none can doubt about.

However, the advantages for this new collaboration are certainly not restricted to the scientific transfer of knowledge. Industry will have a key role in training. It can provide qualitative training to the researchers dealing with applied techniques and practices creating preconditions to acquire someone advanced skills and unique experience. Companies involvement will provide the researchers with the opportunity to experience working in industry and they will gain a better insight into their preference with regard to their potential career paths. Moreover our SMEs show a large variety of ongoing projects outside HEP, many of them funded by FP7. They show a larger experience on FP7 projects than Academia that is focalized only on People sector to remain strongly tight to HEP projects. This is a very interesting source of trainings for the Academia researchers, an important stimulus to create spinoff. For this reason we decided to dedicate some of our trainings on the SME experience on their research outside HEP. Apart from these, the two SMEs are also characterized by their experience on handling successfully CERN projects, fact which enlarges the impact the researchers will benefit, working in a focused environment under austere procedures.

Impact of the proposed outreach activities. The *Outreach plan* described in section B.4 is very important in our project for many reasons: (a) to promote communication between the scientific community and the general public and to increase awareness of science. These will be occasions to show how important the HEP experiments are not only for the advancement of the nature knowledge, but also for the technological advancement. (b) to allow clever students to come in contact with the “big science” and let them know LHC and the experiments that they could join for their own future research activity. (c) to spread the use of programmable electronics (FPGAs) has new computing facilities.

STOP PAGE COUNT – MAX 30 PAGES

B.6 ETHICS ISSUES

This should be done in conjunction with the information provided in Guide for Applicants, Marie Curie Actions (Ethics) and for **all** proposals the following table must be completed.

ETHICS ISSUES TABLE

	Research on Human Embryo/ Foetus	YES	Page
*	Does the proposed research involve human Embryos?		
*	Does the proposed research involve human Foetal Tissues/ Cells?		
*	Does the proposed research involve human Embryonic Stem Cells (hESCs)?		
*	Does the proposed research on human Embryonic Stem Cells involve cells in culture?		
*	Does the proposed research on Human Embryonic Stem Cells involve the derivation of cells from Embryos?		
	I CONFIRM THAT NONE OF THE ABOVE ISSUES APPLY TO MY PROPOSAL	X	

	Research on Humans	YES	Page
*	Does the proposed research involve children?		
*	Does the proposed research involve patients?		
*	Does the proposed research involve persons not able to give consent?		
*	Does the proposed research involve adult healthy volunteers?		
	Does the proposed research involve Human genetic material?		
	Does the proposed research involve Human biological samples?		
	Does the proposed research involve Human data collection?		
	I CONFIRM THAT NONE OF THE ABOVE ISSUES APPLY TO MY PROPOSAL	X	

	Privacy	YES	Page
	Does the proposed research involve processing of genetic information or personal data (e.g. health, sexual lifestyle, ethnicity, political opinion, religious or philosophical conviction)?		
	Does the proposed research involve tracking the location or observation of people? I CONFIRM THAT NONE OF THE ABOVE ISSUES APPLY TO MY PROPOSAL	X	

	Research on Animals	YES	Page
	Does the proposed research involve research on animals?		
	Are those animals transgenic small laboratory animals?		
	Are those animals transgenic farm animals?		
*	Are those animals non-human primates?		
	Are those animals cloned farm animals? I CONFIRM THAT NONE OF THE ABOVE ISSUES APPLY TO MY PROPOSAL	X	
	Research Involving ICP Countries	**YES**	**Page**
	Is the proposed research (or parts of it) going to take place in the one or more of the ICP countries?		

	Is any material used in the research (e.g. personal data, animal and /or human tissues samples, genetic material, live animal, etc) a) collected in any of the ICP countries?		
	b) Exported to any other country (including ICPC and EU Member States)?		
	I CONFIRM THAT NONE OF THE ABOVE ISSUES APPLY TO MY PROPOSAL	x	

	Dual Use	YES	Page
	Research having direct military use		
	Research having the potential for terrorist abuse I CONFIRM THAT NONE OF THE ABOVE ISSUES APPLY TO MY PROPOSAL	X	

B.7 TABLE - CAPACITIES OF THE HOST

(1 table per partner – maximum half a page per table)

Partner 1 – UniPI	
General description	The Enrico Fermi department of Physics in Pisa is classified to be in the first 100 in the world. It has ~ 90 faculty members. The University and Scuola Normale Superiore (SNS) find a common structure in the INFN for HEP experiments. Pisa had a leading participation to into many particle physics experiments: CDF (Fermilab), Aleph (LEP), CMS and Atlas (LHC) for collider physics. The Tracker Inner Barrel (TIB) was designed/produced in Italy and integrated in the large Pisa infrastructures. The Atlas group is small but had an important role in the tile calorimeter construction and has now a leading role in the FTK project. The Heavy Flavour experiments have been strongly represented both in the K (Epsi) and B (Babar) sectors; the neutrino sector by the Chooz and Nomad collaborations, the rare decay experiments by the MEG and the N64 experiments, the gravitational wave physics by the VIRGO laboratory. A large activity is present for astroparticle physics (Glast, AMS, Cream, Magic, Antares and Nemo).
Staff Expertise	Professors:. M. Dell'Orso, G. Punzi; Researchers: C. Roda, P. Giannetti, S. Donati; all physicists with large experience in Hadron Collider Physics (CDF, Atlas), in particular trigger and online/offline tracking (SVT at CDF and FTK in Atlas, data analysis). Engineer M. Piendibene: large experience in CDF trigger & AM system development and test.
Key facilities and infrastructure	HEP activity is strongly supported by (a) a strong theoretical team, (b) large laboratory space for all different activities (c) high-level infrastructures for electronics service (designing and production/test of boards), mechanics service (designing, developing, integrating detectors and large structures), high-technology (clean-rooms for silicon detectors with all necessary machines), computing (GRID facilities).
Previous involvement in Research Programmes	FP6-2005-Mobility-6 Proposal N° 039099- POT – european funds Fast Tracker - funds from INFN National Scientific Committee (NSC) V, 1999-2001 CDF Silicon Vertex Tracker Upgrade – INFN NSC I funds 2003-2004 CDF Level-2 Calorimeter trigger Upgrade – INFN NSC I funds 2006-2007
Current Involvement in Research Programmes	Fast Tracker Prototype Development for 2013 TDR submission: INFN NSC I funds
Publications	"**Observation of B0s - anti-B0s Oscillations**". By CDF Collaboration, Phys. Rev. Lett. 97, 242003, 2006; A. Annovi et al., "**A VLSI Processor for Fast Track Finding Based on Content Addressable Memories**". IEEE Transaction on Nuclear Science, vol. 53; p. 2428, 2006 A.Bhatti et al. "**The CDF level 2 calorimetric trigger upgrade**". IEEE Transaction on Nuclear Science, Volume 56, Issue 3, pp 1685-1689, 2009

Partner 2 – CAEN	
General description	CAEN is one of the most important spin-offs of the Italian Nuclear Physics Research Institute, founded in Viareggio (Lucca) in 1979. CAEN (www.caen.it) designs and manufactures sophisticated electronic equipment for nuclear physics research and is today one of the world's leading companies in the field.
Staff Expertise	• High voltage and low voltage power supply systems and boards (standalone, VME and NIM versions), front-end electronics for data acquisition and analysis (Silicon Photomultiplier read out - SiPM, digitizers, Digital Pulse Processing, triggering & timing, preamplifiers, etc.) • R&D, Production and Test facilities for electronic systems; Project Management division
Key facilities and infrastructure	R&D, Production and Test facilities for electronic systems; Project Management division
Previous involvement in Research Programmes	• Participation to many Regional, National and European research projects. • More than 30 years of experience in electronics for high energy physics.
Current Involvement in Research Programmes	• **MODES_SNM - MOdular DEtection System for Special Nuclear Materials** Funded by European Commission under the 7th Framework Programme (FP7) / Cooperation - Theme: SECURITY • **DICASTERO** – Funded by Regione Toscana
Publications	[1] D.Cester, D. Fabris, M. Lunardon, S. Moretto, G. Nebbia, S. Pesente, L. Stevanato, G. Viesti, F. Neri, S. Petrucci, S. Selmi, C. Tintori: An Integrated mobile system for port security, ANIMMA Conference 2011, Ghent, 5.06. [2] D. Cester, G. Nebbia, L. Stevanato, G Viesti, F. Neri, S. Petrucci, S. Selmi, C. Tintori, P. Peerani, A. Tomanin: Special nuclear material detection with a mobile multi-detector system, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Volume 663, Issue 1, 21 January 2012, Pages 55-63. [3] G Viesti, D. Cester, G. Nebbia, L. Stevanato, F. Neri, S. Petrucci, S. Selmi, C. Tintori, P. Peerani, A. Tomanin: Special Nuclear Material detection studies with the SMANDRA mobile system, IX LASNPA Conference, Quito 2011.

Partner 3 – CERN	
General description	CERN, the European Organization for Nuclear Research, is one of the world's largest centres for scientific research. The instruments used at CERN are particle accelerators and detectors. The TE-MPE-EM section (Technical Engineering Department – Machine Protection and Electrical integrity - Electronics Modules) provides CERN-wide support for the layout, production and assembly of printed circuit boards, flexible circuits, hybrids and fine pitch detectors
Staff Expertise	Fabio Formenti (TE-MPE-EM Section Leader), Betty Magnin (Design Office Leader), William Billereau (Supervisor Cadence design team)
Key facilities and infrastructure	TE-MPE-EM has know-how, workshop equipments and informatic tools for: (a) Layout of printed circuit boards and ceramic hybrids, fine-pitch detectors and fan-outs for detectors, front-panels and small mechanics, user-specific crates, schematic and library symbols for Cadence, Altium and PCAD, management of component purchasing and orders, archival of standardised production files in EDMS; (b) Production of ceramic hybrids, low-mass circuits with Aluminium conductive layers (CERN developed process), fine-pitch detectors and readout circuits (MPGD as GEM, THGEM, Resistive Micromegas, FGLD: CERN developed processes), multilayer PCB (FR4, kapton, flex-rigid), thermal management devices based on pyrolitic carbon structures; (c) Assembly of surface mount components (including BGA), wire bonding and die attach (in cooperation with PH-DT2), assembly of through-hole components, wiring of electrical cables, assembly of crates and small mechanics, cabling of crates. On the other side the facility for commissioning will be ATLAS itself, in particular the trigger system - selecting 100 interesting events per second out of 1000 million others; (b) the data acquisition system - channelling the data from the detectors to storage; (c) the computing system - analysing 1000 Million events recorded per year.
Previous involvement in Research Programmes	CERN research programs BE - Design office : ~ 600 jobs/year, 150 clients, organised fabrication of over 800 designs PMT – Production: ~ 800 "standard" jobs/year, ~ 100 jobs in cleanroom /year
Current Involvement in Research	CERN research programs for physics experiments and for accelerator domains

Programmes	
Publications	"A four-gap glass-RPC time-of-flight array with 90 ps time resolution" Formenti, F. et al., IEEE Transactions on Nuclear Science, Volume: 48 , Issue: 5, Page(s): 1658 - 1663 "Arc Suppression Snubbers on Energy Extraction Switchgear in the LHC Superconducting Main Circuits of the LHC Collider: Impact on the Vital Quench Protection Systems", Formenti, F. et al., Proceedings 18th IEEE International Pulsed Power Conference - June 19-23 2011, Chicago (USA), 2P-4 "Upgrade of the quench protection systems for the superconducting circuits of the LHC machine at CERN: from concept and desing to the first operational experience", F. Formenti et al., Proceedings 1st International Particle Accelerator Conference, Kyoto, Japan, 23 - 28 May 2010, pp.MOPD013

Partner 4 – AUTH	
General description	AUTH is the largest Greek University: more than 100k students. The Physics Department has ~ 90 faculty members. The Division of Nuclear and Particle Physics has a long standing involvement in particle physics experiments at CERN; it is currently in ATLAS with an important contribution on the experiment construction (over 10% of the precision tracking muon chambers), and on the physics exploitation (conveners of the B-physics group, leading the analysis of ZZ production, background for the Higgs->ZZ->4l channel). The Division of Electronics has extensive experience in FPGA programming, algorithm implementation on hardware, testing and firmware development.
Staff Expertise	Faculty in ATLAS: Prof. C. Petridou (the ATLAS group leader in AUTH) , Assis. Prof D. Sampsonidis, Lecturer K. Kordas; Students: O. Sidiropoulou. Facutly in Div. Electronics: Assoc. Prof. S. Nikolaidis, Adjoint Lecturer V. Konstantakos; Students: C-L. Sotiropoulou, L. Voudouris (for curricula see Sections B.3 and B.4)
Key facilities and infrastructure	Lab with ATLAS muon scintillators, muon chamber prototypes and electronics (NIM modules) and PCs to Trigger and do the Data Acquisition. Setup for testing new prototypes (micromegas modules) with cosmics & radioactive sources. Tier 3 cluster in the ATLAS computing grid. Avnet Spartan-6 LX150T Developers Kit with camera extension and daughter card, 2 Xilinx Virtex 5 XUPV-LX110T evaluation platforms, 12 Xilinx Spartan-3E Starter Boards and 5 XC9572 CPLDs, Altera Nios II Development Kit (Stratix II Edition). Full access to the Xilinx tools through Europractice. Cadence Suite through Europractice, Measurement and analysis instruments for low-frequency analogue electronic circuits (signal generators, analog and digital oscilloscopes of various types, voltmeters, power supply circuits etc). Specialized equipment (low-frequency spectrum analyzer, distortion measurement instrument, phase difference measurements, frequency meters, characteristic curve plotters for transistor and integrated circuit characterization).
Previous involvement in Research Programmes	ATLAS group has attracted ~2 Meuros in funding during the last 16 years. Two of those programs: i) The **CROSSGRID** project (IST March 2002-February 2005) ii) **ARTEMIS** – Marie Curie RTN (Oct. 2006 – Sept. 2010). "Architectures and Methodologies for Dynamic Reconfigurable Logic" (**AMDREL**) IST-2001-34379, EU funded; "Methodology Development for Optimum Design for Special Purpose Processors", PENED '03, Nationally Funded
Current Involvement in Research Programmes	**DIBOSON,** (2011-2015). Nationally Funded by ESPA (Thalis action). **AIDA,** (2011-2015), FP7-INFRASTRUCTURES-2010-1 . **"Microelectronic elements for Lab-On-Chip Devices for Molecular Analysis targeting Genetic and Environmental Applications",** Nationally Funded by ESPA (Corallia) **"Jordan Europe Wide Enhanced research Links in ICT"**, Coordination and Support action, No 266507
Publications	[1] "**Measurement of the ZZ Production Cross Section and Limits on Anomalous Neutral Triple Gauge Couplings in Proton-Proton Collisions at √s=7 TeV with the ATLAS Detector"**, ATLAS Collaboration, Phys. Rev. Lett. 108, 041804 (2012). [2] "**Performance of the final Event Builder for the ATLAS Experiment"**, M. L. Ferrer, H. P. Beck, S. Gadomski, K. Kordas et al. IEEE Trans. Nucl. Sci. 55, 176 (2008). [3] **"The ARISE Approach for Extending Embedded Processors with Arbitrary Hardware Accelerators,"** N. Vassiliadis, G. Theodoridis, and **S. Nikolaidis**, IEEE Transactions on Very Large Scale Integration Systems, Vol. 17, No 2, pp.221-233, Feb. 2009.

Partner 5 - PRISMA	
General description	PRISMA is an R&D performing SME with main mission to promote and support the right and effective use of new technologies in Electronics and ICT. PRISMA's top priority is the development, through applied R&D, of innovative Products and Services, to be competitive in the international market.
Staff Expertise	**Andreas Sakellariou,** Electrical and Electronic Engineer. Experienced in PCB design & RF simulation. Participated in 5 R&D EU and national projects. **Dimitrios Dimas**, Physicist with MSc in Radioelectrician and currently PhD candidate in Optical Sensors. He has experience in software development and in wireless networks. Participated in 7 R&D projects. **Panagiotis Kalaitzidis**, Electrical and Computer Engineer. Production Manager. Highly experienced in prototypes production and performing tests (functional, Isolation&Continuity and burn in tests). **Konstantina Mermikli**, Electrical and Computer Engineer. R&D projects manager. Strong experience in embedded software development and testing tools design and in testing boards and integrated systems. **Serafeim Katsikas**, Electrical and Electronic Engineer. Highly experienced in electronics design and software development, with over than 14 years of complex research activities. **Petros Soukoulias**, MSc in Computer Science, Highly experienced in application software development and in electronics manufacturing. Participation in 11 Research projects and strong experience in multinational project management.
Key facilities and infrastructure	• Tools and means for PCB design, RF simulations and embedded programming. • Electronic lab with oscilloscopes, Spectrum analyzers, Frequency generators etc. • A PCBs assembly line, using SMT and TH technologies. • Equipment for electrical & optical tests, functional tests and burn in tests.
Previous involvement in Research Programmes	• **Tyre Pressure Monitoring System** (CRAFT 5513, 1999-2000) : Cooperative research for the development of a Tyre Pressure Monitoring System. • **Solar Air Conditioning System using Very Low Cost Variable Plastic Ejector** (CRAF-1999-70921, 2002-4). Cooperative research & development of a solar air-conditioning system. • **Dynamite** (FP6 2005-2009): Development of an advanced e-maintenance solution incorporating mobile monitoring technology, sensors, wireless telemetry, intelligent local history in smart tags.
Current Involvement in Research Programmes	• **Hypersol** (FP7 2010-2013) Environmentally Sustainable Manufacturing of Ultra-Functional Miniaturized Consumer Electronics Using Hyper-Fine Solder Powders • **IceHeart** (FP7 2010-2013) Highly integrated ultra-low-power SoC solution for unobtrusive and energy-efficient wireless cardiac monitoring • **MicroStir** (FP7 2010-2013) High reliability electronics assembly and encapsulation for extreme service environments using micro friction stir welding • **Nanocom** (2011-2014) New approach for future generation of smart systems by introducing nano-structured materials capacitive MEMS to improve reliability by one order of magnitude • **WelCOM** (2010-2014) Condition Monitoring (CM) via a flexible toolset of solutions based on Wireless Sensor Network platforms
Publications	• Autonomous and wireless enabled liquid level sensors based on a Multi-segment polymer fiber optic. • Wireless-Enabled Photonic Sensor for Liquid Level & Distributed Flood Monitoring, Comadem 2011 • Predictive Maintenance in Maritime Vessels, Comadem 2011

Partner 6 - LPNHE	
General description	The LPNHE (Laboratoire de Physique Nucléaire et des Hautes Energies) of Paris is a Mixed Unit of Research (UMR7585) of CNRS, Université Pierre et Marie Curie (UPMC) and Université Paris Diderot. It is at Campus Jussieu, in the 5th arrondissement of Paris. It is composed of 12 research and 5 support groups (administration and services) for a total of about 200 persons. Among the different Collaborations there are many involving High-Energy Physics: ATLAS at CERN, CDF and D0 at Fermilab, BaBar at SLAC, T2K in Japan; the participation in cosmic rays studies is represented by contributions to HESS in Namibia and AUGER in Argentina; cosmology by SNLS and LSST.
Staff Expertise	**Giovanni Calderini**, former Pisa University and Scuola Normale student, is Director of Research (DR2) at LPNHE, working in the Atlas Group. He was the Project Leader of the BaBar Silicon Vertex Tracker (SVT) and has been Run Coordinator of PEP-II at SLAC. He has extensive experience of Collider Physics and Silicon Trackers in High Energy Physics and is the responsible of the activities for the ATLAS upgrade at LPNHE. **Francesco Crescioli**
Key facilities and infrastructure	The LPNHE is equipped with a few ISO7 and ISO8 clean rooms, presently used for the ATLAS and LSST R&D. Among other instruments, they are equipped with a Karl Suss PA200 Semiautomatic Probe station with a temperature controlled chuck (-60+200C); semiconductor parameter analyzers; laser systems coupled to XY stages for charge collection efficiency characterization of Silicon sensors; all the other necessary instrumentation for R&D on silicon sensors. The Electronics Division of the laboratory is providing all the necessary support in chip design (recently a 65nm CMOS process) and peripheral electronics development (FPGA programming, card design and assembly), Cadence for board design and Xilinx, Altera CADs. Tier3 Computing facility. A large mechanical workshop equipped with numerical controlled machines is providing the necessary infrastructure for detector building.
Previous involvement in Research Programmes	BaBar Silicon Vertex Tracker – INFN Comm I - funds 1998-2001 ATLAS Silicon Vertex Tracker Upgrade – INFN Comm I - funds 2008-2009 PRIN Giorgi – Development of Silicon Trackers - funds 2004-2006
Current Involvement in Research Programmes	HIGGSNET – ANR Blanc 2010 AIDA – Advanced European Infrastructures for Detectors and Accelerators 2011-2014 ATLAS Insertable B-Layer and Pixel Upgrade – IN2P3 funds
Publications	[1] Simulations of planar pixel sensors for the ATLAS high luminosity upgrade, G.Calderini, M. Benoit, N. Dinu, A. Lounis, G. Marchiori, 2011. 5 pp. Published in **Nucl.Instrum.Meth. A636 (2011) S37-S41** [2] The SuperB silicon vertex tracker, G.Rizzo, C.Avanzini, G.Batignani, S. Bettarini, F. Bosi, G. Calderini, M. Ceccanti, R. Cenci, A. Cervelli, F. Crescioli *et al* (2010) 3pp Published in **Nucl.Instrum.Meth. A617 (2010) 585-587** [3] Study of the radiation hardness of irradiated AToM front-end chips of the BaBar silicon vertex tracker. S. Bettarini, M. Bondioli, L. Bosisio, G. Calderini, S. Dittongo, F. Forti, M.A. Giorgi (2006) 5 pp. Published in **IEEE Trans.Nucl.Sci. 53 (2006) 584**

B.8 GANTT CHART Organised per fellow and reflecting Secondments, Recruitments, Management and Dissemination / Outreach Activity

Ref in A forms	[Sending institution] [Country] [Commercial sector Y/N]	[Hosting/ Recruiting institution] [Country] [Commercial sector Y/N]	Active in WP	Type	Fellow starts at project month	Total PM	Year 1												Year 2												Year 3												Year 4											
							1	2	3	4	5	6	7	8	9	10	11	12	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3	4	5	6	7	8	9	10	11	12
							1 St art	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	46	43	44	45	46	47	48
1	[UniPi], [Italy], [N]	[Prisma], [Greece], [Y]	1	M-ER B>10	7	3							1	2																3																							
2	[UniPi], [Italy], [N]	[Prisma], [Greece], [Y]	1	M-ER B>10	8	3								1	2																										3											
3	[AUTH], [Greece] [N]	[Prisma], [Greece], [Y]	1	ER A<10	5	6					1	2				3	4								5	6																											
4	[AUTH], [Greece] [N]	[Prisma], [Greece], [Y]	1	ER A<10	11	2											1	2																																			
5	[Prisma], [Greece] [Y]	[AUTH], [Greece], [N]	1	ER A<10	8,22, 31	6								1	2													1	2							1	2														
6	[Prisma], [Greece] [Y]	[CERN], [Switzerl.], [N]	3	ESR A	18	2																		1	2																											
7	[CAEN], [Italy] [Y]	[CERN], [Switzerl.], [N]	3	M-ER B>10	8	6								1	2										3	4													5	6												
8	[UniPi], [Italy], [N]	[CAEN], [Italy], [Y]	2	M-ER B>10	10	16										1	2	3	4	5	6	7	8	9	10	11								12	13	14	15	16														
9	[AUTH], [Greece], [N]	[CAEN], [Italy], [Y]	2	M-ER B>10	4,15	7				1	2										1	2																						3	4	3								
10	[AUTH], [Greece], [N]	[CAEN], [Italy], [Y]	2	ER A>10	38	1																																					1										
11	[AUTH], [Greece], [N]	CAEN], [Italy], [Y]	2	ESR A	15	6															1	2	3																				4	5	6								
12	[AUTH], [Greece], [N]	CAEN], [Italy], [Y]	2	ER A<10	4	4				1	2											3	4																														
13	[AUTH], [Greece], [N]	CAEN], [Italy], [Y]	2	M-ER A<10	4	5				1	2										3	4	5																														
14	[LPNHE], [France], [N]	CAEN], [Italy], [Y]	2	M-ER B<10	8	8								1	2			3	4							5	6																	7	8									
15	[LPNHE], [France], [N]	CAEN], [Italy], [Y]	2	M-ER B>10	8	4								1											2											3												4					

FTK

Ref in A forms	[Sending institution] [Country] [Commercial sector Y/N]	[Hosting/ Recruiting institution] [Country] [Commercial sector Y/N]	Active in WP	Type	Fellow starts at project month	Total PM	Year 1												Year 2												Year 3												Year 4											
							1	2	3	4	5	6	7	8	9	10	11	12	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3	4	5	6	7	8	9	10	11	12
							1 Start	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	46	43	44	45	46	47	48
16	[Prisma], [Greece] [Y]	[UniPi], [Italy], [N]	1	ER A<10	5, 26	6					1	2																			1	2		3	4																		
17	[Prisma], [Greece] [Y]	[UniPi], [Italy], [N]	1	ESR, A	3,14	4			1	2									1	2																																		
RECRUITMENTS																																																					
1		[AUTH], [Greece], [N]	1,3,4	ER A<10	13	24													1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24											
2		[CERN], [Switzerl.], [N]	1,3	ER A<10	32	12																				1	2	3	4	5	6	7	8	9	10	11	12															
3		[LPNHE], [France], [N]	2,6	ER A>10	13	12													1	2	3	4	5	6	7	8	9	10	11	12																									
4		[UniPi], [Italy], [N]	8	ER A<10	10	20										1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20																	
5		[UniPi], [Italy], [N]	8	ER A<10	26	18																									1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18					
OUTREACH								UNIPI						CAEN						AUTH						CERN				LPNHE						PRISMA						Not decided yet										
1	IAPP OPEN DAY																																																				
2	WORKSHOP DAY																																																			
3	SUMMER SCHOOL WEEK																																																			
4	FTK WORKSHOP																																																			
5	TRAININGS																																																			

In the “column Type” we define the type of contract:
A = contract with full social security coverage
B =status equivalent to a fixed amount fellowship.
M = married
<10 = less than 10 years of research experience
>10 = more than 10 years of research experience

ENDPAGE

PEOPLE
MARIE CURIE ACTIONS

Marie Curie Industry-Academia Partnerships and Pathways (IAPP)
Call: FP7-PEOPLE-2012-IAPP

PART B

"PROPOSAL ACRONYM"