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Low latency, fast inference neural networks on FPGA: the ATLAS L0 Muon Barrel Trigger use case

In many research and industrial settings, achieving fast, low-latency algorithmic responses is essential. To meet the demands of the upgraded LHC and future High Energy Physics (HEP) detectors, quick and powerful triggers are necessary. In recent years, Machine Learning (ML) algorithms have been widely applied to such tasks, and more recently, hardware solutions for ML applications based on Field Programmable Gate Arrays (FPGAs) have proven to be effective, offering reduced latency and power consumption compared to GPUs not only in HEP field.

This work presents an implementation of fast neural networks on FPGAs for the Level-0 Muon Barrel trigger system in the ATLAS experiment.

The implementation of the different architectures has been performed using the HLS4ML library, which in combination with Vitis HLS package translate a Tensorflow model into VHDL code. We made synthesis-level estimations for the latency and the occupancy in terms of FPGA components usage of different CNN architectures.

Moreover, the performance and scalability of the proposed algorithm on multi-FPGA systems could be tested on the AMD Alveo cluster available at the INFN-Naples site. This cluster will also be used for Atlas High Level Trigger studies.

This work is within the use case “Ultra-fast algorithms running on FPGA” within the WP2 frame.

INFN OpenAccess Repository link

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