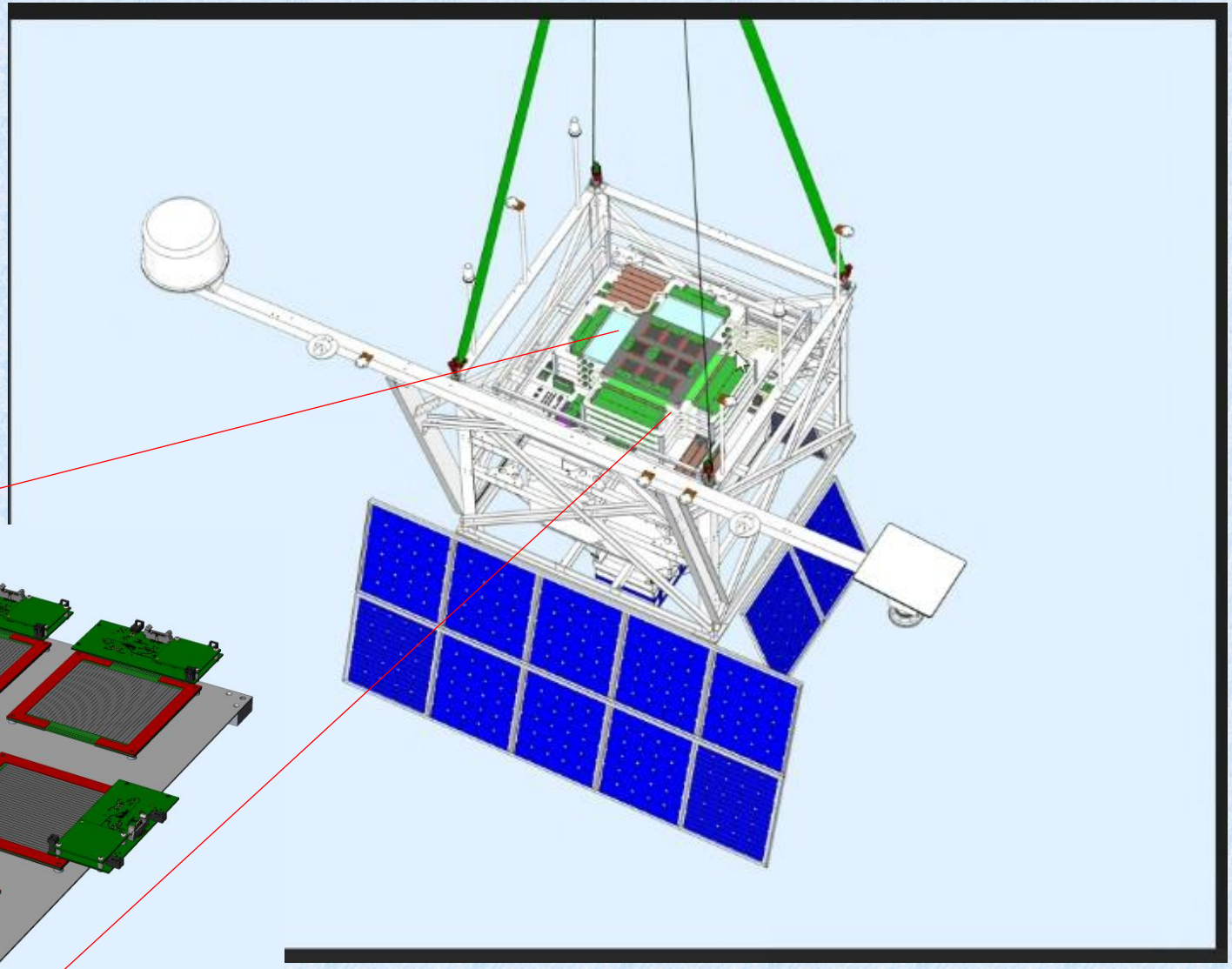
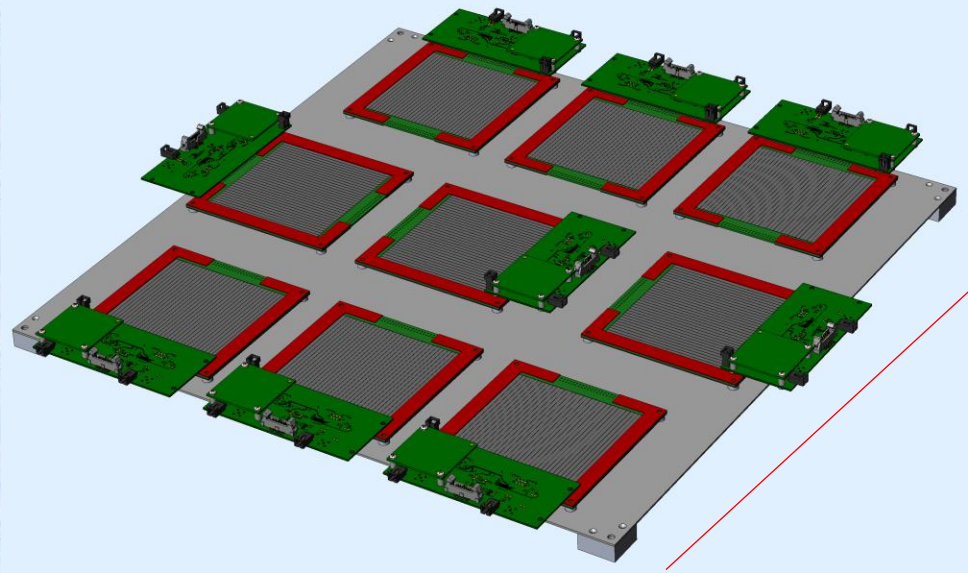
ADAPT Silicon Strip Detector System Status

John Krizmanic NASA/GSFC
Richard Bose WUSTL

Science/Technical Goals

1. **Measure flux of light thru heavy (^{2}He thru ^{42}Mo) cosmic rays.**
2. Prototype detector for APT.
3. Investigate measuring Compton-scattering gamma events.

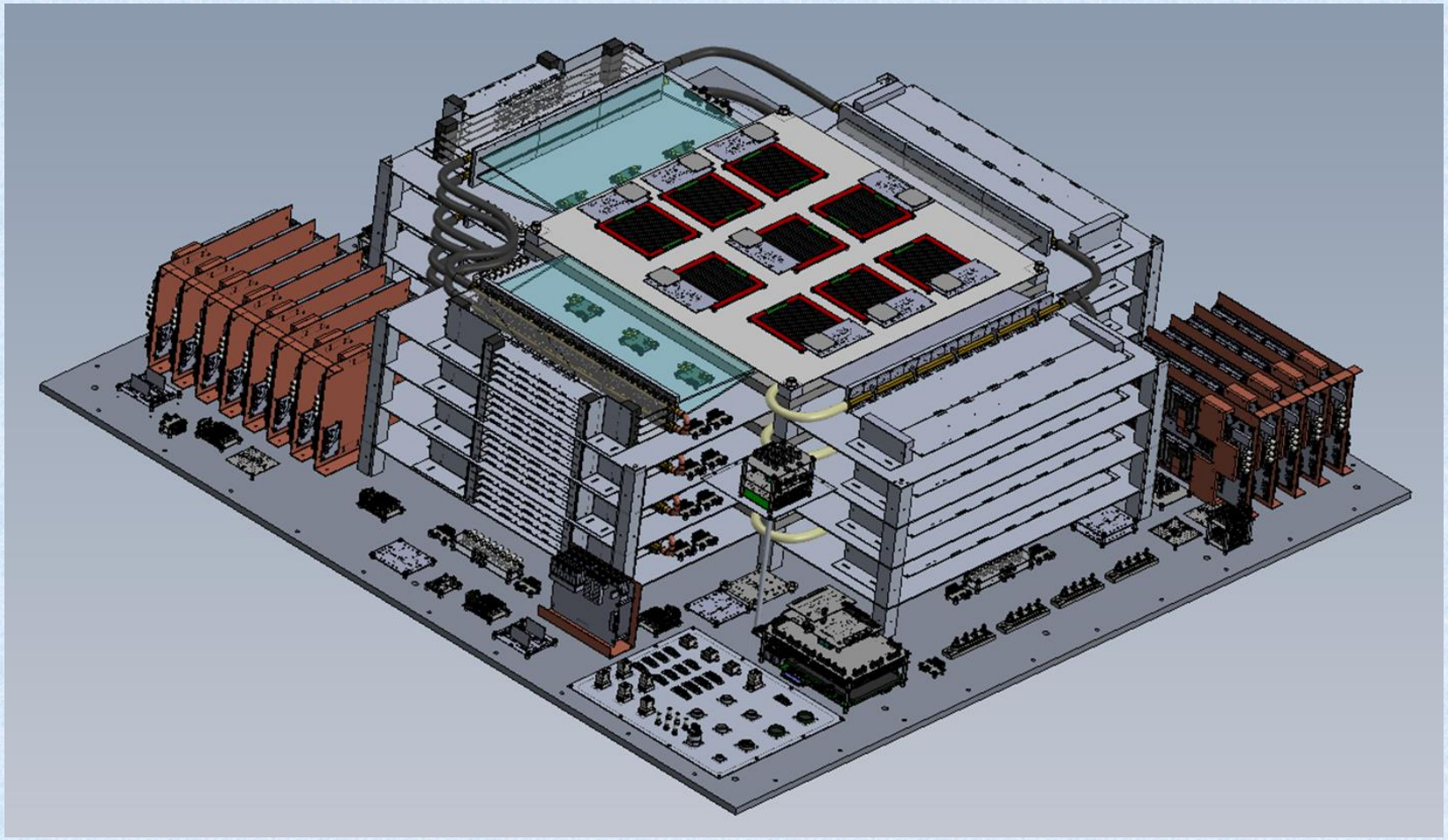




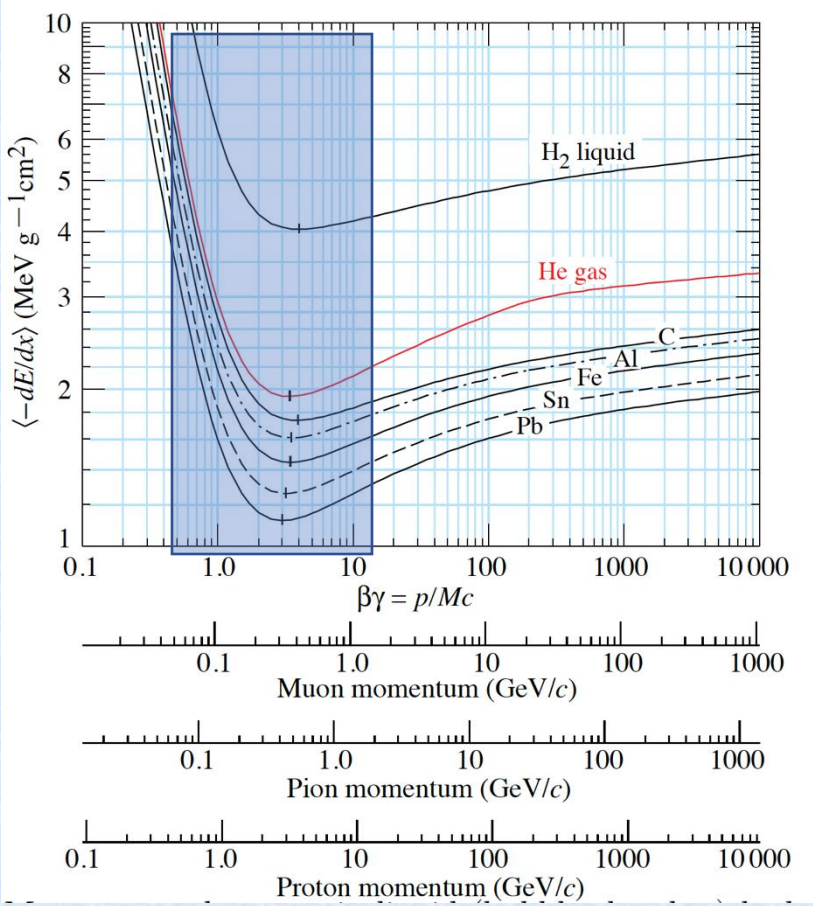
ADAPT Silicon Strip Detector Layout

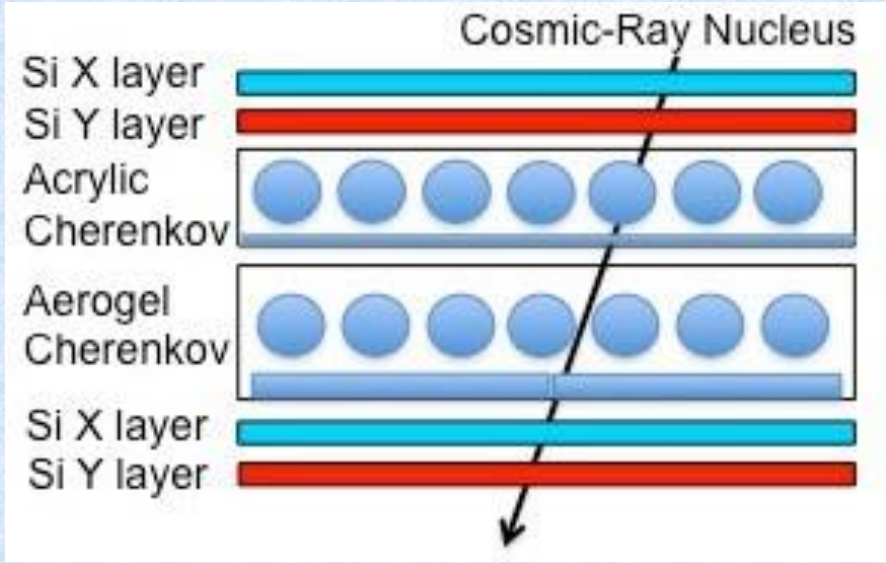
Purpose:

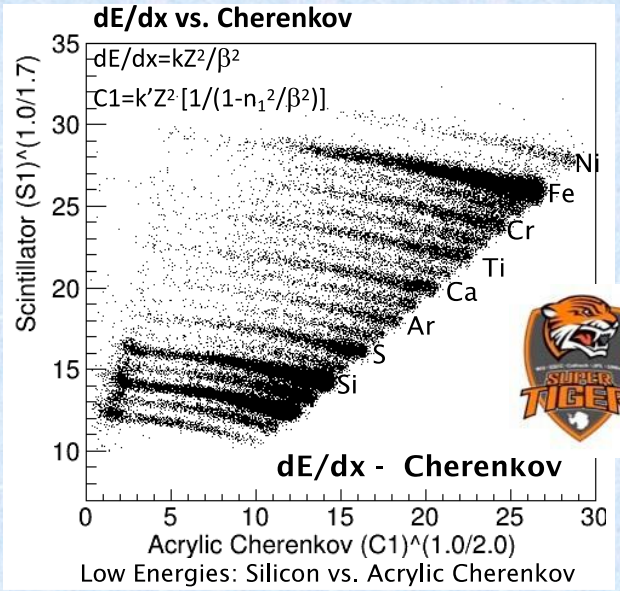
- ADAPT:
  1. Measure flux of light thru heavy (^{2}He thru ^{42}Mo) cosmic rays.
- ADT:
  1. Measure flux of ultra-heavy Galactic Cosmic Rays (UHGCRs) at least thru ^{82}Pb, potentially actinides (3 × 6 m^2 area -> GF ~ 40 m^2 sr (for $0 \leq \theta \rho 60$).
  2. Depending on ADAPT development, measure Compton-scattering gamma events, but would need double-sided SSDs or Pixel detectors.



SSD Principle of Operation in TIGERISS







How do we define minimal dE/dx range for ADAPT?

https://pdg.lbl.gov/ *32. Passage of particles through matter* **5**

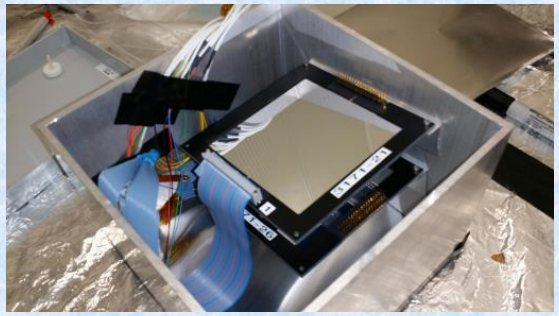
32.2.3. ***Stopping power at intermediate energies*** :

The mean rate of energy loss by moderately relativistic charged heavy particles, $M_1/\delta x$, is well-described by the "Bethe equation,"

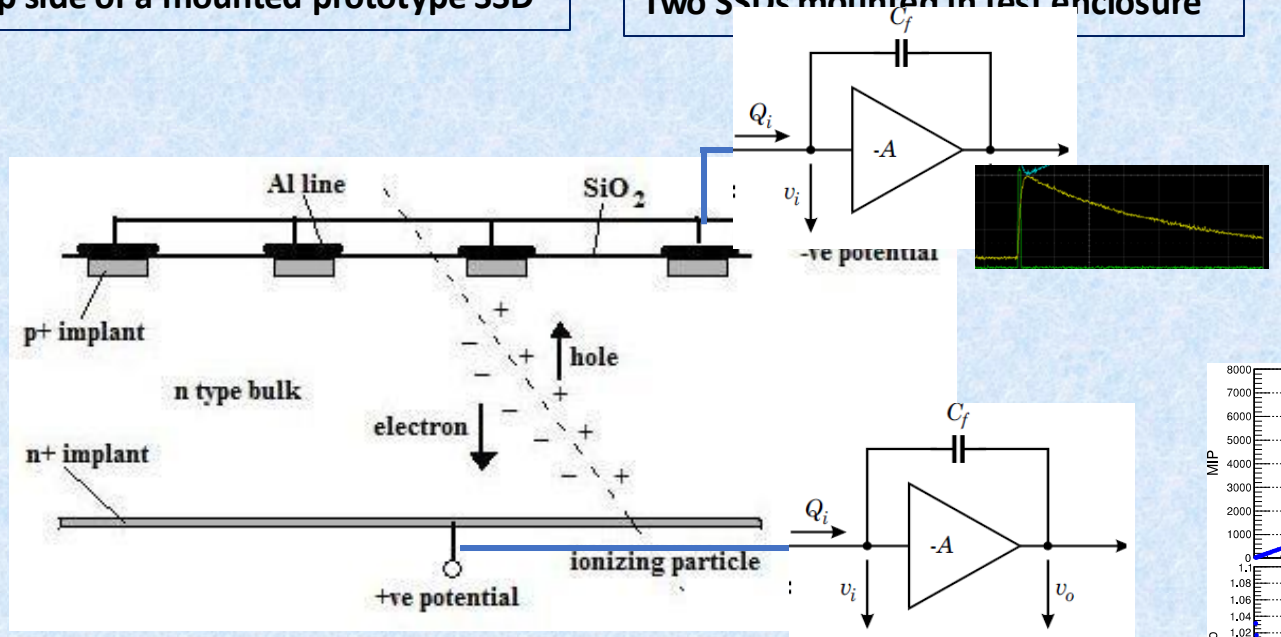
$$\left\langle -\frac{dE}{dx} \right\rangle = Kz^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 W_{\max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right] . \qquad (32.5)$$

SSD Principle of Operation for Charge Measurment

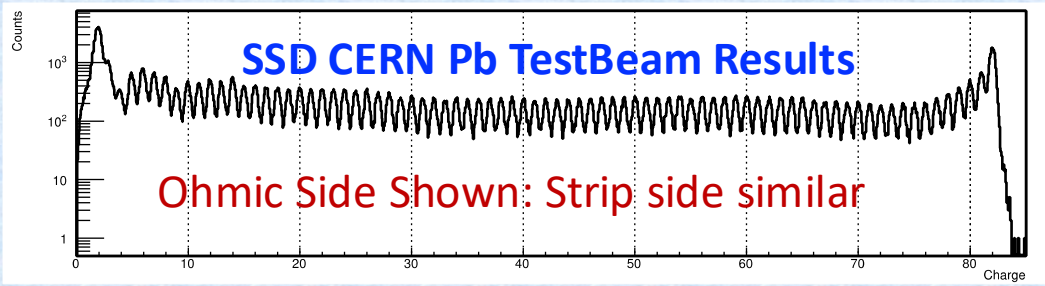
The strip side of a mounted prototype SSD



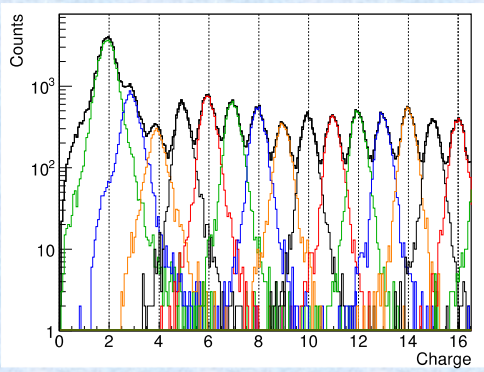
Two SSDs mounted in test enclosure



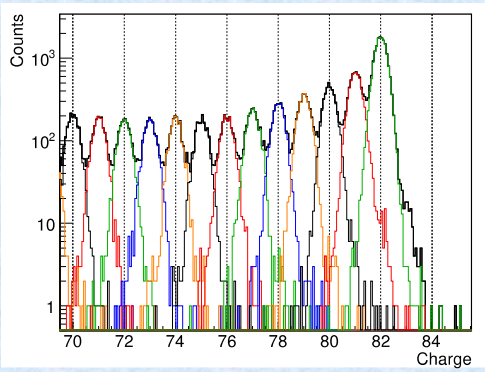
Source: Tata Institute of Fundamental Research



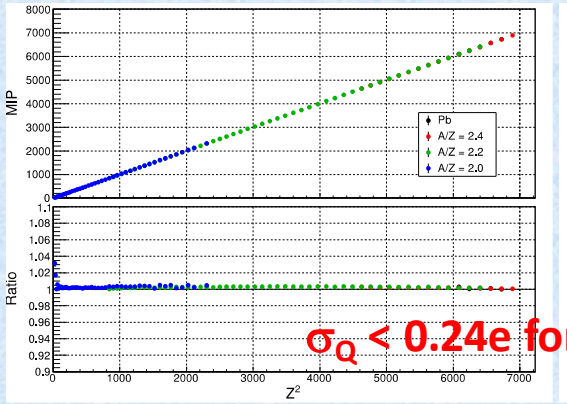
(a) $Z = 2 - 82$



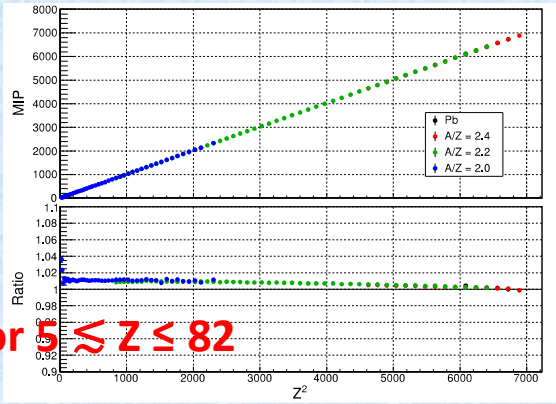
(b) $Z = 2 - 16$



(c) $Z = 70 - 82$



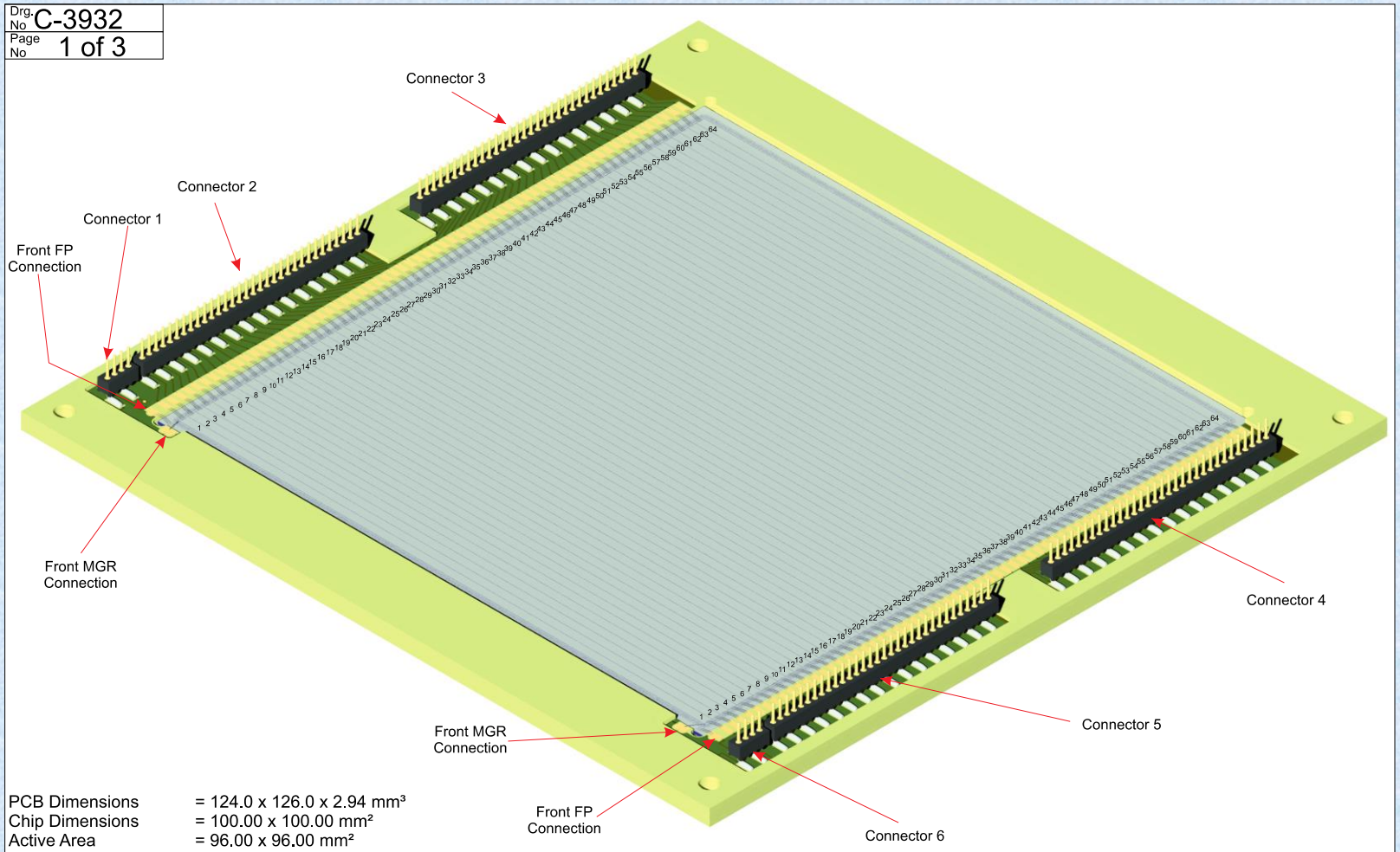
(a) Ohmic-side



(b) Strip-side

$\sigma_Q < 0.24e$ for $5 \lesssim Z \leq 82$

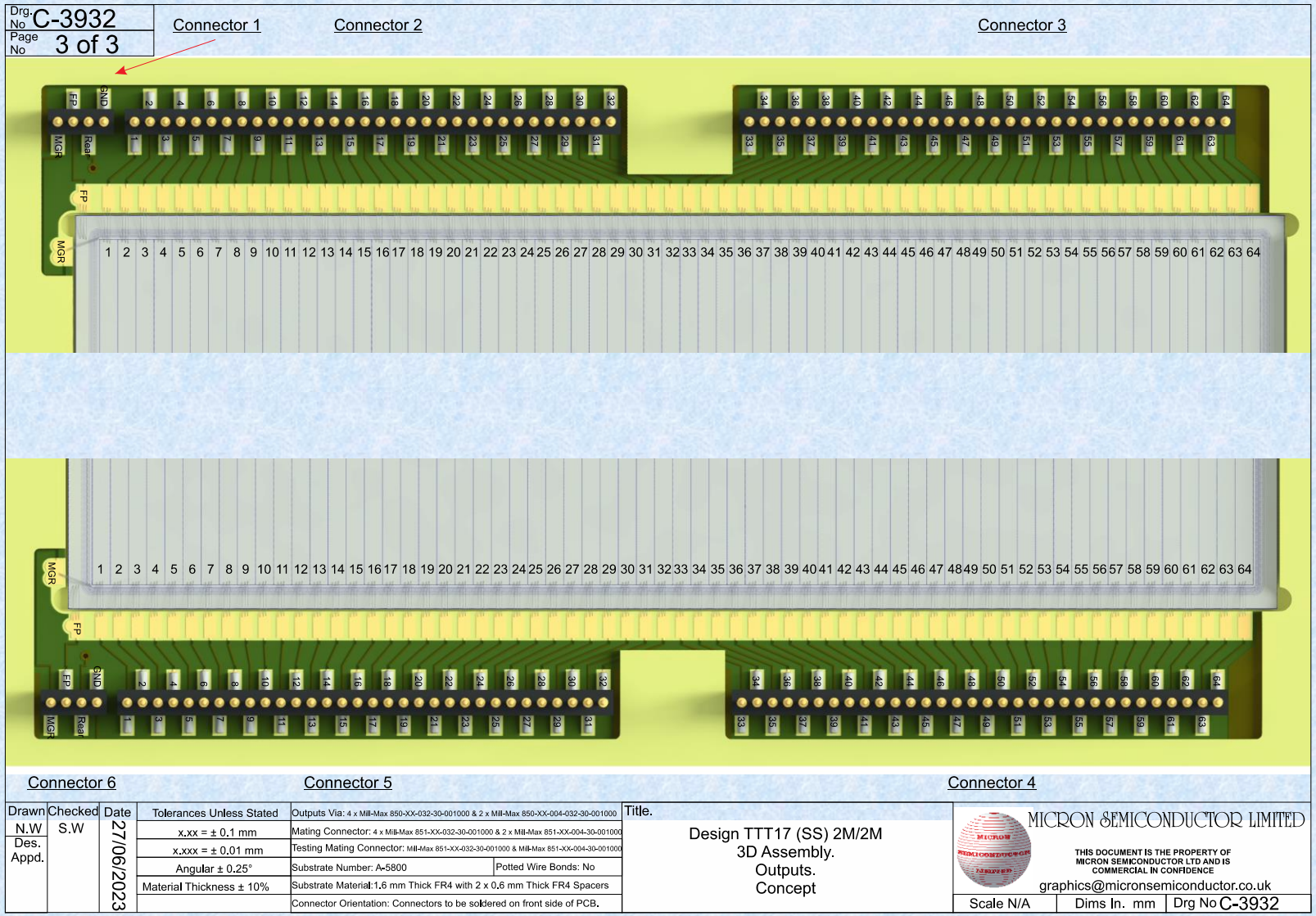
ADAPT Micron SSD Design (64 strips with 1.5 mm pitch)

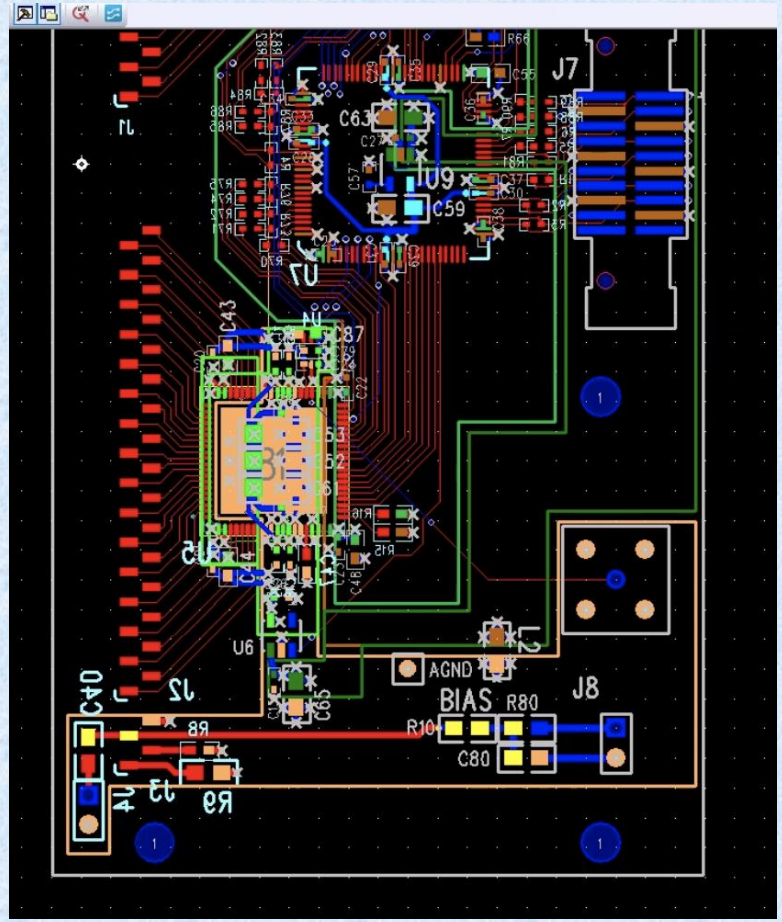


SSD Design:

- Single Sided, DC-coupled Strip Detector
- Size: 10 cm x 10 cm x 500 um
- Channels: 64
- Strip Pitch: 1.5 mm
- Active Area: 96 mm x 96 mm
- Each SSD mounted in custom PCB
- Twelve SSDs ordered

ADAPT Silicon Strip Detector Status

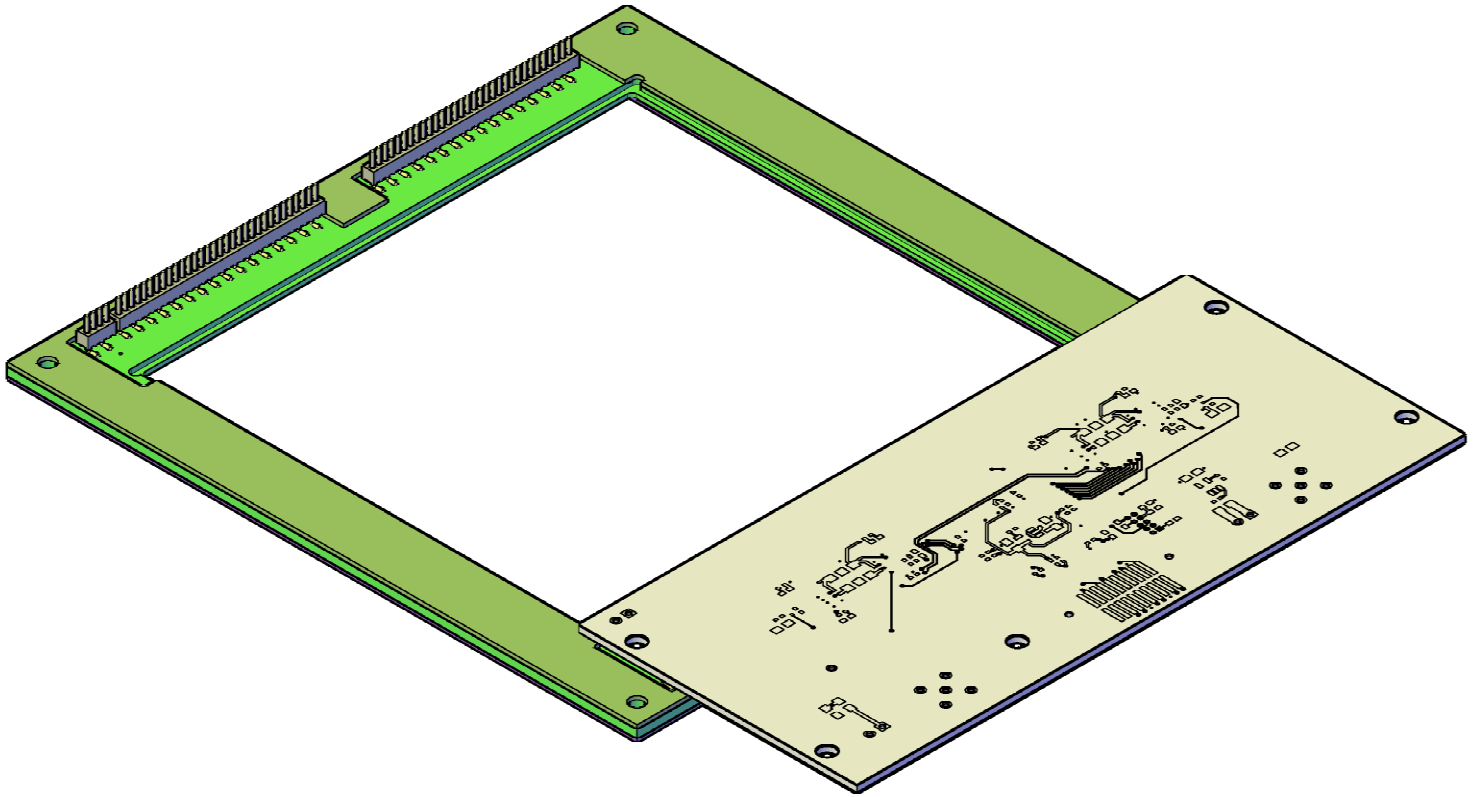




Bottom part of an NRL card

ADAPT Silicon Strip Detector Mounted to NRL Card

Drg. No.	A-5826
Page. No.	5 of 5



Drawn. N.W	Checked S.W	Date 13/09/2023	Tolerances Unless Stated	Material - Standard FR4 PCB material		Title.	TTT17 (SS) Version 2 PCB Design 3D View with FEE Board
Design Approved			x.xx ± 0.1mm	Plating - 1oz Cu plating with ENIG areas			
Customer.			x.xxx ± 0.01mm	Solder Resist Front - Green	Front Spacer - 0.6 mm FR4		
			Angular ± 0.25°	Solder Resist Rear - No	Rear Spacer - 0.6 mm FR4		
			Material Thickness ± 10%	Ledge - 1.0 mm Deep in Main PCB Layer			

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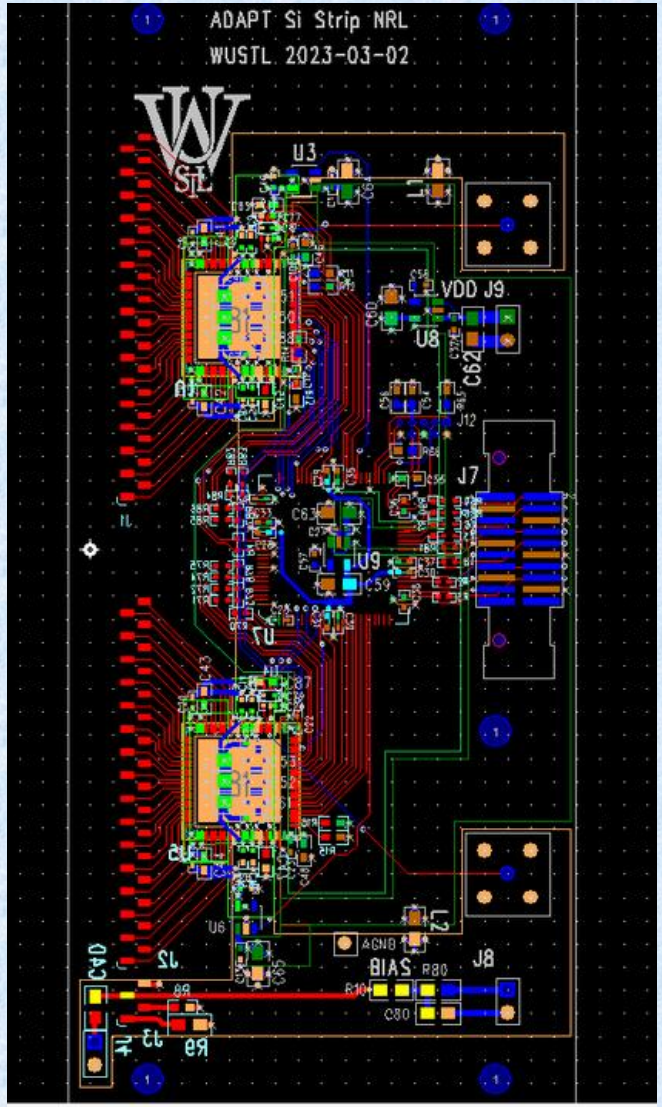
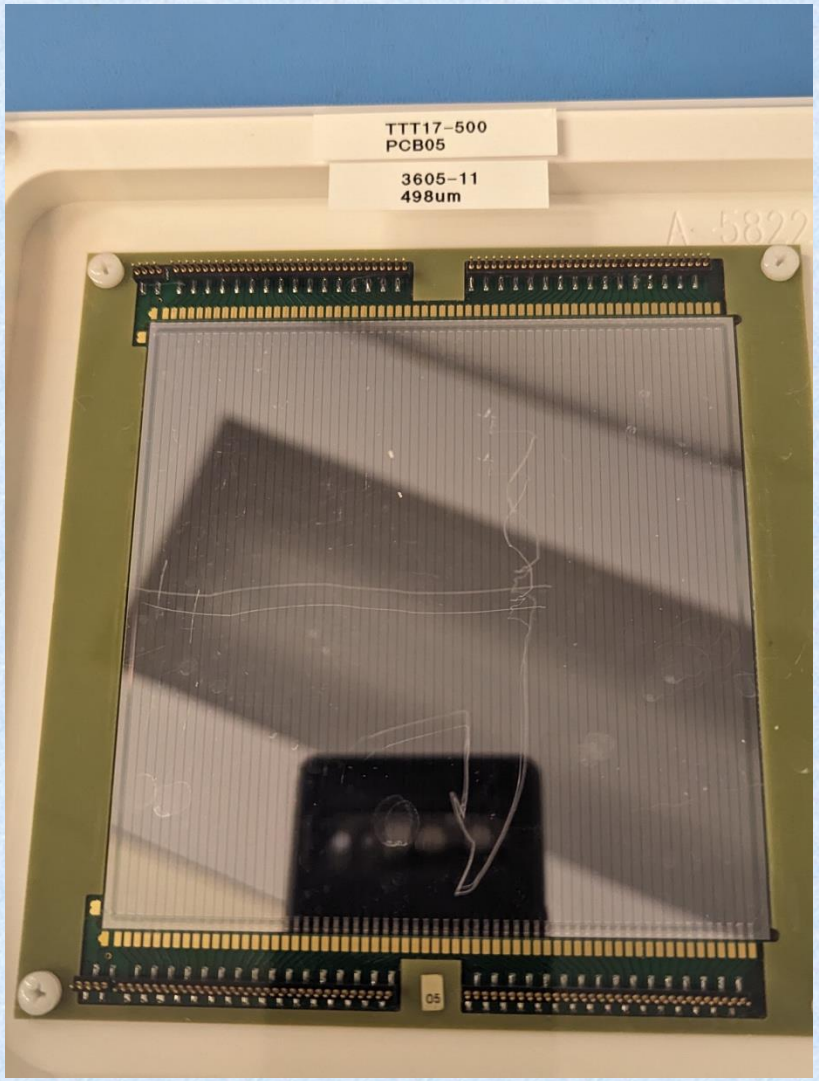
Scale. 1.25:1 | Dims In. mm | Drg. No. A-5826

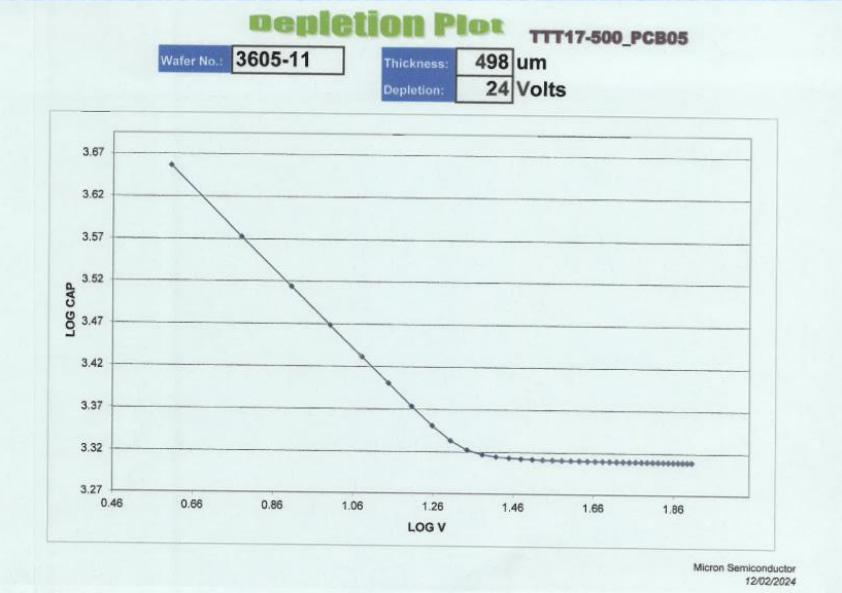


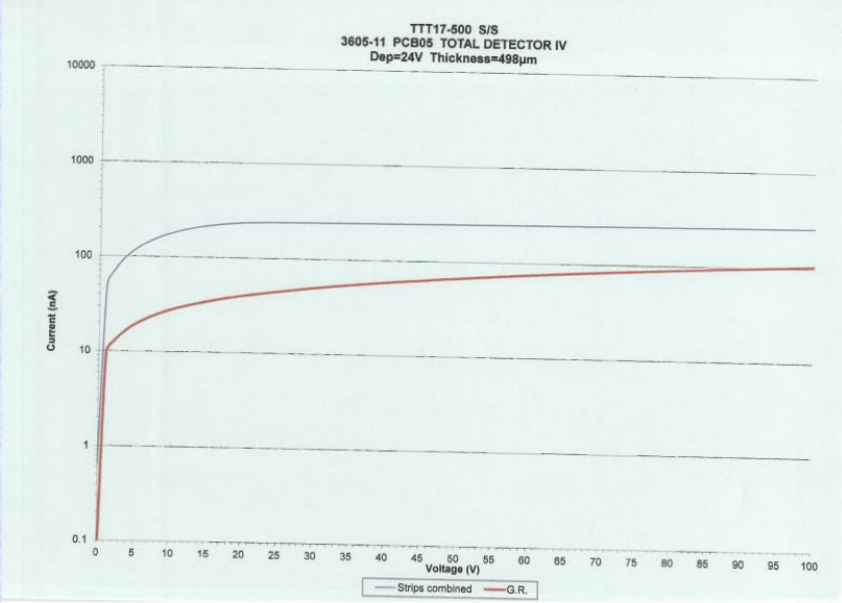
ADAPT SSD Inventory

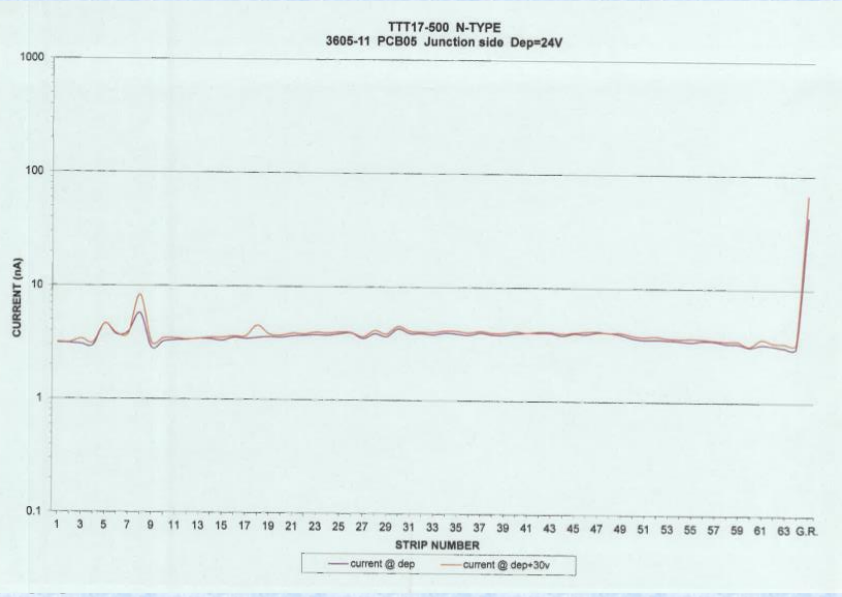
Device	PCB #	Thickness [um]	V_Dep [V]	IV Evaluation	Location	Comment
3605-07	18	505	23	Acceptable	WUSTL	I (Vdep+30V) ~20 nA Channel 34
3605-09	12	503	24	PASS	GSFC	I (Vdep+30V) < 10 nA all channels
3605-10	16	504	25	PASS	GSFC	
3605-11	5	498	24	PASS	WUSTL	
3605-14	1	500	23	Acceptable	GSFC	I (Vdep+30V) ~60 nA Channel 28
3645-03	33	520	15	PASS	GSFC	
3645-04	29	502	15	Acceptable	GSFC	I (Vdep+30V) ~ 50 nA Channel 39
3645-06	23	510	15	Acceptable	GSFC	I (Vdep+30V) ~25 nA Channel 40
3645-09	26	515	15	PASS	GSFC	
3645-10	24	511	15	PASS	GSFC	
3645-11	30	508	15	PASS	GSFC	
3645-12	28	499	15	Acceptable	GSFC	I (Vdep+30V) ~20 nA Channel 23
3645-02	34		15	PASS	Micron	
3648-16	35		15	PASS	Micron	
3648-17	36		15	PASS	Micron	
3648-18	37		15	PASS	Micron	
3648-22	40		16	PASS	Micron	

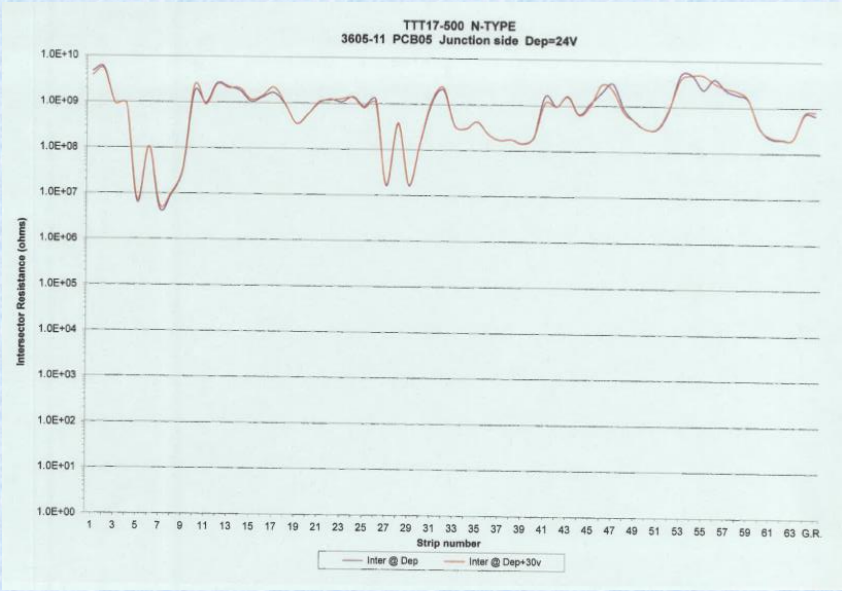


ADAPT SSD Micron Test Results: 3605-11 ACCEPTED

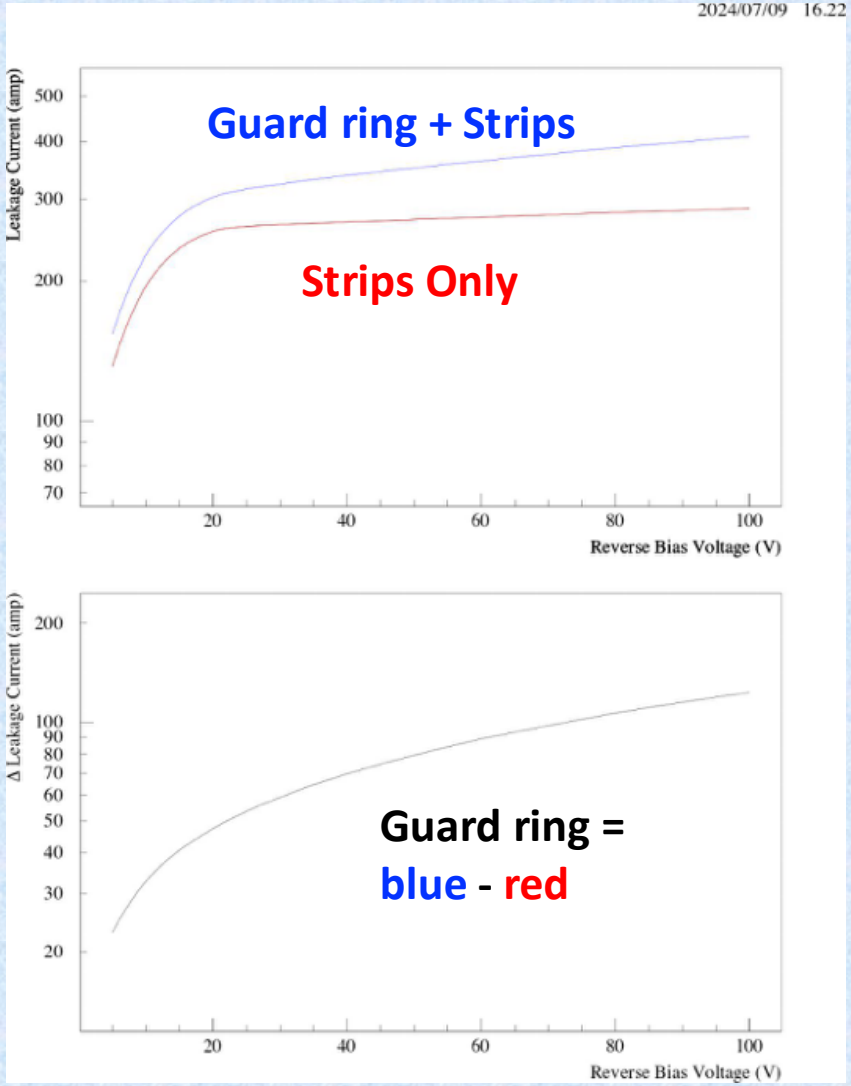




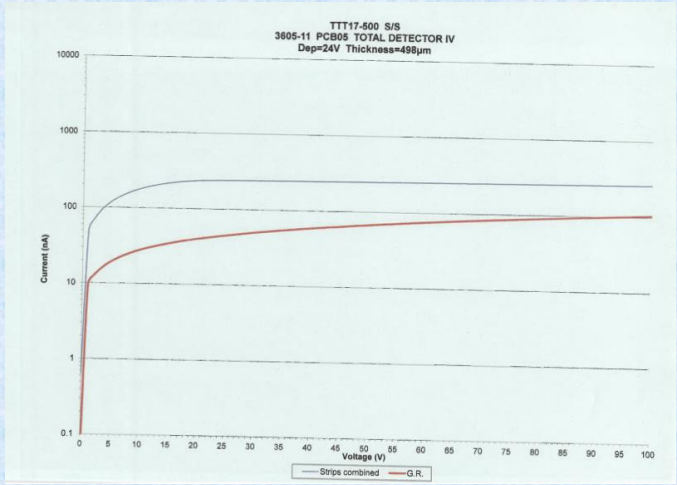


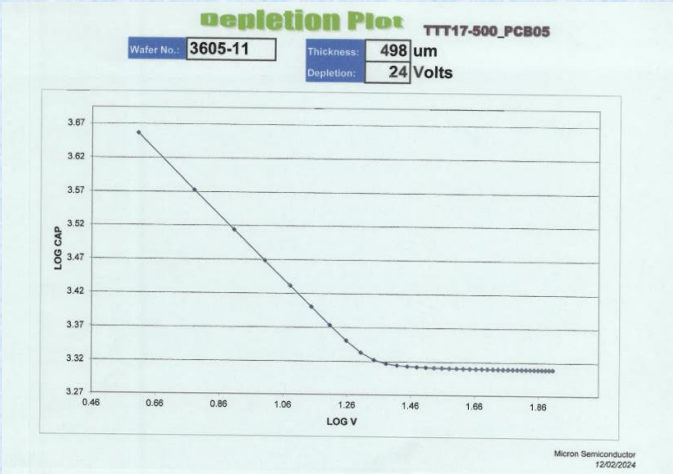


ADAPT SSD GSFC Testing 3605-11

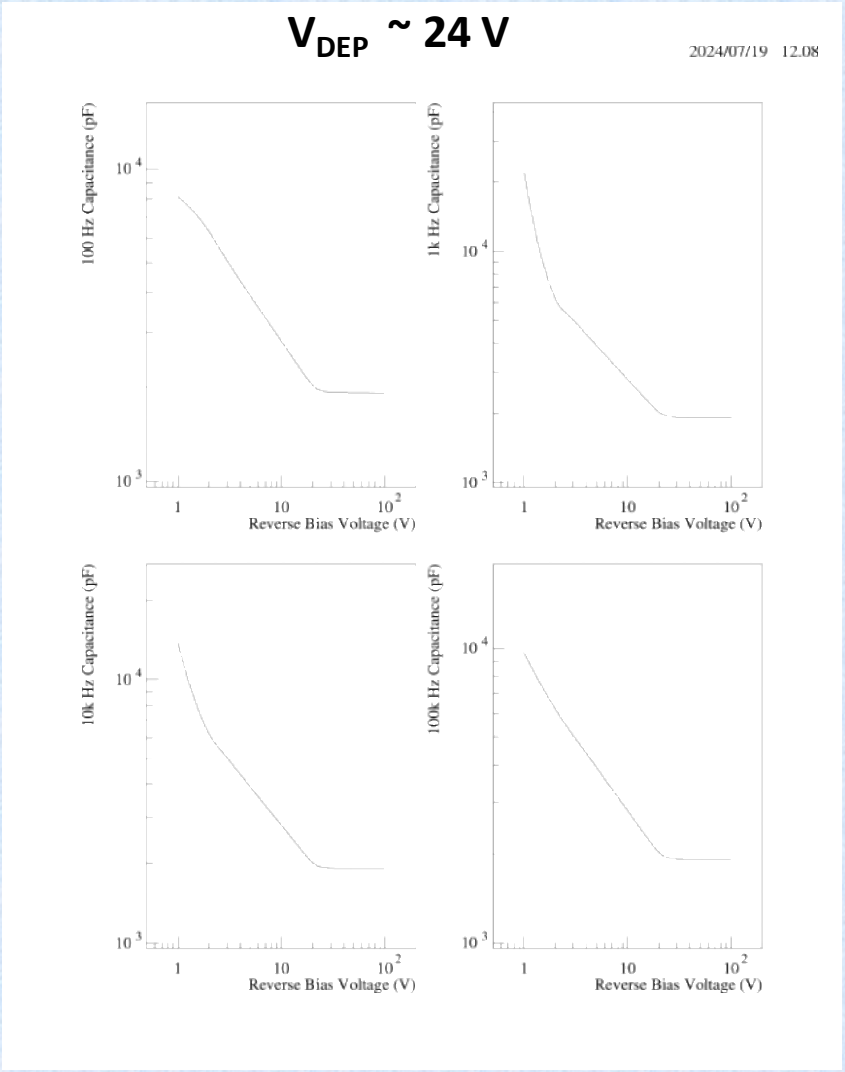


IV measured at GSFC



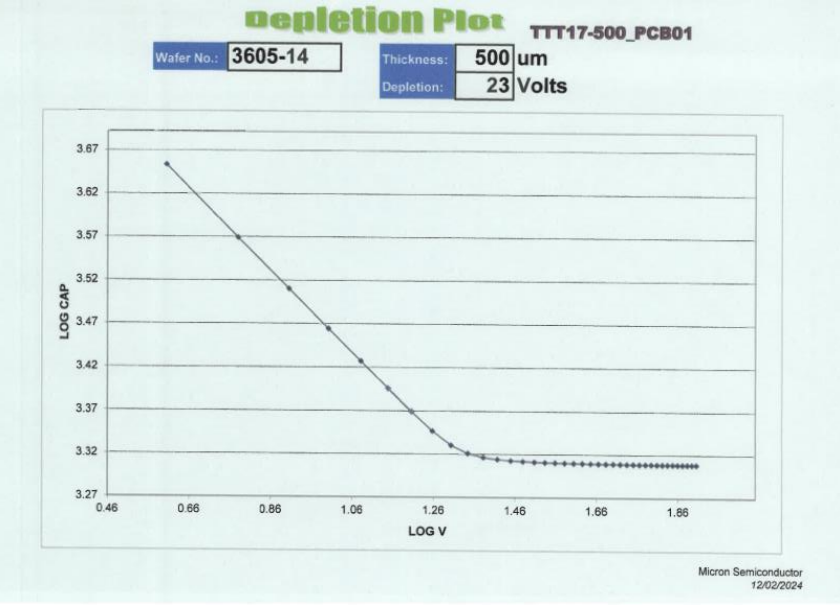


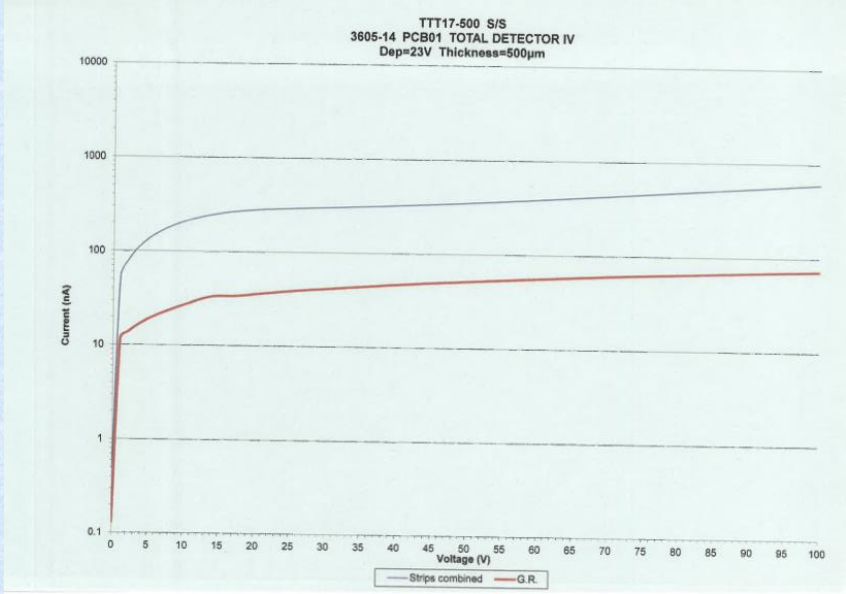
V_{DEP} ~ 24 V

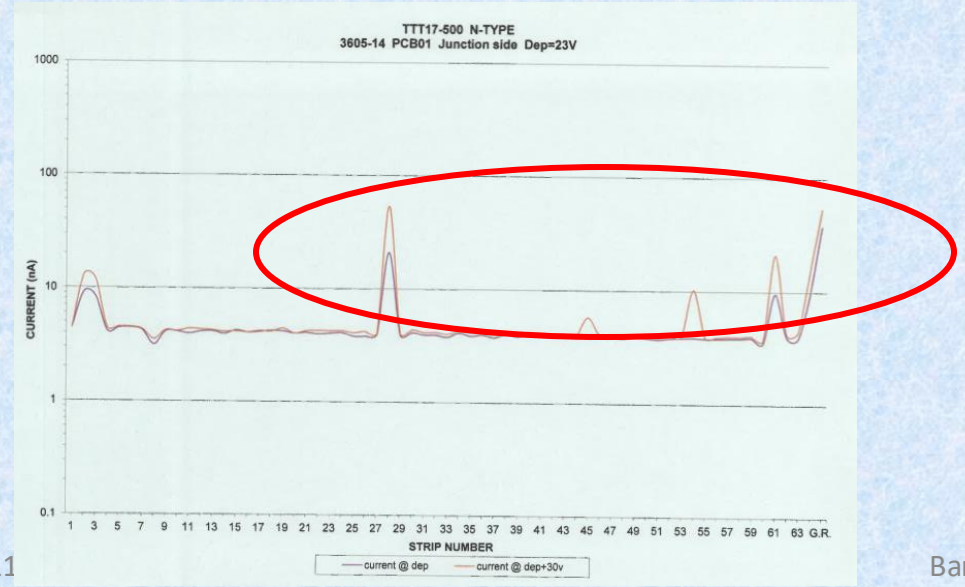


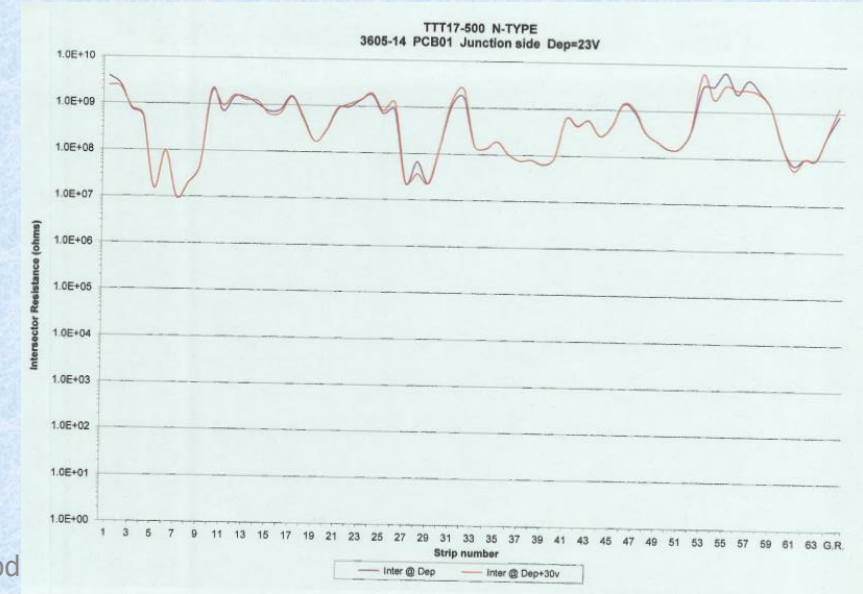
CV measured at GSFC

ADAPT SSD Micron Test Results: 3605-14 NOT ACCEPTED



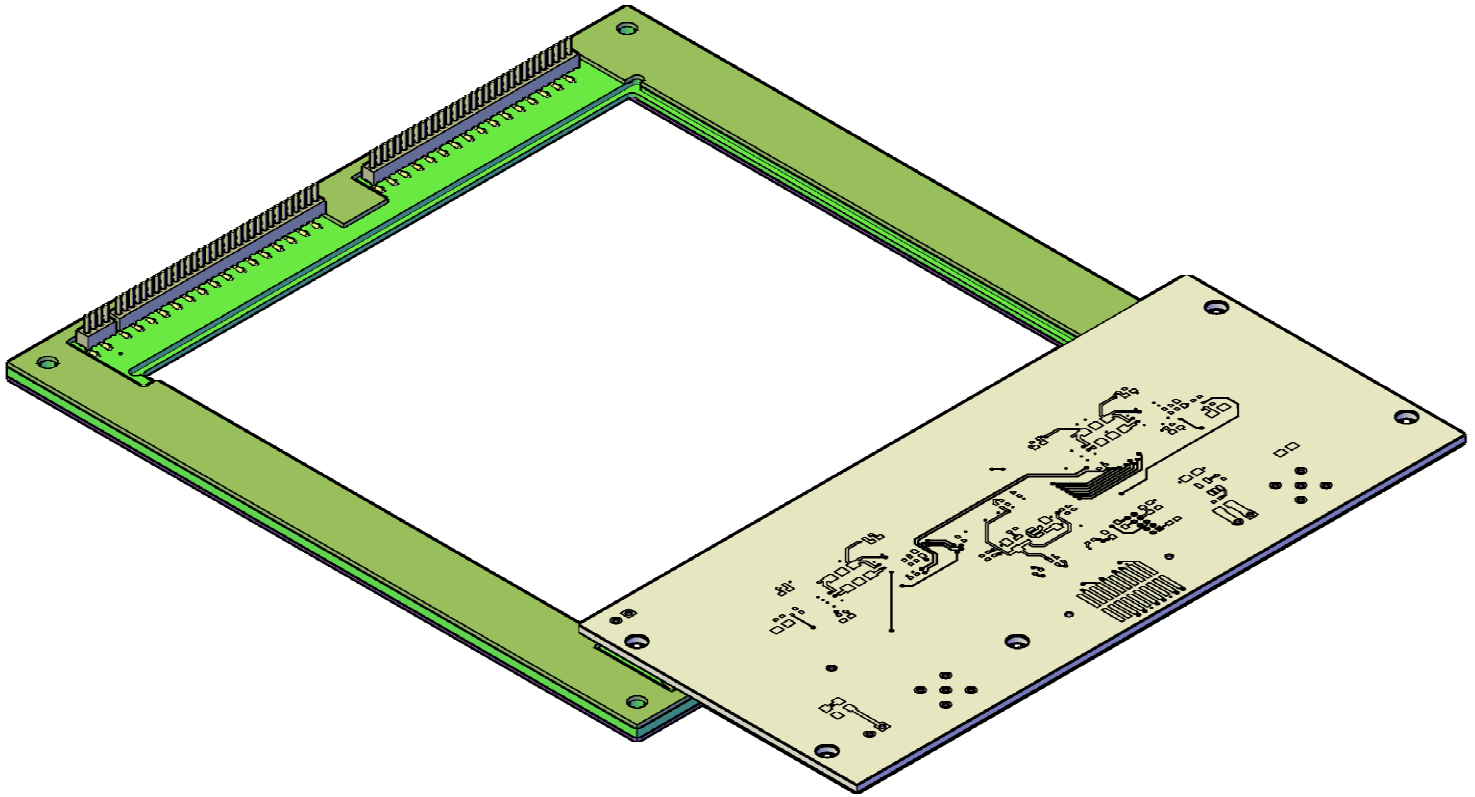






ADAPT Silicon Strip Detector Electronics Discussion

Drg. No.	A-5826
Page. No.	5 of 5



Drawn.	Checked	Date
N.W	S.W	13/09/2023
Design Approved		
Customer		

Tolerances Unless Stated	Material - Standard FR4 PCB material	
x.xx ± 0.1mm	Plating - 1oz Cu plating with ENIG areas	
x.xxx ± 0.01mm	Solder Resist Front - Green	Front Spacer - 0.6 mm FR4
Angular ± 0.25°	Solder Resist Rear - No	Rear Spacer - 0.6 mm FR4
Material Thickness ± 10%	Ledge - 1.0 mm Deep in Main PCB Layer	

Title. TTT17 (SS)
Version 2 PCB Design
3D View with FEE Board

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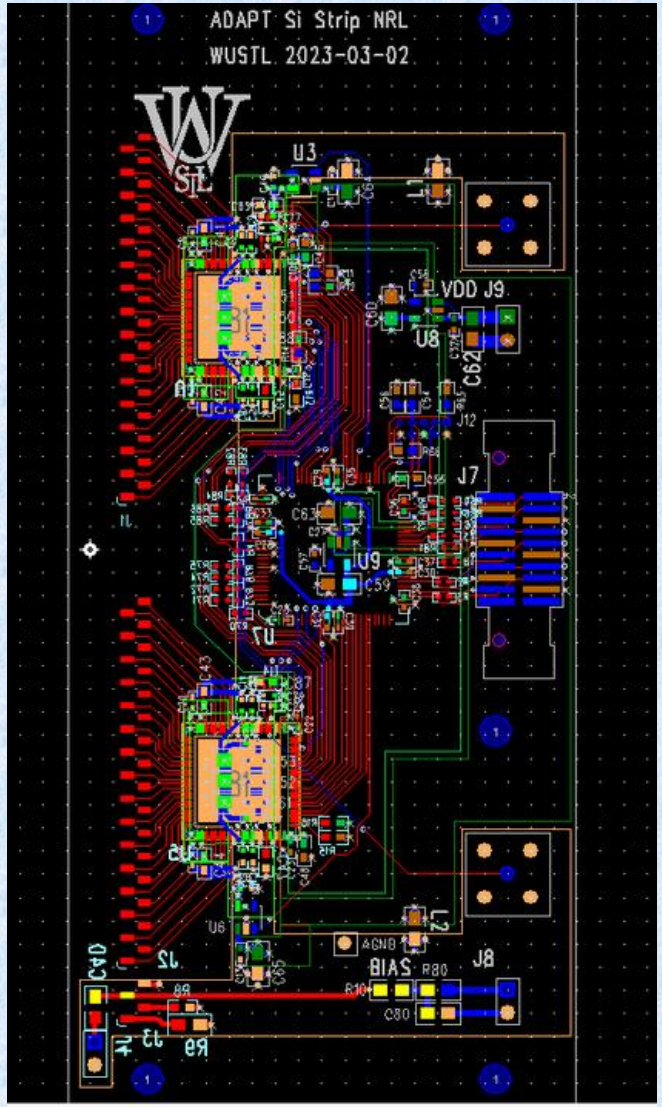
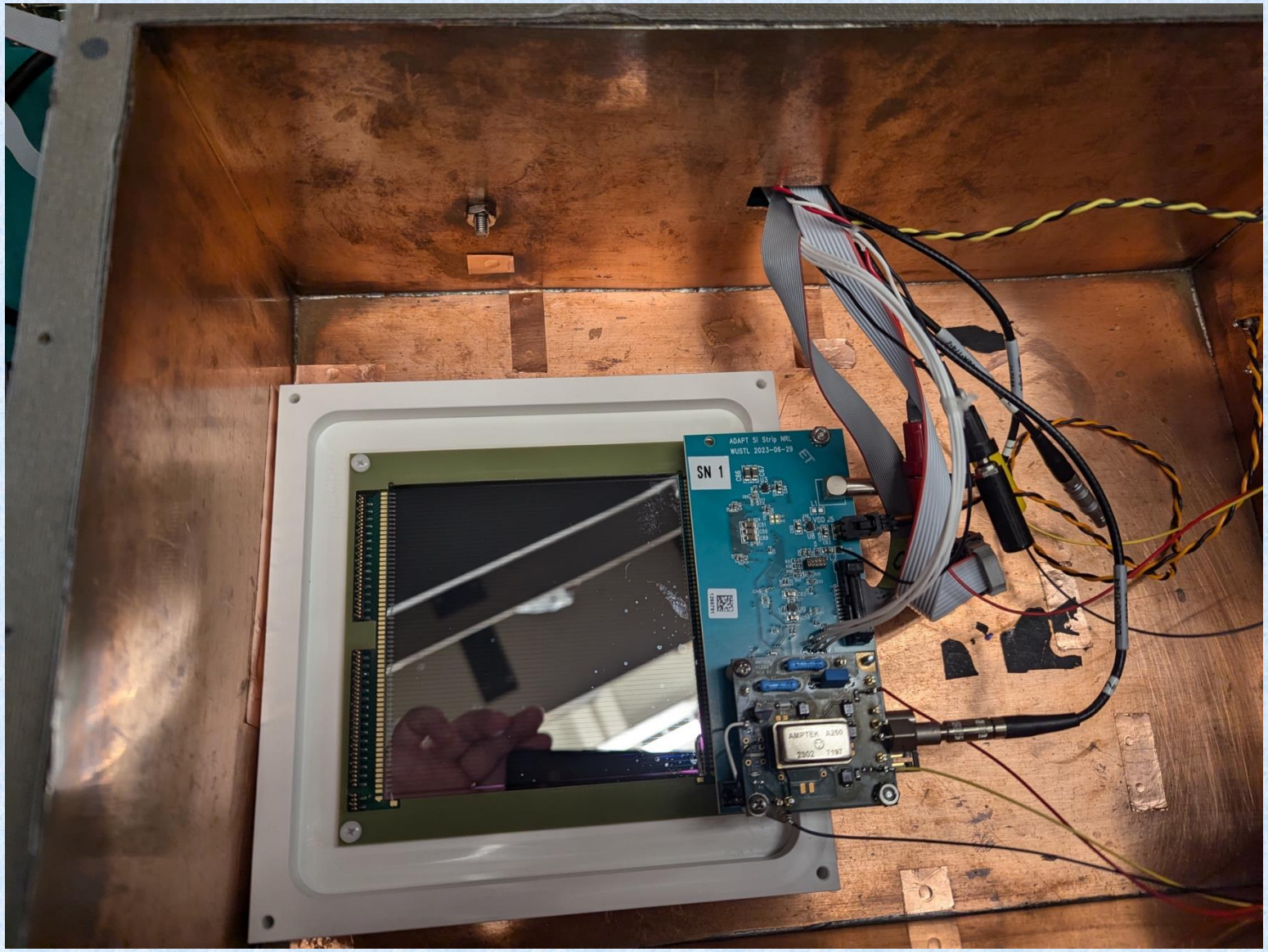
Scale. 1.25:1 | Dims In. mm | Drg. No. A-5826



Initial Testing Results: Aug 2024 at WUSTL: A250 had oscillation problem



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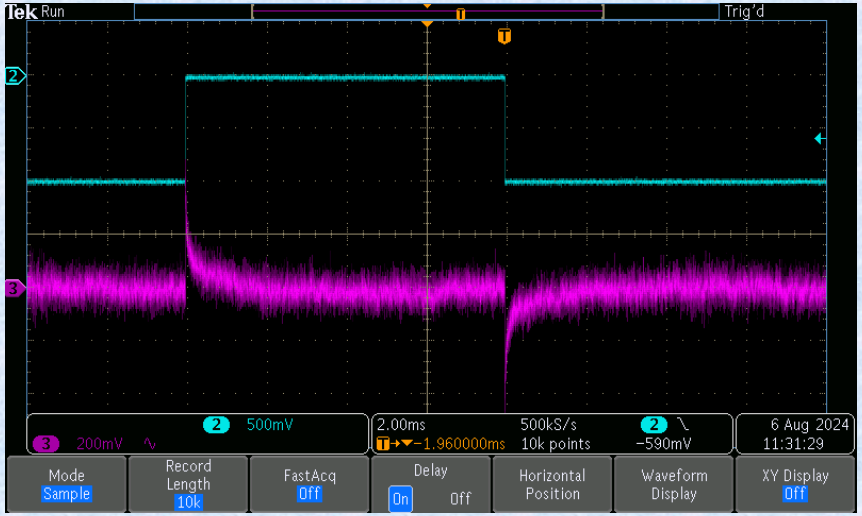
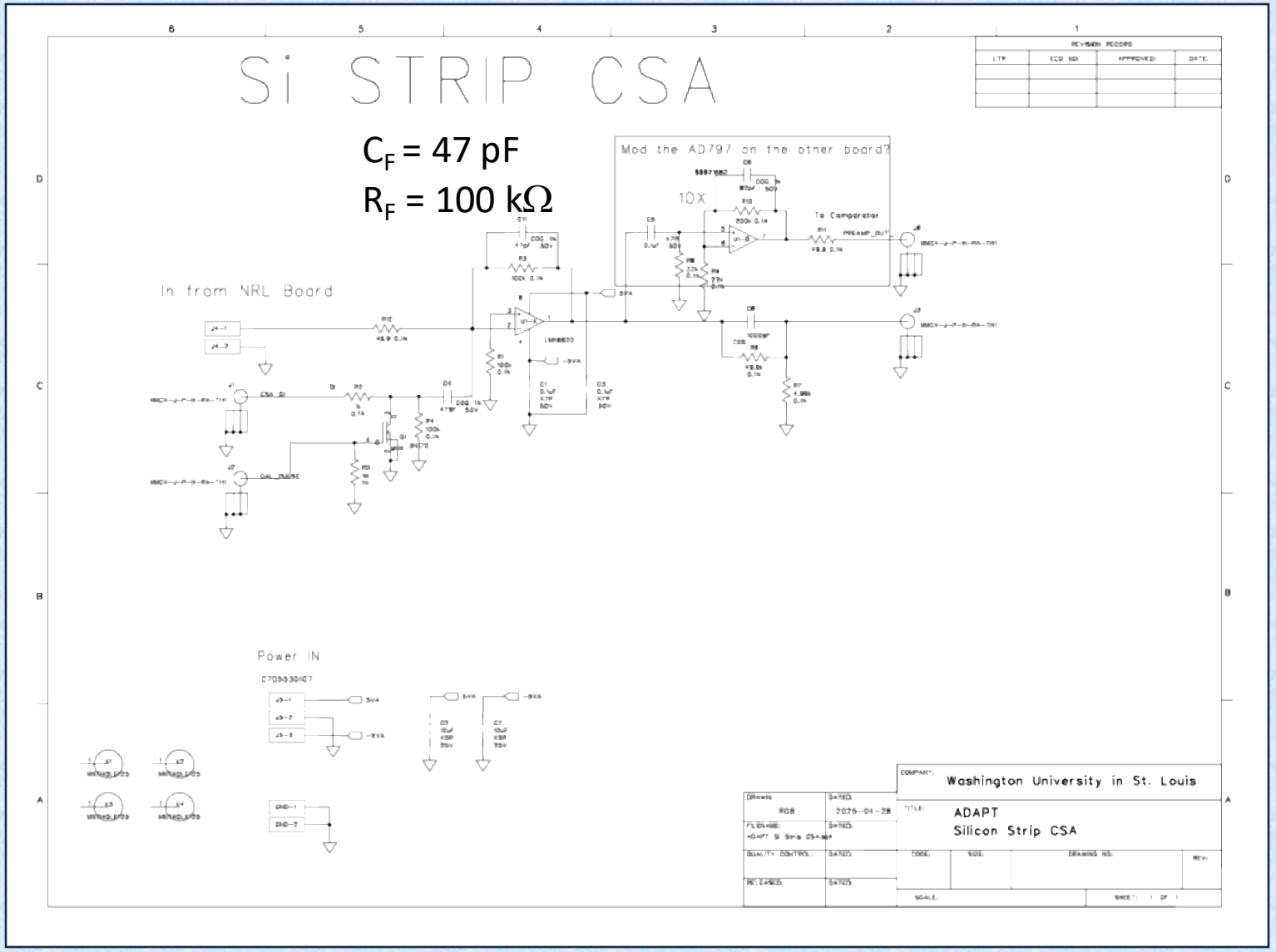
Ultra-Low Noise at Both High & Low Frequencies With a Narrow Range of IDSS

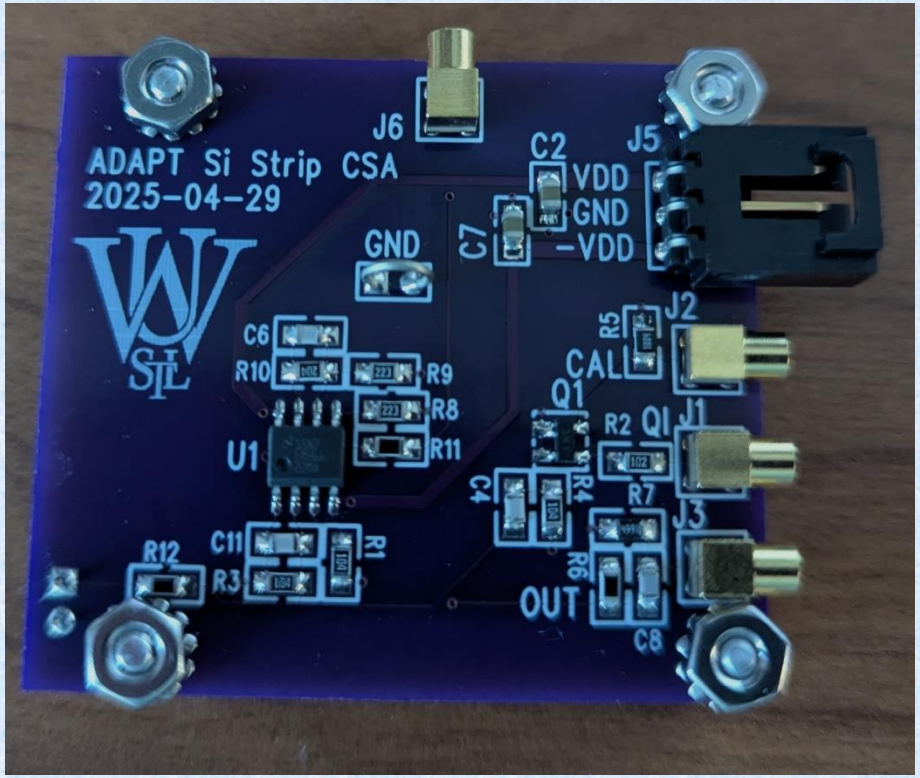
Absolute Maximum Ratings @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +135°C
Maximum Power Dissipation	
Continuous Power Dissipation @ +25°C	400mW
Maximum Currents	
Gate Forward Current	$I_{G(F)}$ = 10mA
Maximum Voltages	
Gate to Source	V_{GSS} = 40V
Gate to Drain	V_{GDS} = 40V

TO-92 3L TOP VIEW (D G S) SOT-23 3L TOP VIEW (G D S) SOT-89 3L TOP VIEW (G S D)



ADAPT CSA for Ohmic Readout





Ohmic CSA Performance Requirements

The dynamic range and signal rail from TIGERISS used in Table below.

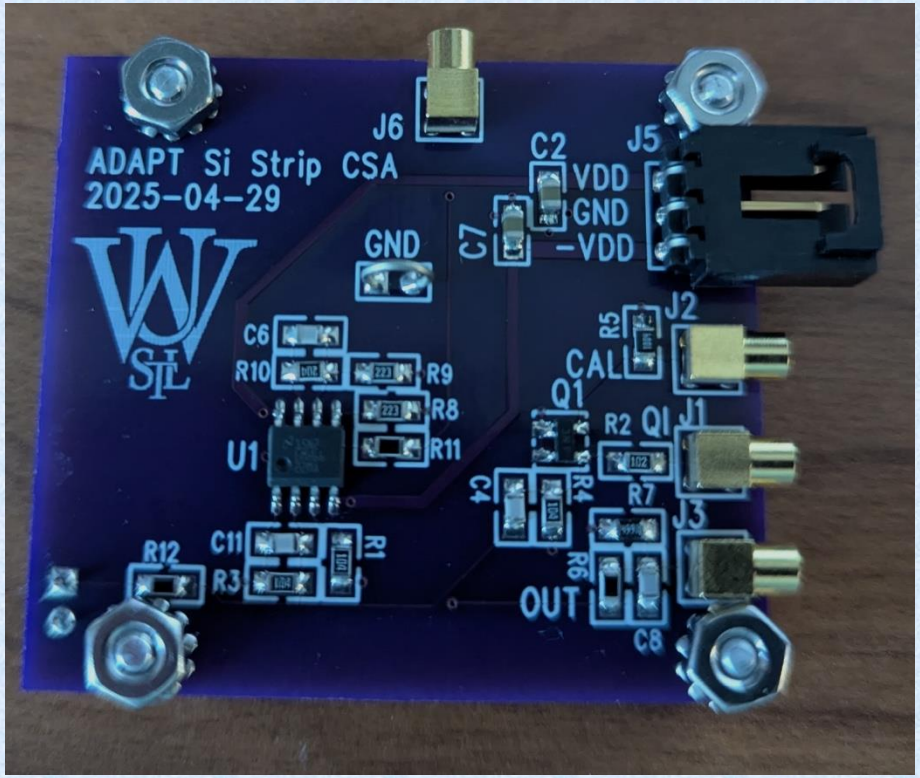
	Specifications/Requirements			Comments
Nominal Detector Thickness [um]	500 +/- 3 um			+/- 3 um needed to get Qres <= 0.25 at Z=82
Minimum detector thickness	485 um			to get Qres <= 0.25 at Z=82 w/+/- 3 um
Maximum detector thickness	520 um			to get Qres <= 0.25 at Z=82 +/- 3 um
ADAPT SSD Thickness Range	498 – 520 um			12 ADAPT SSDs (Measured by Micron)
Min Charge Measurement MIP [fC]	1/2 signal of normal incidence Z=2 [fc]	0.012	**0.012**	fC, using MostProb MIP 23.50 fC in 500 um silicon length
Max Qmeasure MIP [fC]	signal of Z=42 (Molybdenum) at 60 deg [fc]	2.7e4	**20700**	fC, rounded up
Bragg Scale Factor (400 Mev/nuc)	400 MeV/nuc lowest energy measured	1.7		Using Scott's GEANT 4 MC for dE/dx curve
Max Qmeasure Absolute [fC]		3.52e4	**35200**	fC, rounded up
Measurement Dynamic Range	**0.012 -> 36 pC**	**3000**	**1.0**	**mV signal assuming 3 V rail for ASIC**
sqrt[trig sig [electrons]	677		458591	Min Qmeas in electrons
Noise [ENC}	ENC for 3 sigma			
	ENC for 5 sigma			
Max Volt into ADC	4.096 V			1.4 mV signal at threshold
CSA FeedBack Capacitance [pF]	=36e-12 [C]/4.096 [V] ~ 8.8 pF			
Min ADC Bit count	to get helium< 0.25 cu	15		Mathematically, ADC res only, noise dominates Qres, I noise ½ MIP , then < 0.25 cu

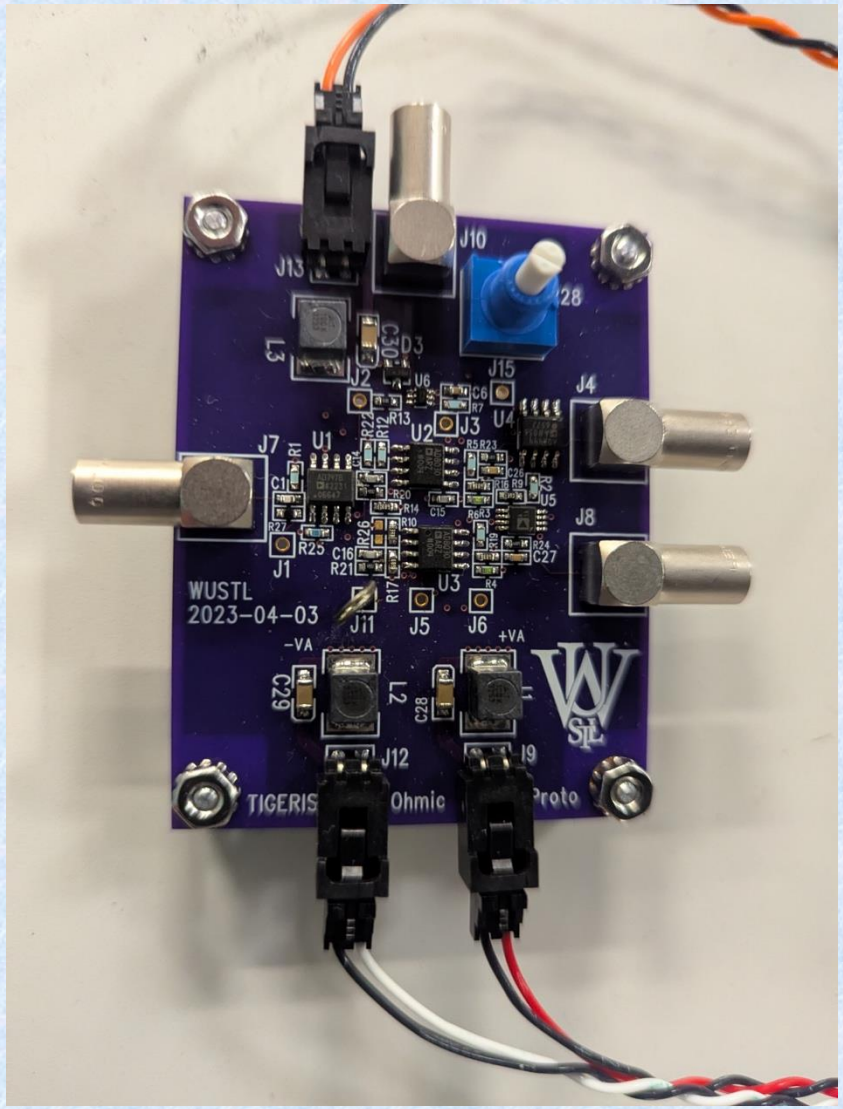
CSA Range Discussion

Min Charge Measurement MIP [fC]	1/2 signal of normal incidence Z=2 [fc]	0.012	**0.012**	fC, using MostProb MIP 23.50 fC in 500 um silicon length
Max Qmeasure MIP [fC]	signal of Z=42 (Molybdenum) at 60 deg [fc]	2.7e4	**20700**	fC, rounded up
Bragg Scale Factor (400 Mev/nuc)	400 MeV/nuc lowest energy measured	1.7		Using Scott's GEANT 4 MC for dE/dx curve
Max Qmeasure Absolute [fC]		3.52e4	**35200**	fC, rounded up
Measurement Dynamic Range	**0.012 -> 36 pC**	**3000**		**1.0 mV signal assuming 3 V rail for ASIC**
Max Volt into ADC	4.096 V			1.4 mV signal at threshold
CSA FeedBack Capacitance [pF]	=36e-12 [C]/4.096 [V] ~ 8.8 pF			

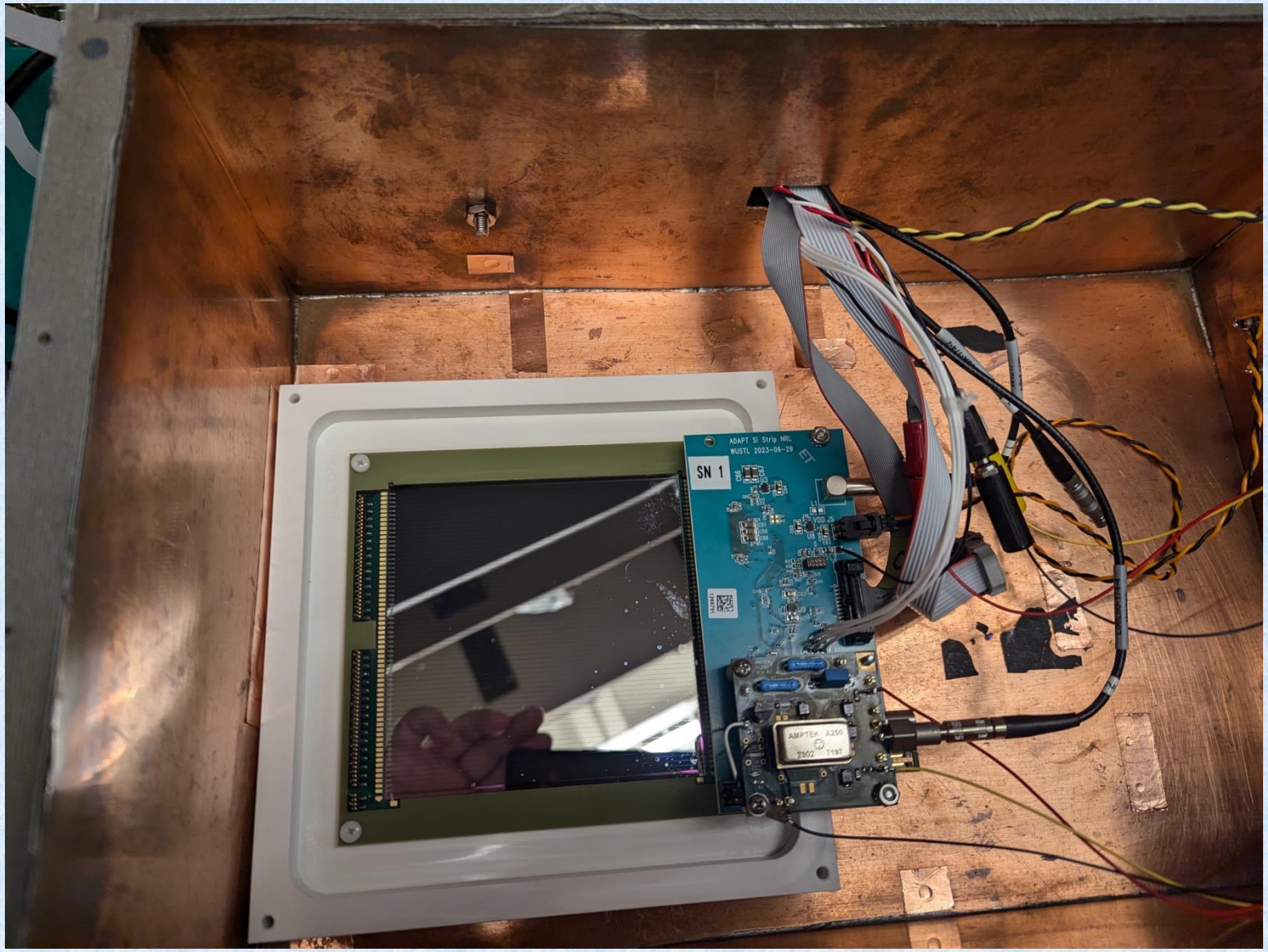
- **Currently have C_F = 47 pF in CSA which has too low gain for ^{42}Mo as maximum signal, but is near TIGERISS range.**
- **Setting C_F = 8.8 pF in CSA set ^{42}Mo as maximum with ^{2}He as lowest signal using dynamic range achieved in CSA based on Satpal Singh's TIGERISS design (but need to verify this on bench).**
- **At this point open to discussing nuclear measurement range for ADAPT.**

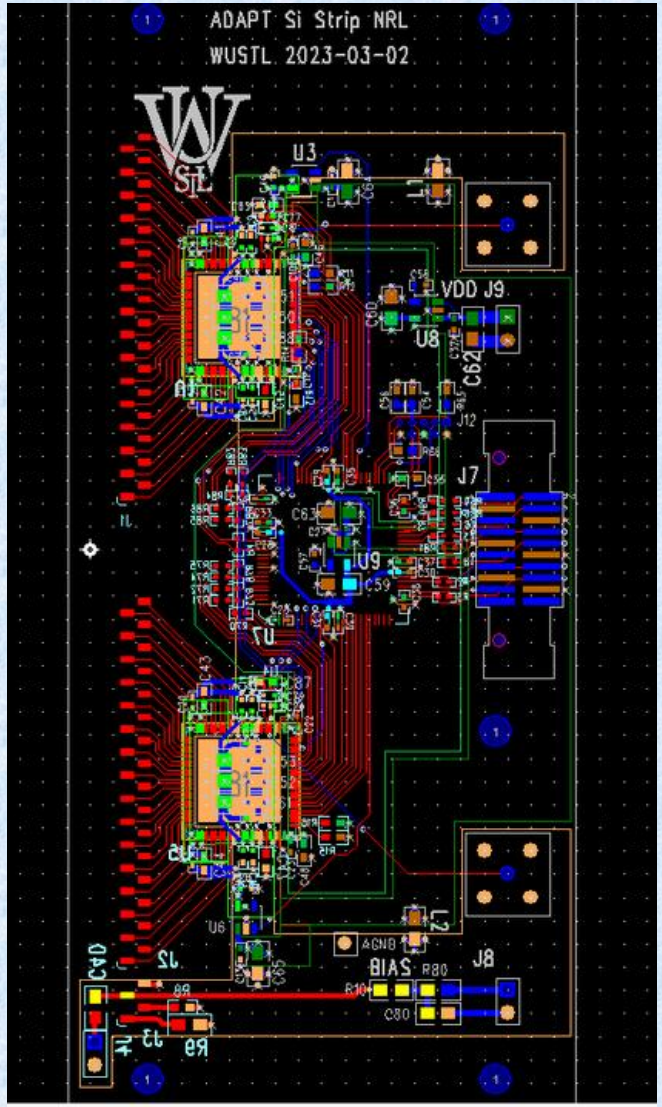
Next step test CSA with Ohmic SA + Trigger board prototype





NRL Board Status





NRL ASIC Anticipated Performance

NRL1

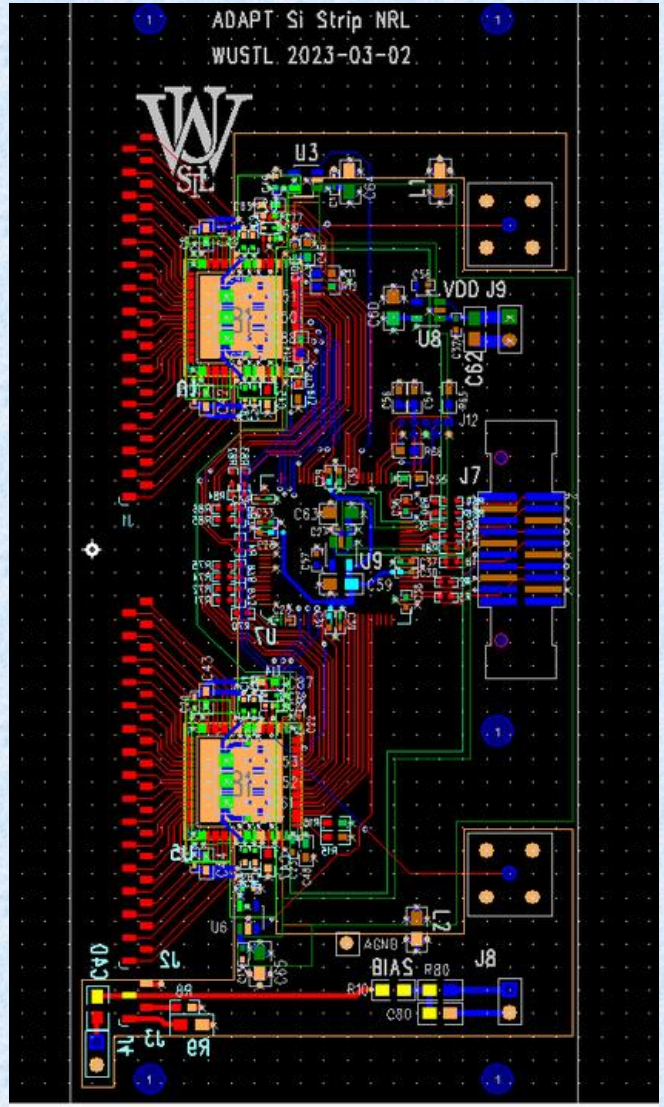
rev. 0 - June 2017

Wenbin Hou and Gianluigi De Geronimo - Stony Brook University

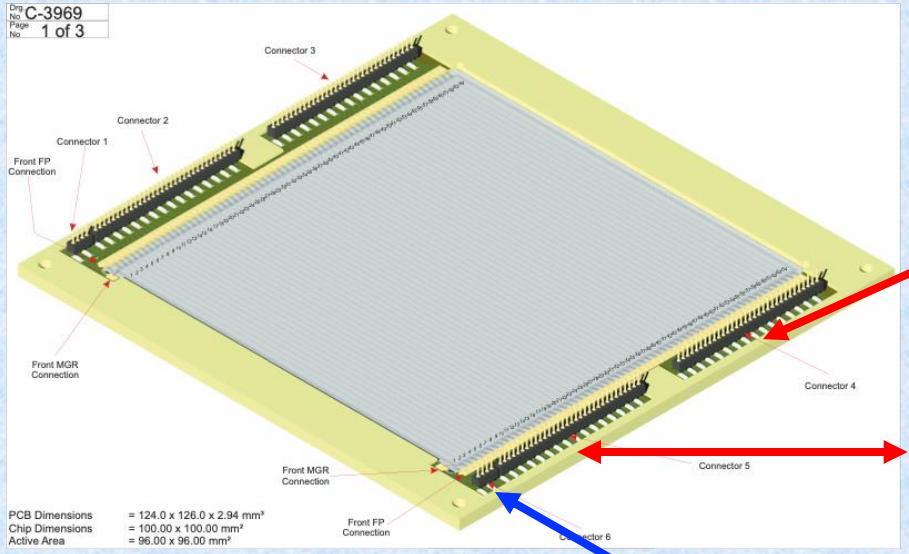
- **Power dissipation**: ≈ 197 mW (4.82mW/channel +43mW)
- **Front-end channels** : 32
  - charge preamplifier, 5th order shaping amplifier, peak detector, time detector, multiplexing
  - charge preamplifier polarity : selectable positive or negative
  - integrated test capacitor: ≈ 200fF
  - shaping amplifier peaking time: selectable 250ns, 500ns, 1µs, 2µs
  - channel gain: selectable 9.2, 18.4, 36.8, and 73.6 mV/fC (baseline ≈ 250mV, max signal ≈ 2V from baseline)
- **Layout size** 5435 × 4922 µm²
- **Die cut size** TBD
- **Pad count, size, pitch** 80, 68 × 68 µm², 247.8 um (top/bottom) and 220.8µm (sides)
- **Technology** : CMOS 0.25µm 2.5V, 1-poly, 5-metal, MiM capacitors, slbk resistors

- Gains are very large, so Z>2 signals will hit the rail hard.
- Minimal Gain: 9.2 mV/fC x 36,000 fC = 331.2 V !!

Max Signal [V from Baseline]	2.0			
Baseline [V]	0.3			
Vspan [V]	1.8			
Gain [mV/fC]	9.2	18.4	36.8	73.6
Max Q [fC]	190.2	95.1	47.6	23.8
Max Z , MIP Normal Incident, [5.87 fC in 500 um Si]	5.7	4.0	2.8	2.0
MaxZ, 400 MeV/nuc, 60 deg [11.7 fC for 60 deg in 500 um Si x 1.7 for Bragg Increase = 19.9 fC]	3.1	2.2	1.5	1.1



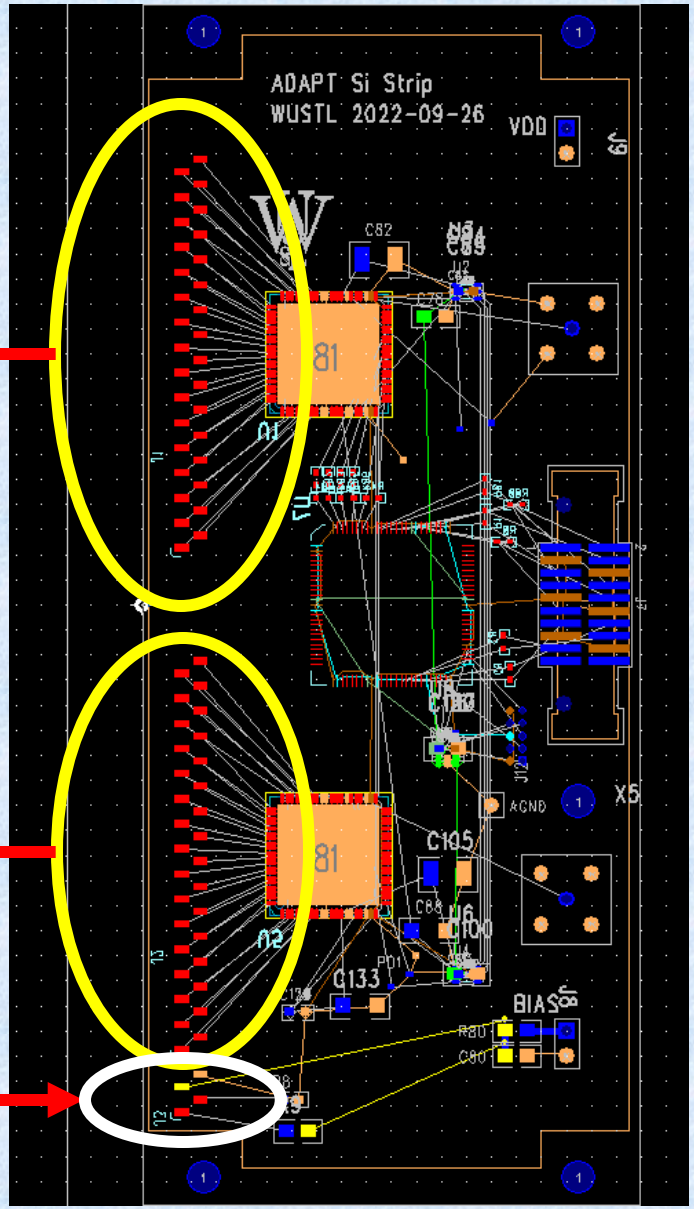
NRL Board Connection to SSD in PCB



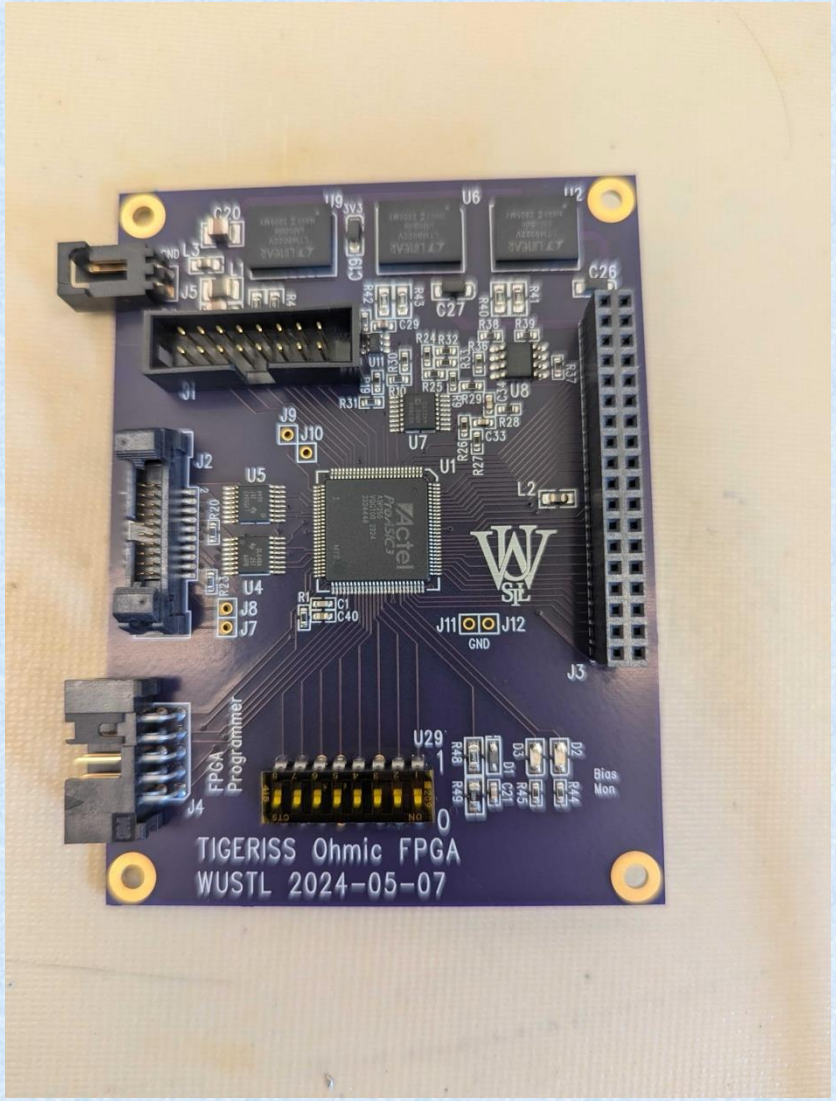
ASIC1: channel 1, 2, …,31,32
J1-1 Channel 1, leftmost, lowest pad

ASIC1: channel 1, 2, …,31,32
J2-1 Channel 1, leftmost, lowest pad

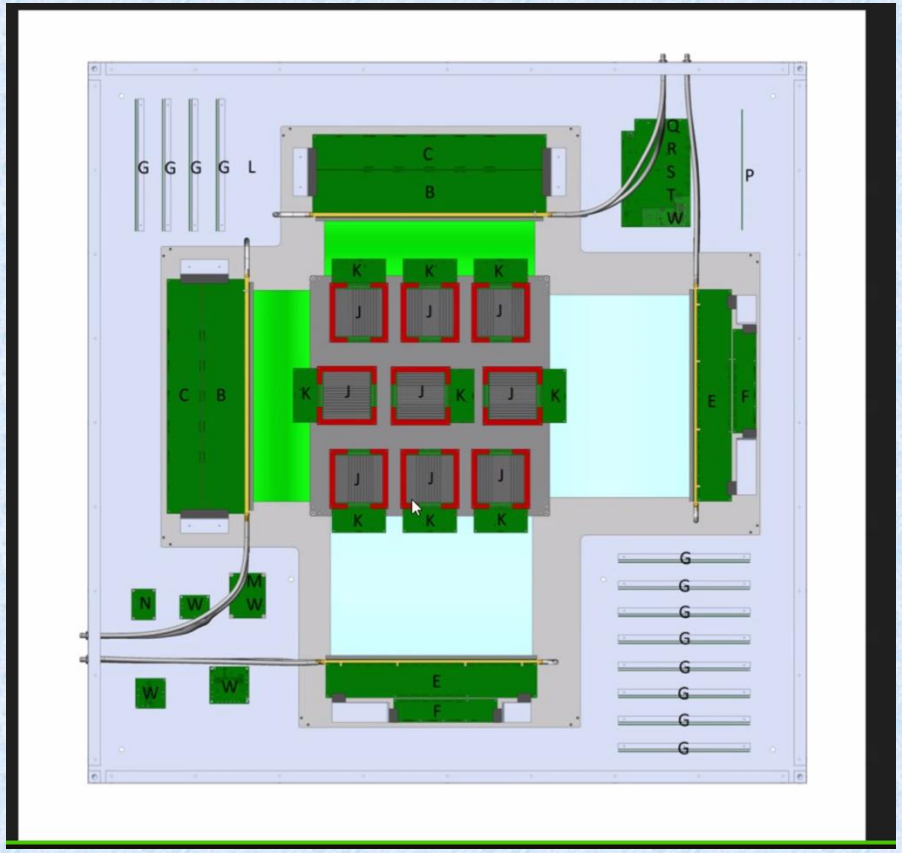
J3-1 GUARD_RING
J3-2 FIELD_PLATE
J3-3 BIAS
J3-4 GND

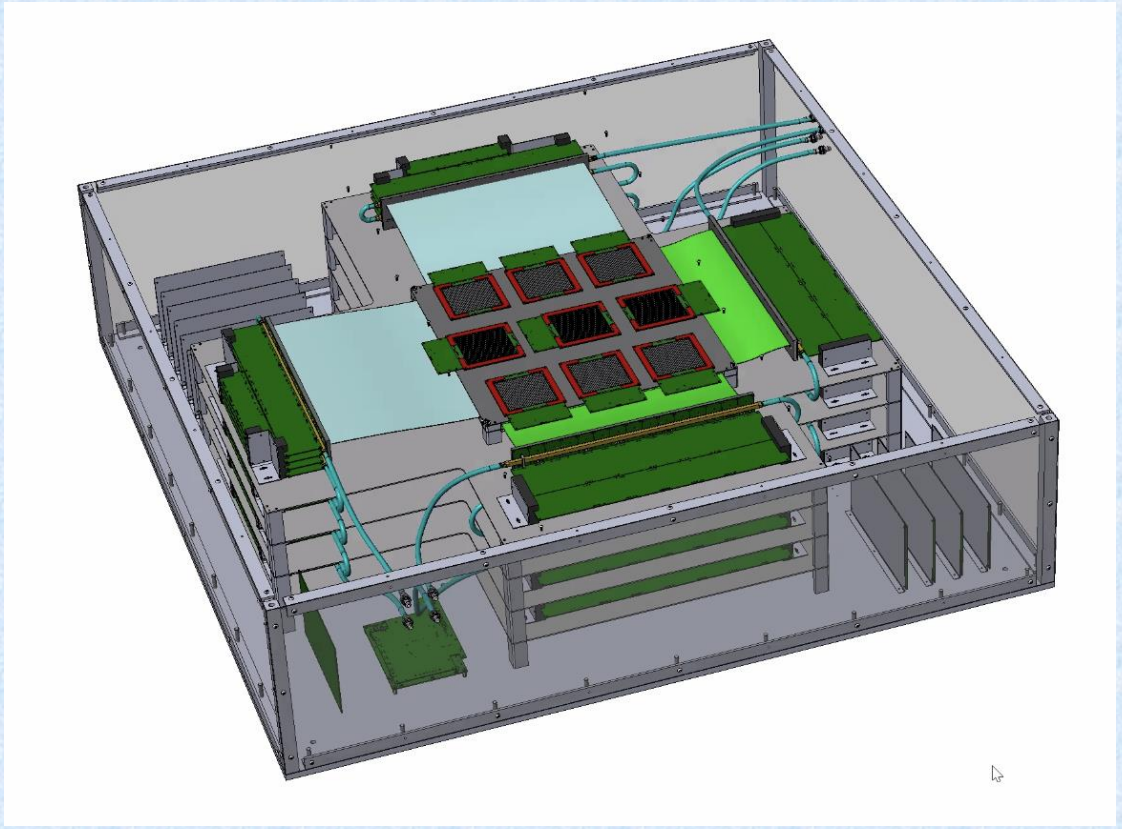


SSD Digital Board Status/Vbias Board Status



Backup Slides





Micron SSD Specifications

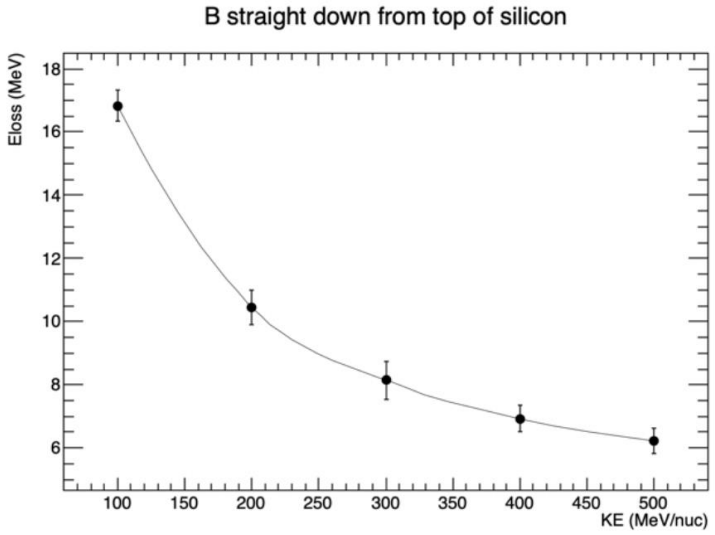
Table 1: Silicon Strip Detector (SSD) Specifications for ADAPT

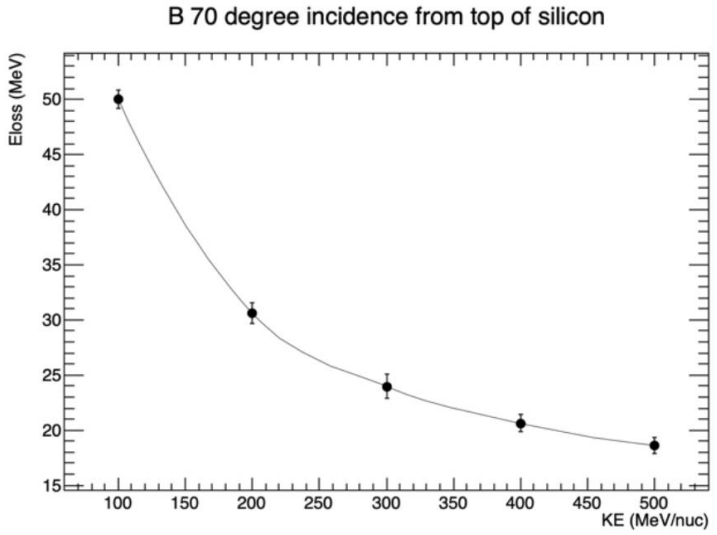
BEST EFFORT/TARGET SPECIFICATION to be used to determine FINAL FLIGHT SPECIFICATION

Design TTT10 (SS) 500 - Type 2M /2M (DC MICROSTRIP)
Window Type 2M /Uniform Aluminium+ Implant Window<1um on both faces.
Single Sided DC Coupled Silicon 64 channel micro-strip
Silicon n-Type FZ <100> orientation
Silicon Resistivity: 10K typ 20K maximum subject to crystal selection.
Design Structure: Ion implanted multi-guard with field plate
Active Area: 100mm x 100mm
Thickness: 500 micron +/- 5 microns TARGET 500+/-/TTV 2 microns (Total Thickness Variation)
Thickness Uniformity +/- 2.5 micron
No. of channels: 64
Strip Pitch 1.5mm
Strip Width 1.4mm
Interstrip Oxide 100um
Full Depletion (FD) 60volt minimum 150 V maximum
Operating Voltage FD to FD + 30V
Total leakage current (FD + 30V) (20C) 2uA maximum
Strip Leakage Current 30nA typical, 100nA maximum (End strips 200nA/max.)
Interstrip Junction 10M min 100M typical (ohms)
Metallising Aluminium 5000Angstroms+/-500Angstroms
Total Alpha (junction) 150keV 1uS shaping maximum. Individual strip alpha < 55KeV FWHM 1uS Total Alpha (ohmic) 150keV 1uS shaping maximum. Individual strip alpha <55KeV FWHM 1uS Operating Alpha Plateau(Ohmic) 30Vminimum 100V maximum
Quality:Substandard but operational channels 2 maximum(usually endstrips higher leakage current as include guard-ring leakage current contribution.
Minimum Acceptance Level(100%) All Channels Operational

Energy loss in 500 um of Silicon in via GEANT4 (Scott Nutter)

B10 from top of Si (500 microns)





KE(MeV/n)	Peak (MeV)	Sigma (MeV)
100	16.8333	0.505503
200	10.4594	0.548648
300	8.13988	0.603457
400	**6.92591**	**0.429773**
500	6.22656	0.414278
1000	4.89483	0.384203
2000	4.38208	0.371092
3000	4.28133	0.367876
5000	**4.26537**	**0.369174**
10000	4.31336	0.374017
20000	4.3672	0.359729
30000	4.40682	0.356846
50000	4.44747	0.356763
80000	4.46046	0.359352
100000	4.48076	0.356806

Assume 400 MeV lowest energy for nuclei
6.92/4.26 = 1.62 ~ 1.7