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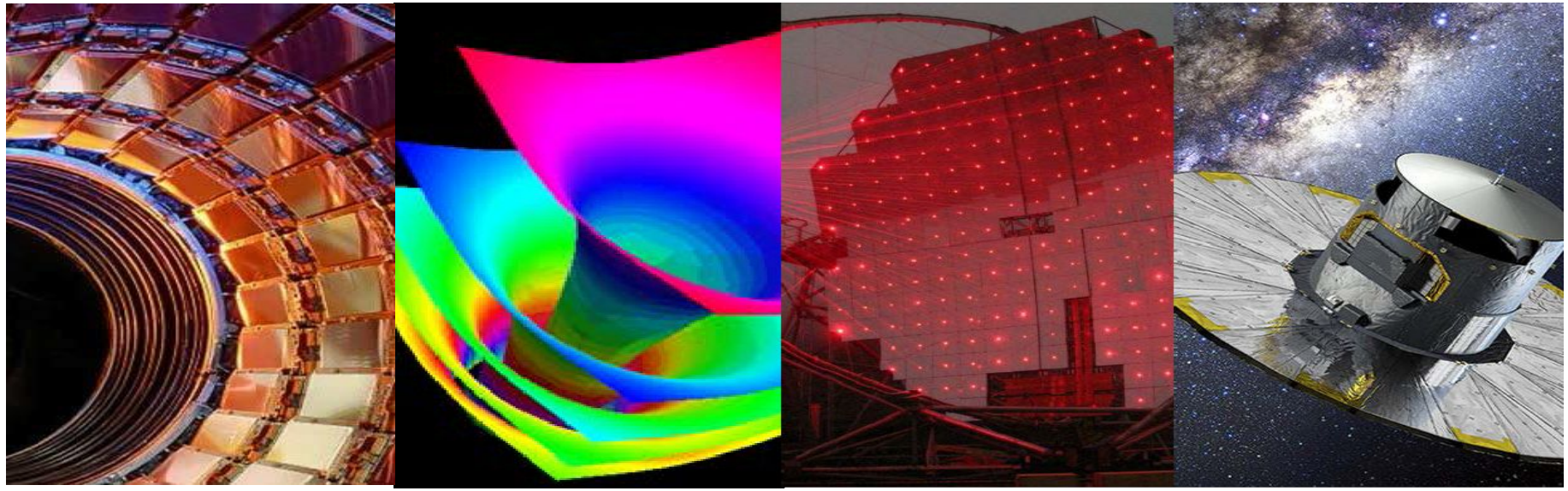


BETA, a low-power, high-dynamic range, radiation-tolerant 64-channel ASIC for space applications and beyond

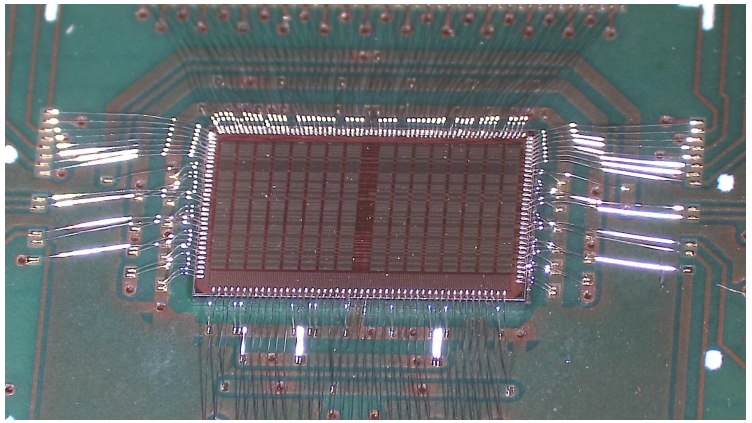
A. Sanuy, R. Catala, A. Comerma, D. Gascon, A. Espinya, D. Guberman, S. Gomez, J. Mauricio, R. Manera, M. Orta, O. de la Torre

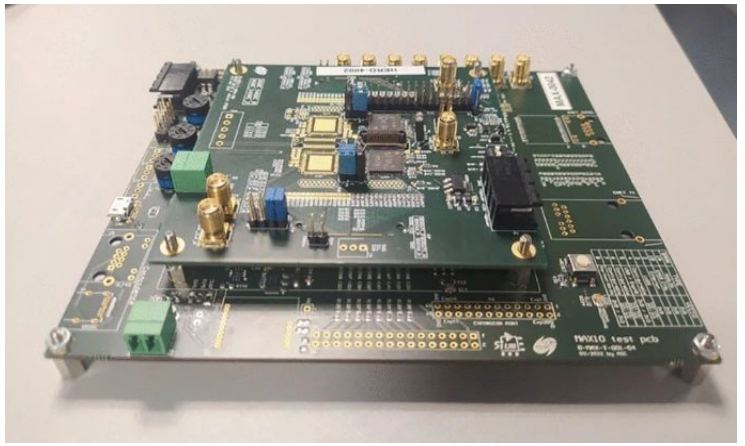
ADAPT Collaboration Meeting 2025

05 November 2025

BETA: a low-power ASIC for SiPM readout in space (and beyond)

- Provides a **digital output** for **16/64 SiPM channels**
- **Low** power (1 mW/ch) consumption
- Excellent resolution for **single photons**
- High **dynamic range (15 bits)**
- For low rate (< 100 kHz) applications
- Designed to be **radiation tolerant**
- Starting the procedure for its **space qualification**

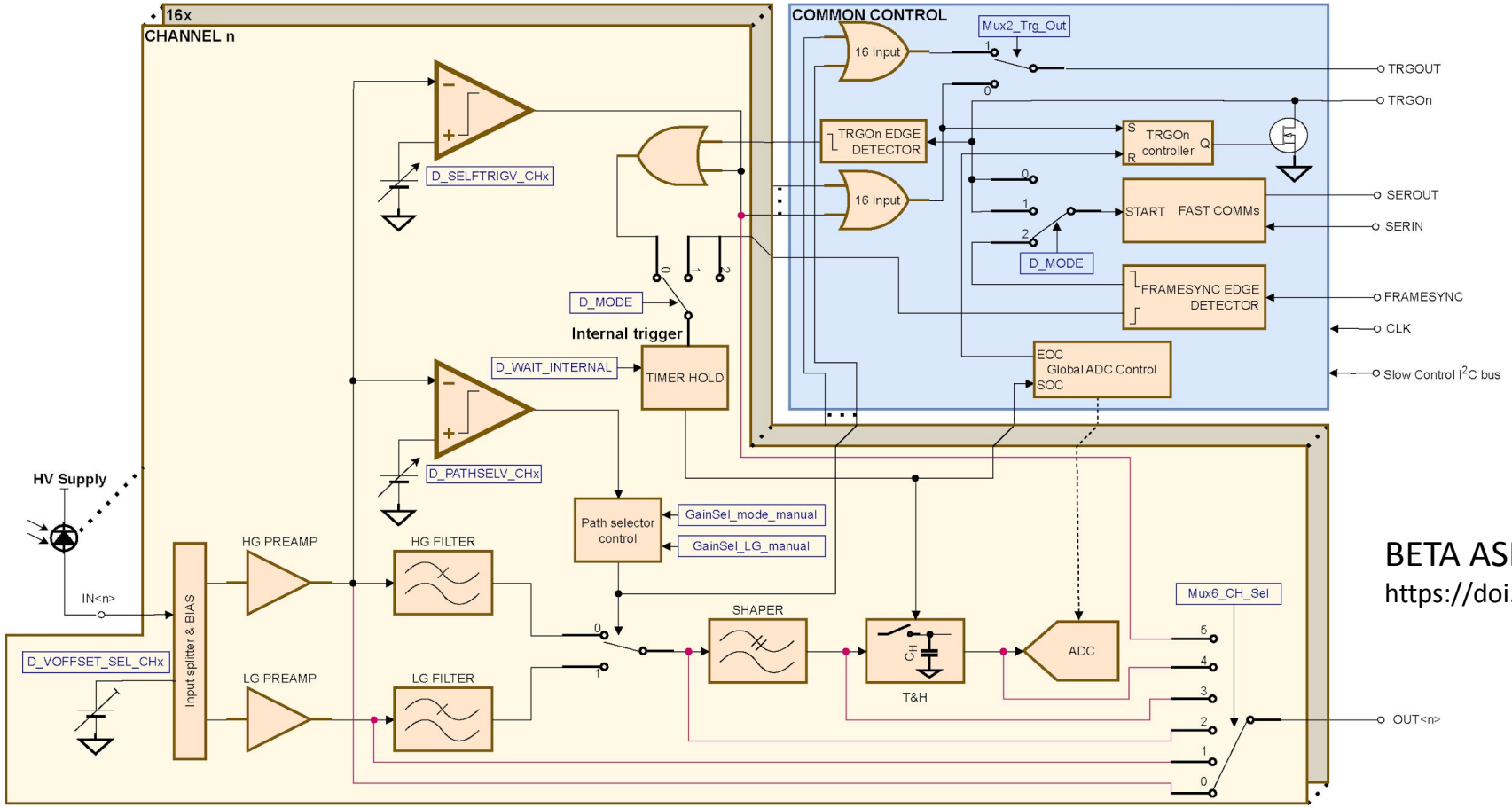




BETA ASIC: A. Sanmukh et al., https://doi.org/10.1007/s41365-024-01419-z

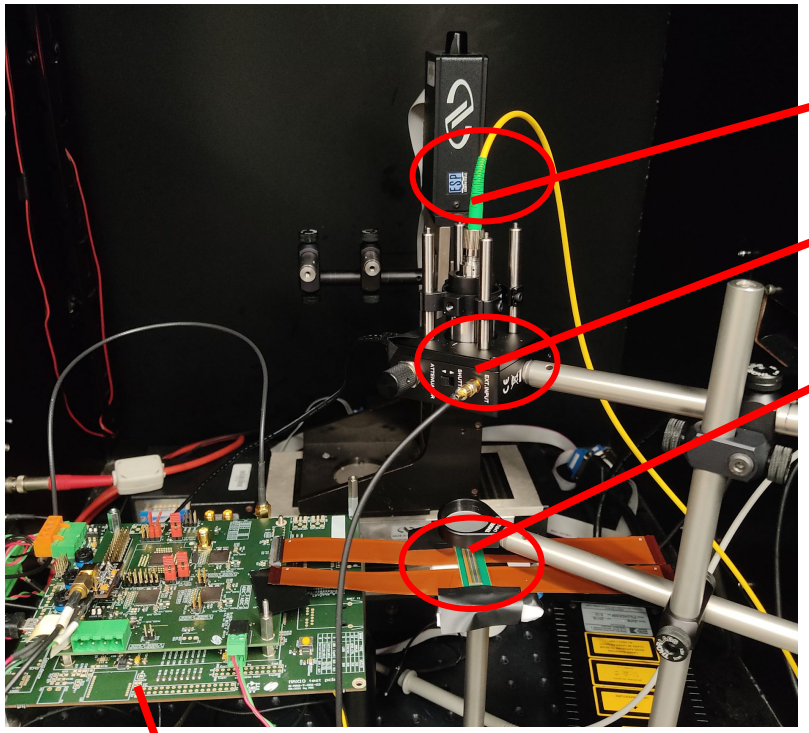
BETA - Architecture

- ✔ Channels: 16 (FIT version: 64 ch)
- ✔ Event rate : 10 kHz (100 kHz) max
- ✔ Configurable preamplifer gain: 4 bits
- ✔ Tunable shaping time: 150 ns to 1.5 us
- ✔ Trigger output: < 250 ps time resolution
- ✔ Single photon resolution: SNR >10
- ✔ Dual path: automatic gain switching
- ✔ On chip ADC: Wilkinson11 bit + 1bit (path sel)
- ✔ Dynamic Range : 15 bit
- ✔ Slow Digital Control : I2C



BETA ASIC: A. Sanmukh et al., https://doi.org/10.1007/s41365-024-01419-z

Performance: Measurements Setup



Laser System

Liquid crystal attenuator

Sensor PCB

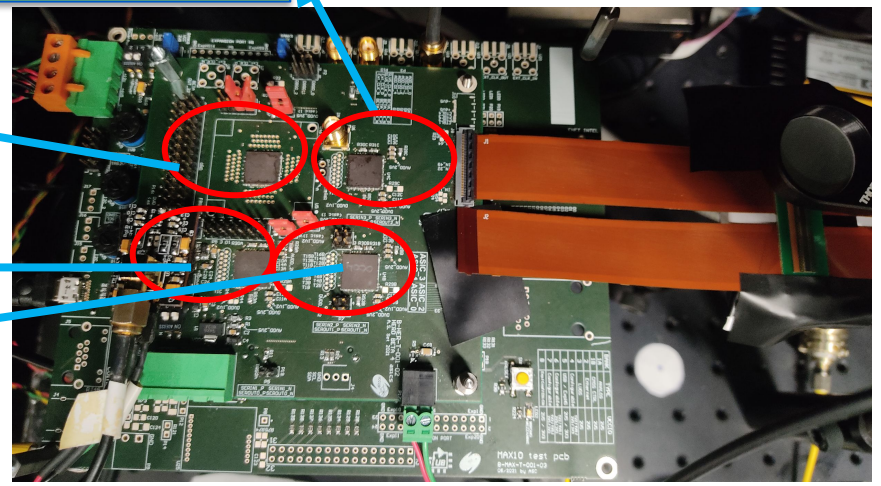
Test System
1. SiPM PCB
2. Analog PCB
3. Digital PCB

HERD ASIC 0

HERD ASIC 1

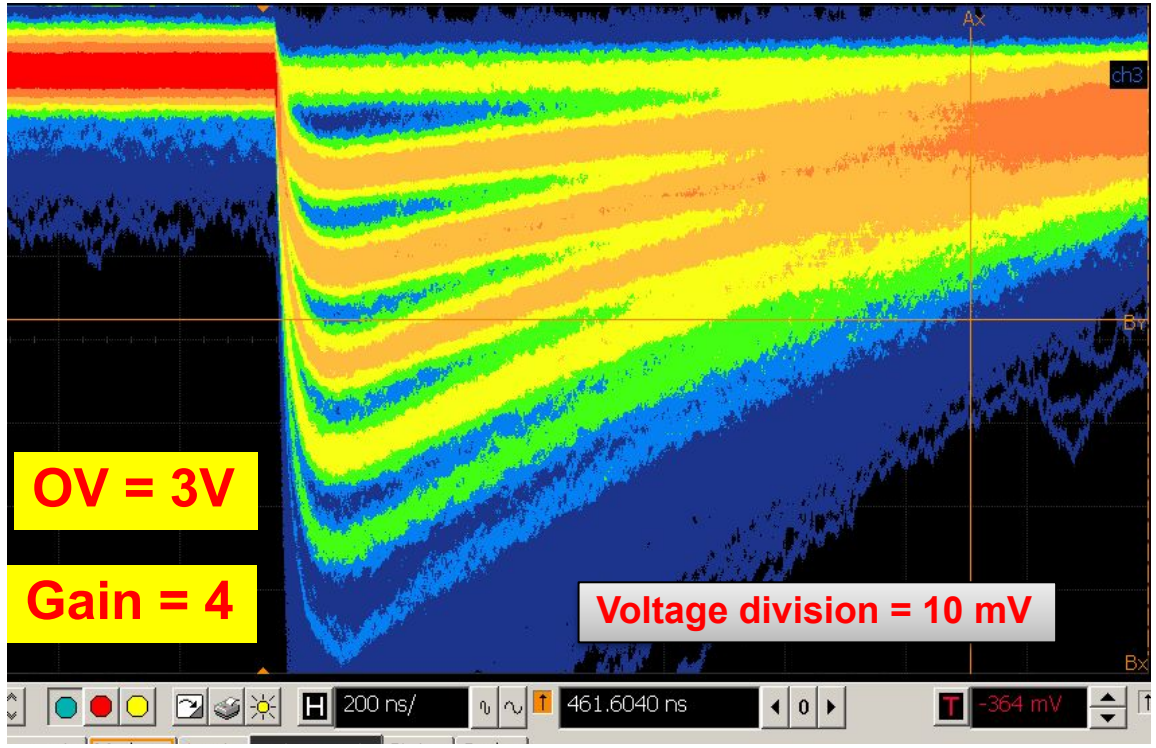
HERD ASIC 2

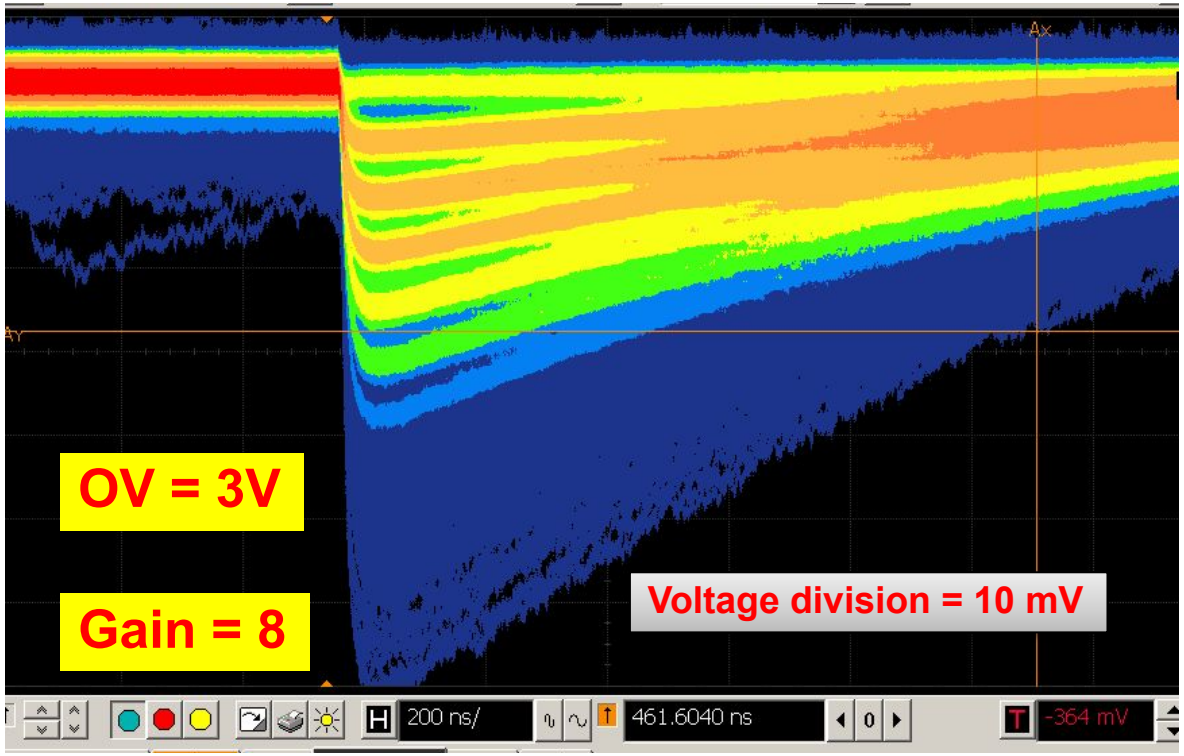
HERD ASIC 3



Digital PCB (FPGA)

Performance: Analog HG preamplifier output

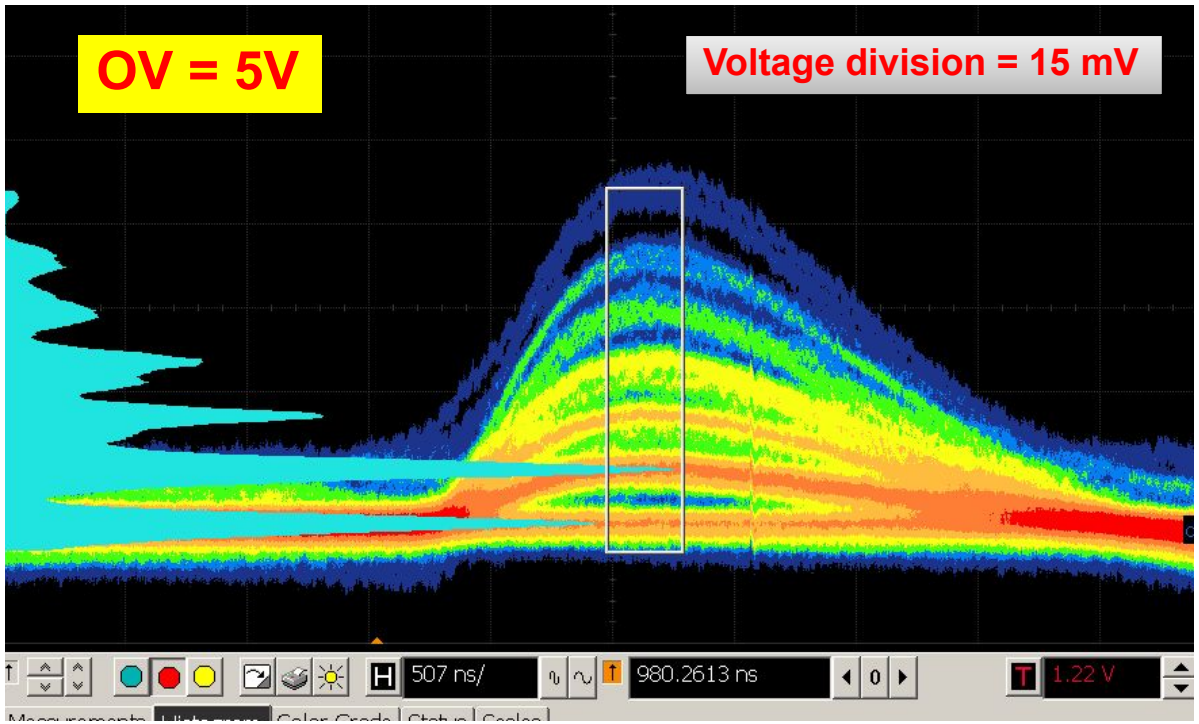


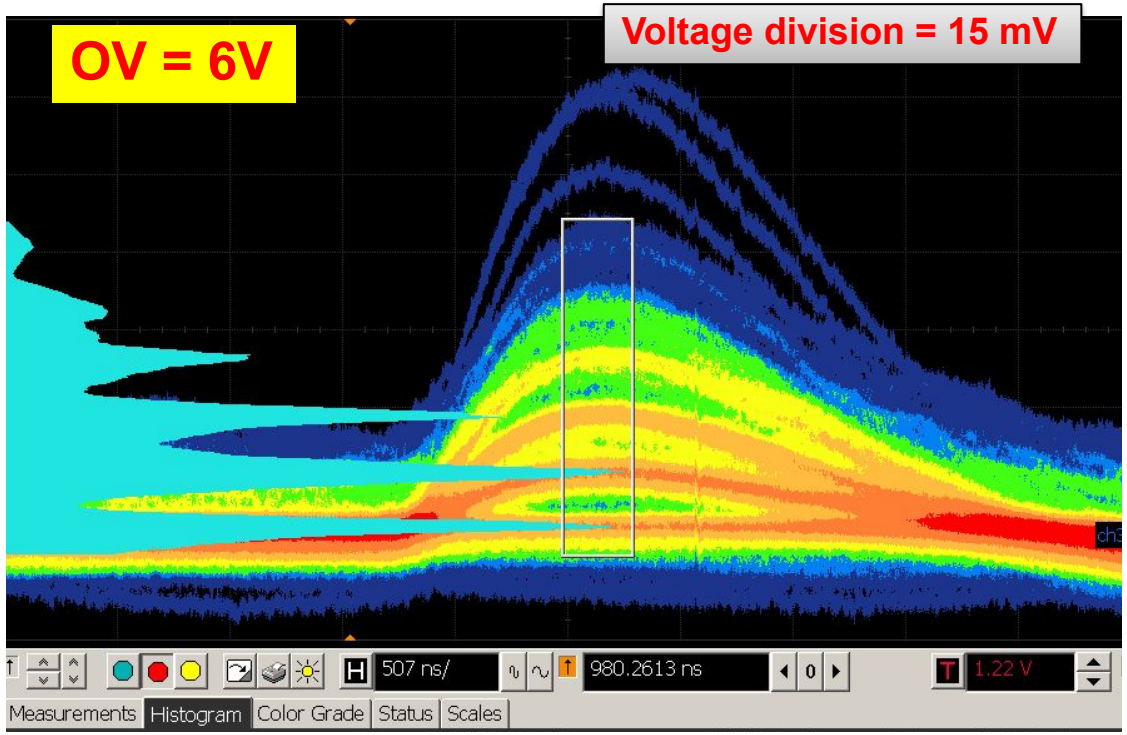


Oscilloscope colour grade capture for various number of photons showing the input HG preamplifier Output for HG path selection

Sensor: SiPM FIT HERD 128 ch array.
SiPM ch: 3749 microcells of 10x10 μm2 (0.23x1.63 mm2)

Performance: Analog Shaper output

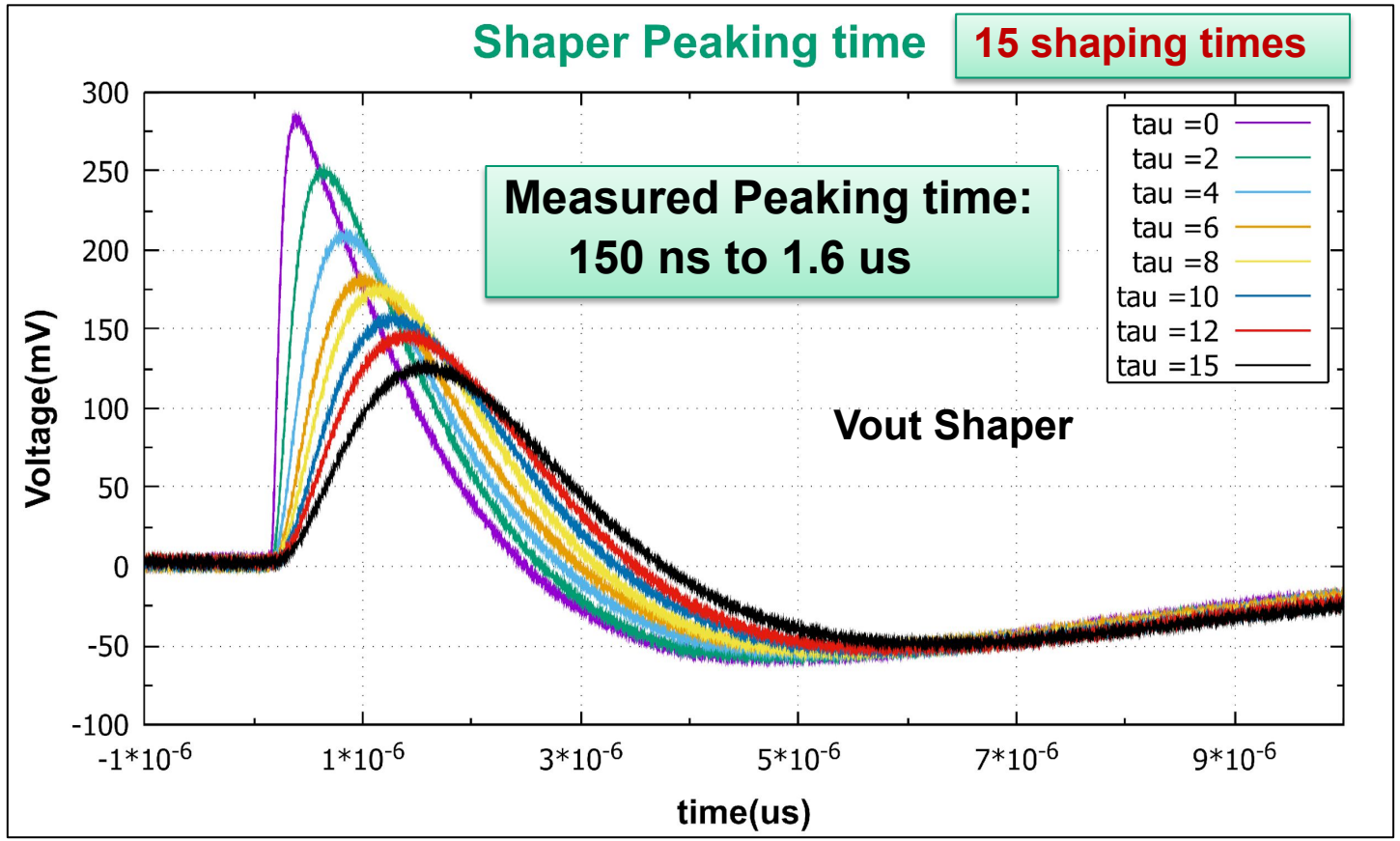




Oscilloscope colour grade capture for various number of photons showing the Shaper Output for HG path selection

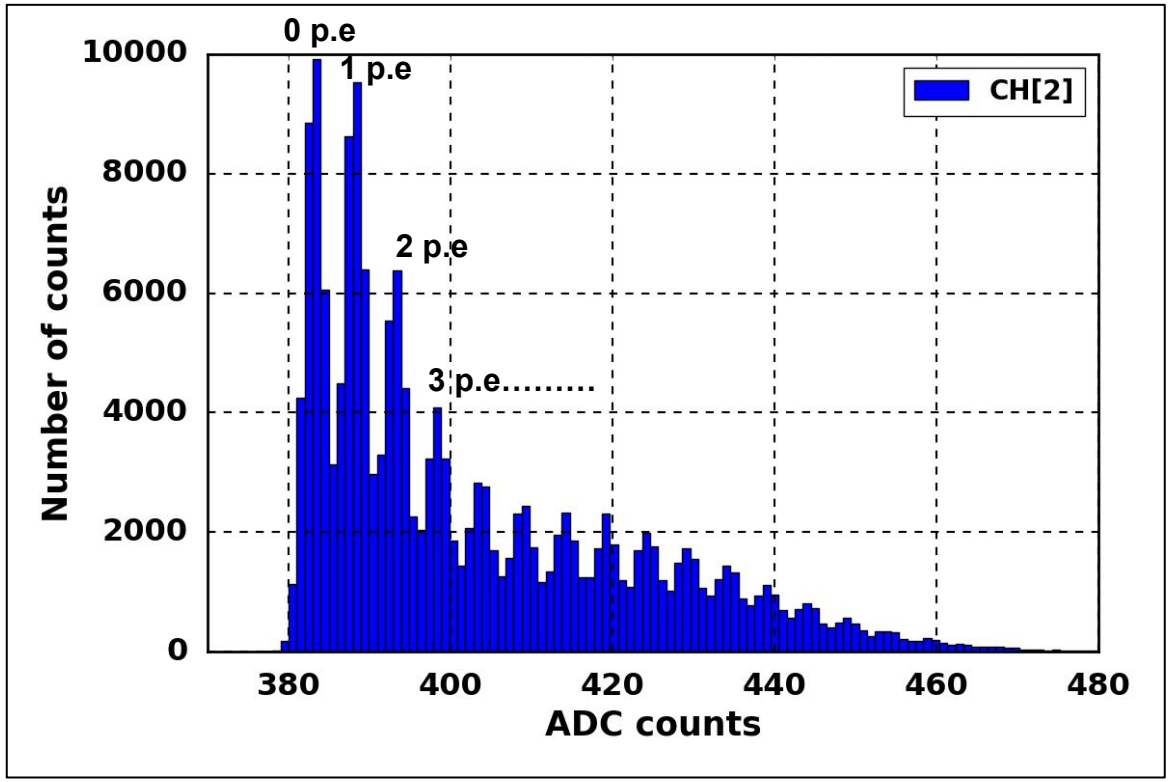
Sensor: SiPM FIT HERD 128 ch array.
SiPM ch: 3749 microcells of 10x10 µm2 (0.23x1.63 mm2)

Performance: Shaper Peaking Time



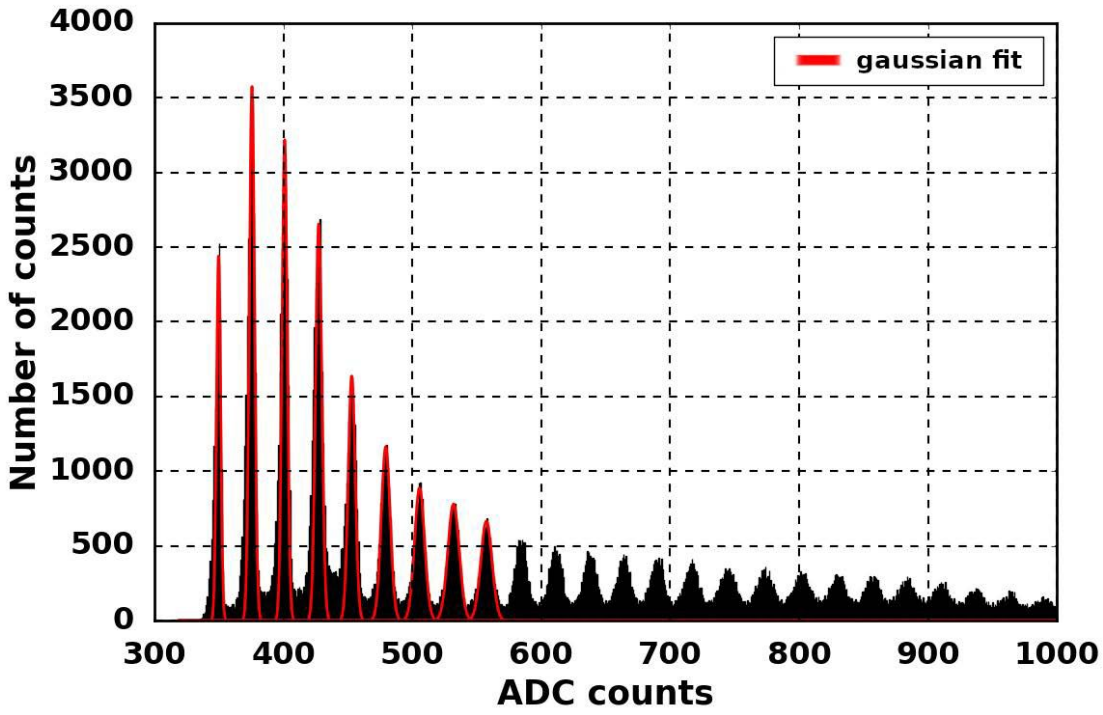
- ❑ The filter implemented is Butterworth Approximation- provides a roll off of -20 dB/decade/order
- ❑ Total 16 shaping times (from ~150 ns to ~ 1.6 µs) are available for these slow shapers

Performance: HG Output Amplitude Measurements



SiPM FIT HERD 128 ch array. OV = 3.5 V
SiPM ch: 3749 microcells of 10x10 μm^2 (0.23x1.63 mm^2)

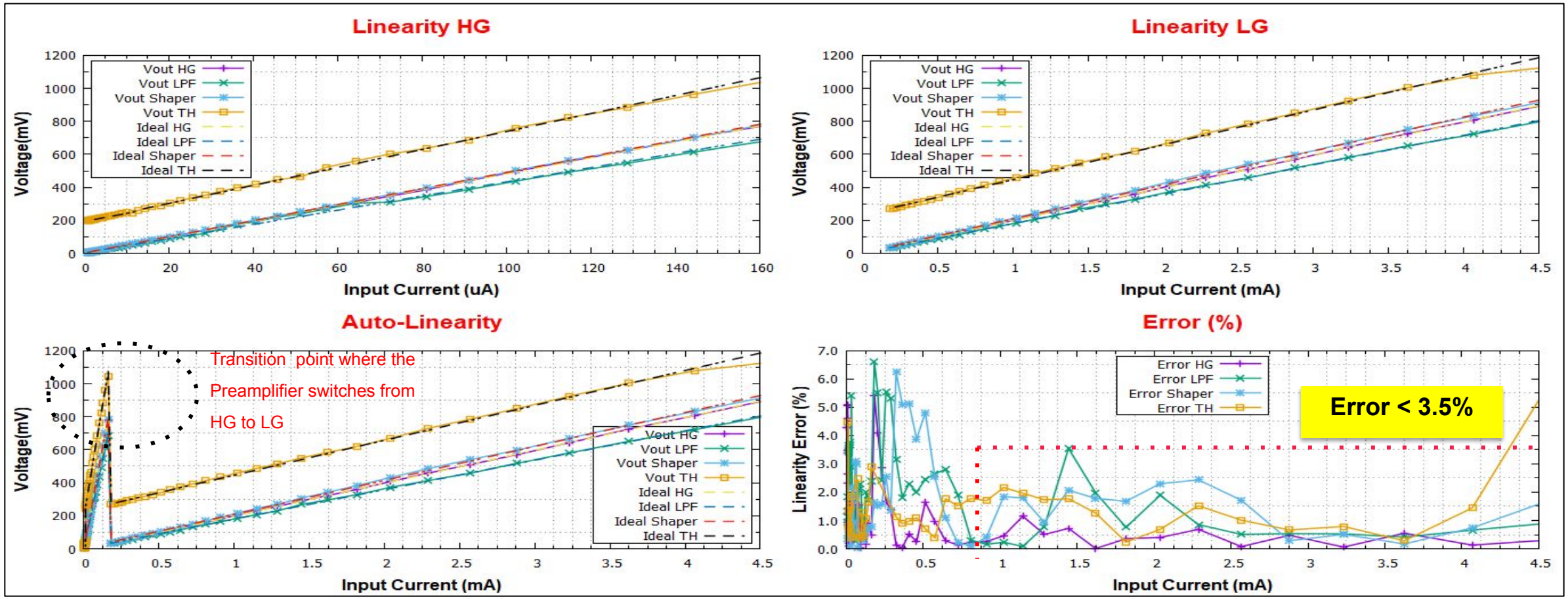
- ❑ Higher dynamic range but lower gain and PDE
- ❑ Charge identification and calorimetry



S13360-1350CS. OV = 2 V
676 microcells of 50x50 μm^2 (1.3x1.3 mm^2)

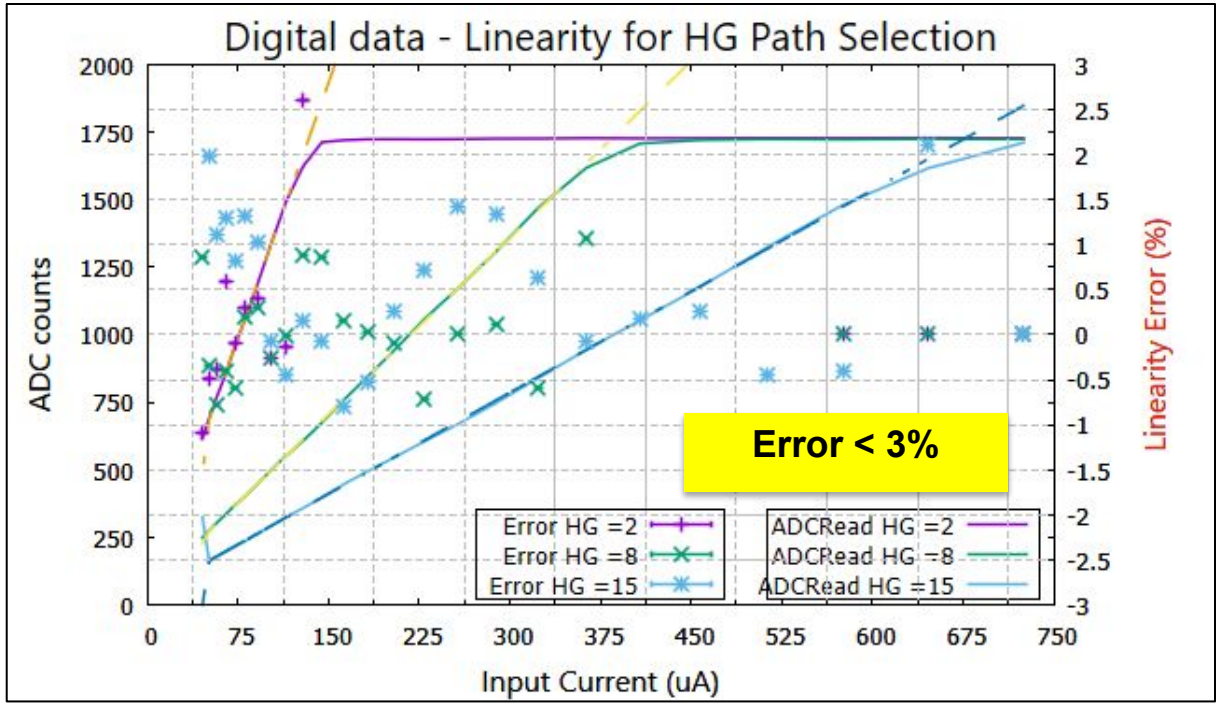
- ❑ Higher gain and PDE, lower dynamic range
- ❑ MIP detection (tracker, trigger and ToF)

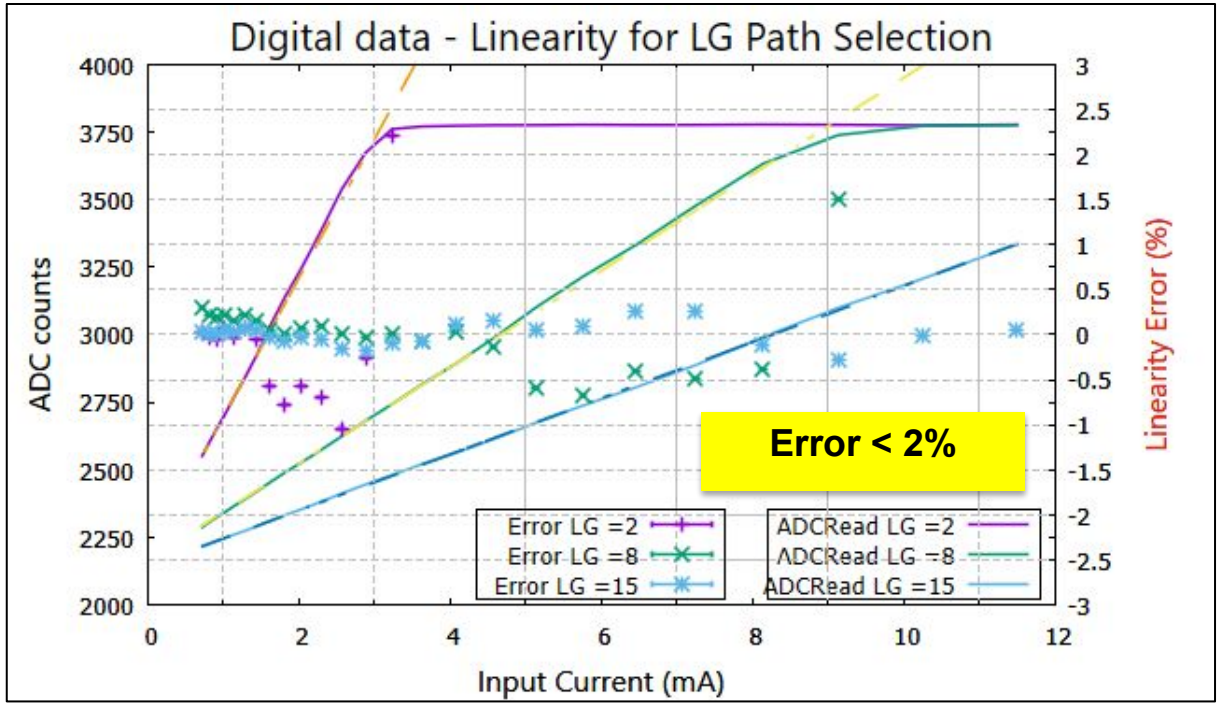
Performance: Analog Voltage measurement Linearity & Error



- The above plot shows the HG and LG response (top) and with auto gain path selection (below)
- The high-gain and low-gain path can be easily cross-calibrated (as you can force the path selection).

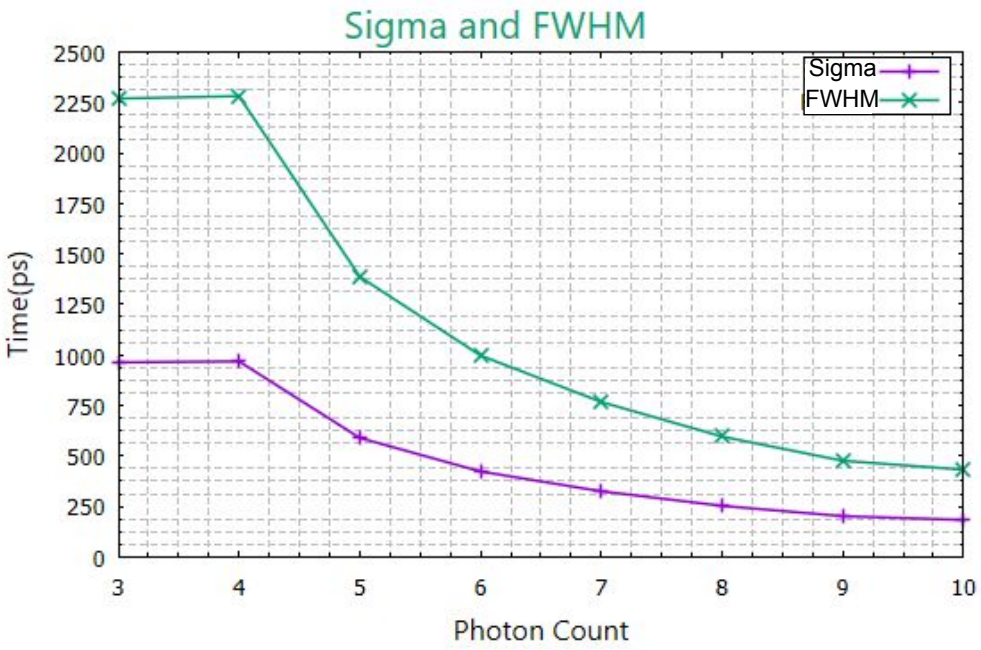
Performance: ADC data readout Linearity & Error

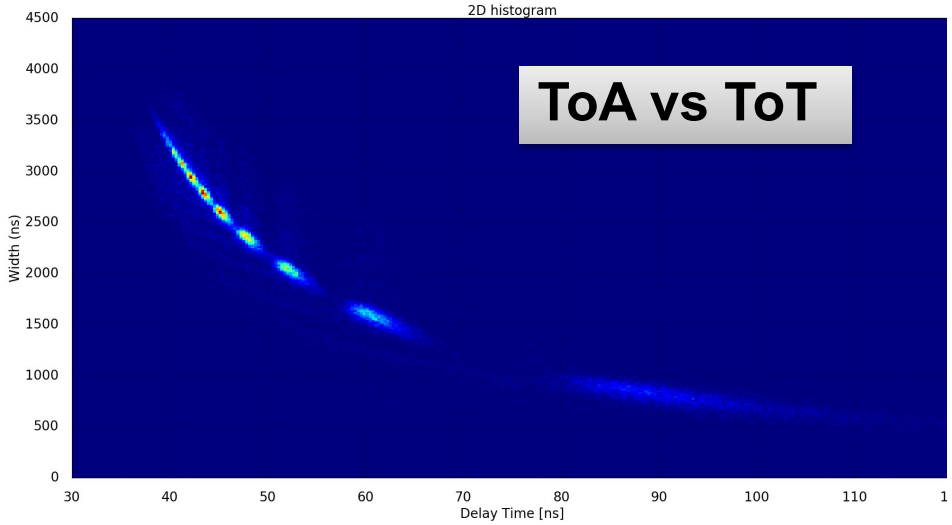


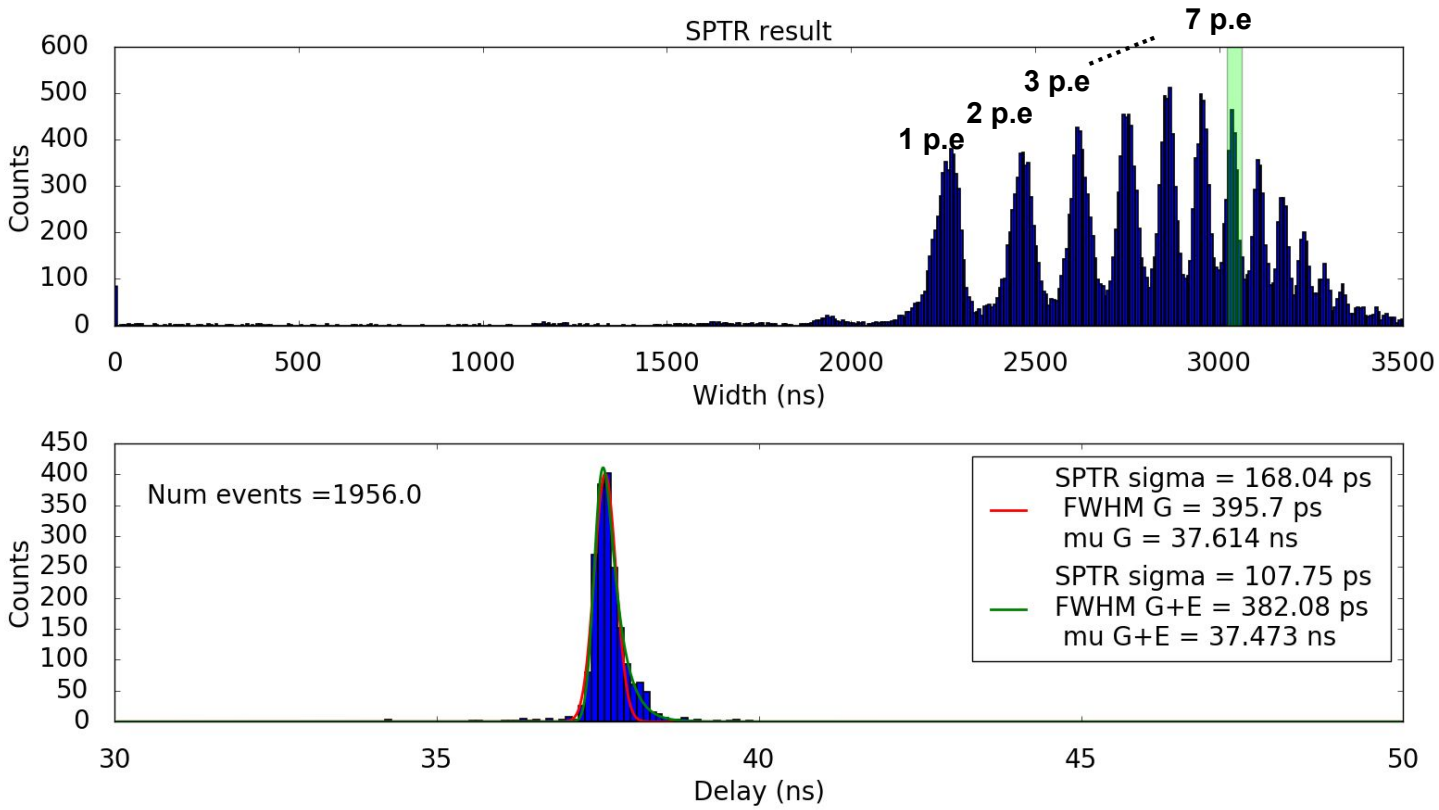


- The linearity error is **below 3%** over the whole dynamic range for HG & LG paths.
- The ASIC provides a large dynamic range from 3800 pe to 0.1 pe as large as 15 bits
- The output saturates at 750 uA of input current for HG path and 12 mA input current for LG path.

Performance: SPTR measurements (S13360-1350CS)



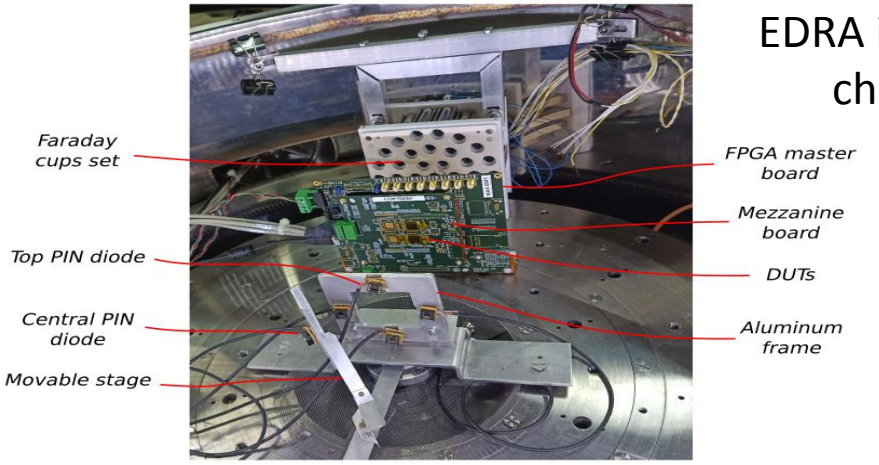




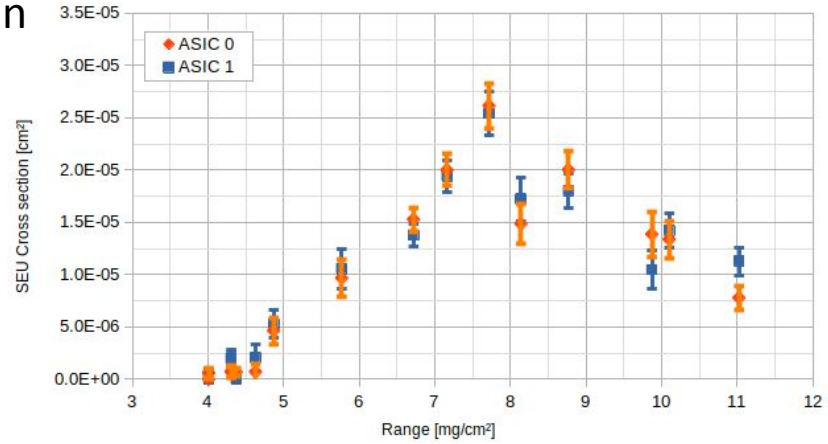
- Sensor: **HPK S13360-1350CS**
  - 10-PTR HERD : 168 ps rms

BETA status

- The 2 first version of 16ch BETA ASIC (BETA16R1 and R2) have been extensively used in beam tests:
  - Collaboration with IFAE, INFN/Bari and University of Geneva
- The BETA16R2 ASIC has been prequalified for radiation
  - Total Ionizing Dose (TID): No degradation after 100 krads
    - Test performed at Nayade facility in CIEMAT
  - Limited Single Events (SEE) qualification: O @ 60 MeV
    - No Single Event Latchup (SEL) detected
    - Some sensitivity of the I2C interface to Single Event Transients SETs → corrected for BETA16R3 and BETA64R1
    - Tests at the EDRA irradiation chamber at Tandar Accelerator, Buenos Aires, Argentina
      - Many thanks to F. Izraelevitch and M. Alurralde (UNSAM-CONICET)



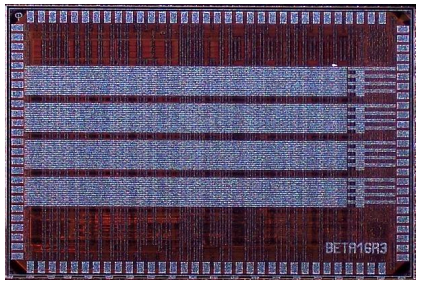
EDRA irradiation chamber



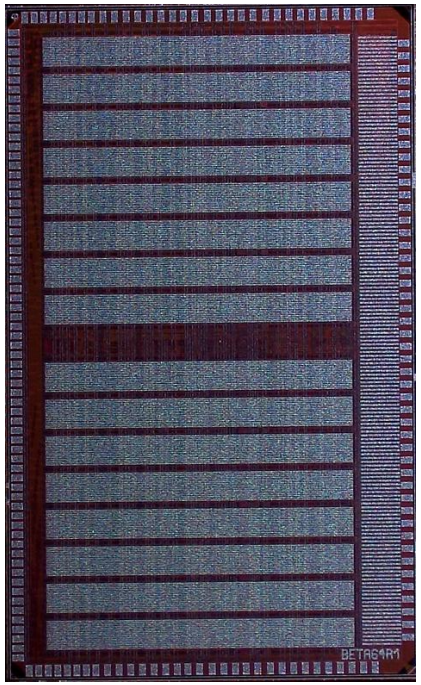
Cross section plots of the irradiated ASICs

BETA status

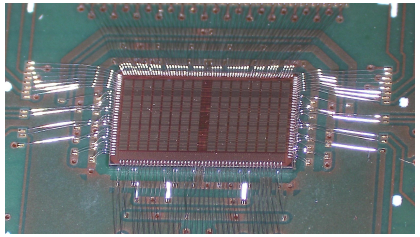
- Two flavours have been produced:
  - 16 ch for trigger/VETO detectors
    - 16 trigger outputs
      - Low Level or Path Selection discriminators
    - Serial ADC output
      - Serial input for daisy chain
    - < 1.5 mW/ch (timing optimized)
    - QFN88 package
  - 64 ch for fiber tracker and large detectors
    - Single trigger output
      - Different combinatorial logic configurations
        - OR, multiplicity, predefined patterns
    - Serial ADC output
      - Serial input for daisy chain
    - < 1 mW/ch
    - Wire-bonded
      - BGA package under consideration



BETA16R3
16 ch
130 nm CMOS
9 mm^2



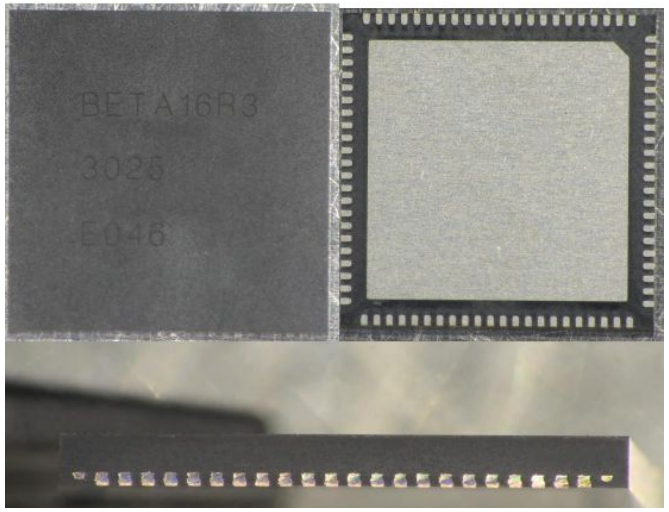
BETA64R1
64 ch
130 nm CMOS
24 mm^2



More information on: https://icc-ub.gitlab.io/instrumentation/documentation/index.html?page=beta

BETA status

- BETA16r3 QFN88 10x10 mm:
  - Some units packaged for space applications validation
    - Custom leadframe to reduce inductance due to WB
    - ~ 50 units received on week 43
    - TID & SEU tests expected at beginning 2026
      - ESA will indicate the facilities for radiation test (TBD)



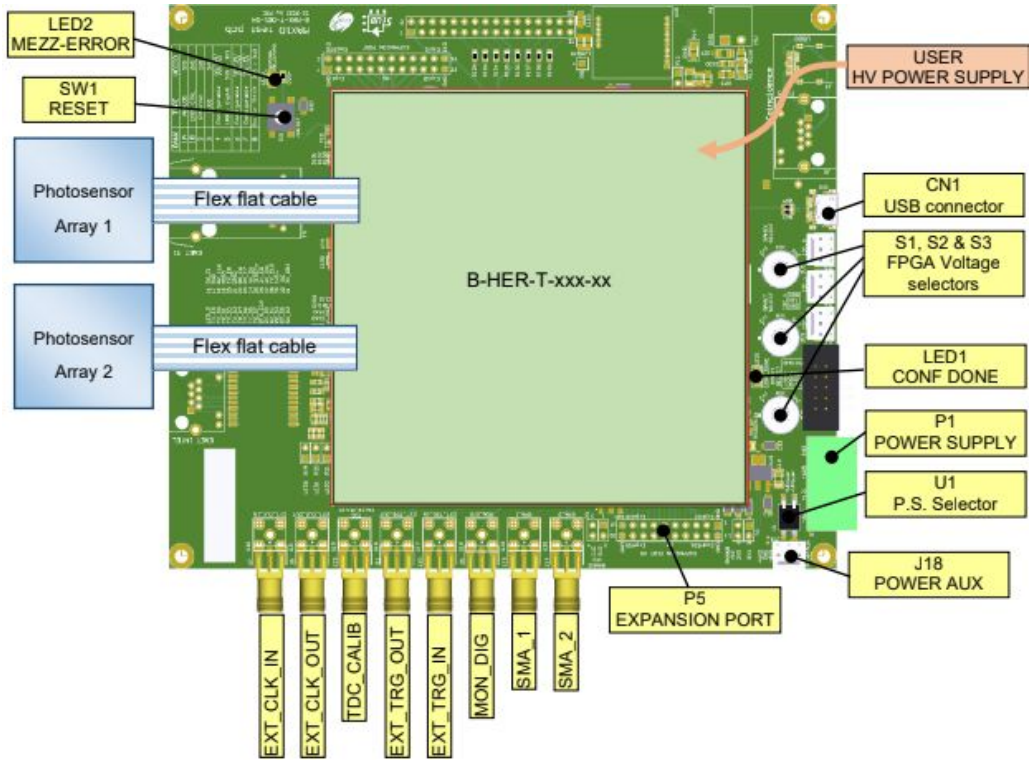
  - 400 units with standard QFN88 leadframe
    - 68 received on week 41 (beginning october)
      - QC test done on week 44
      - 80% yield as expected
    - 10 expected in 1 or 2 weeks
    - 300 expected before end of 2025

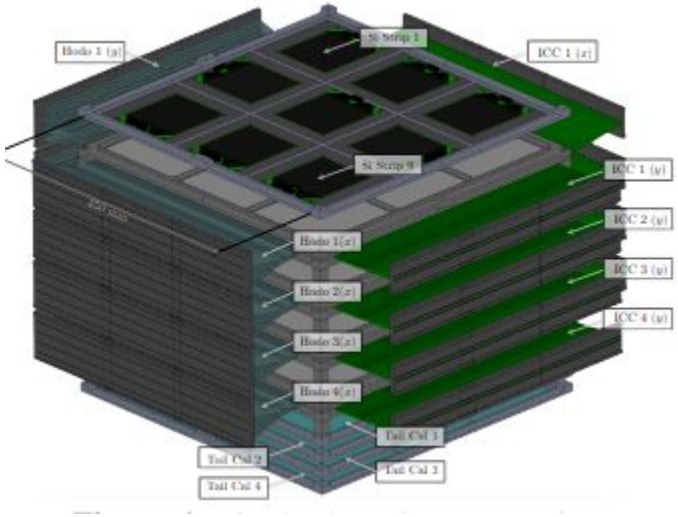
QFN88 10x10 mm TOP VIEW

Applications: Antarctic Demonstrator for APT (ADAPT).

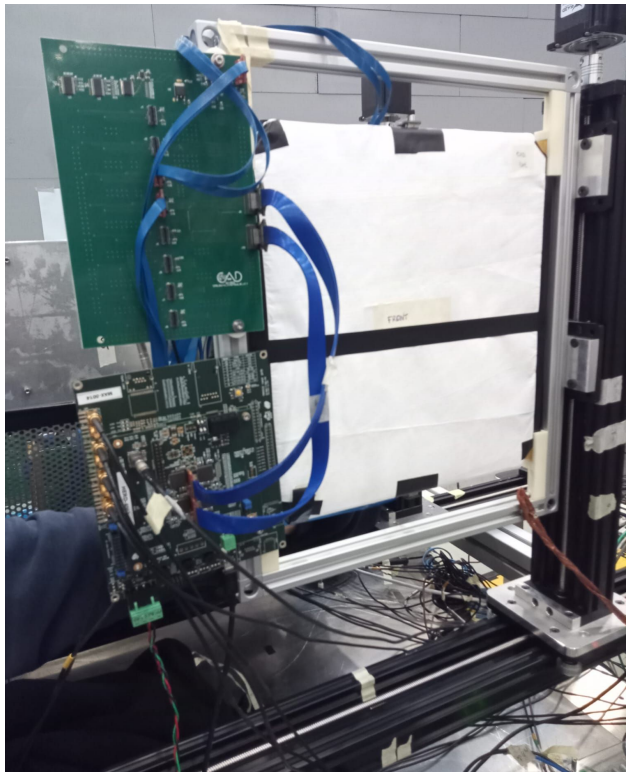
BETA ASIC will equip the anti-coincidence detector (led by INFN Bari):

- - Large plastic-scintillator detectors readout with SiPMs
- - 1st prototype under characterization





https://doi.org/10.22323/1.395.0655

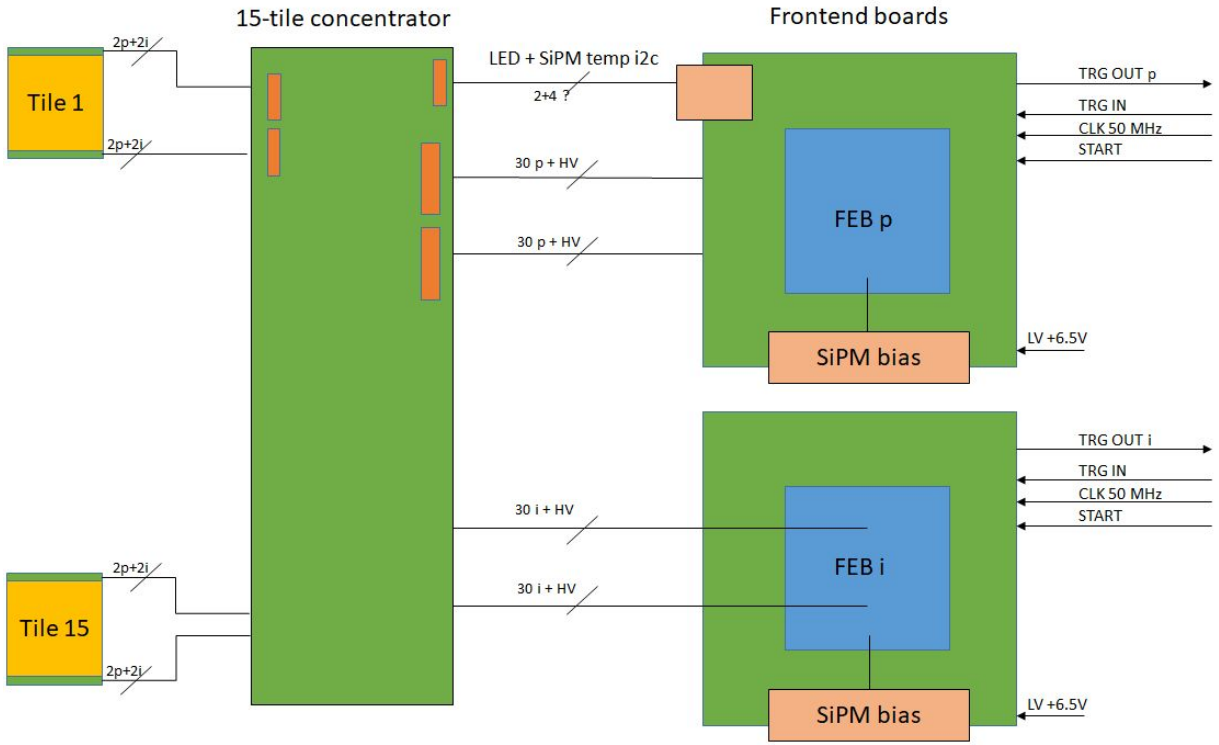


Applications: Antarctic Demonstrator for APT (ADAPT).

FPGA + BETA16r3 ASIC x4 + Piggyback ICCUB

- Up to 64 Ch readout each FEB
- FEB could provide SiPM bias

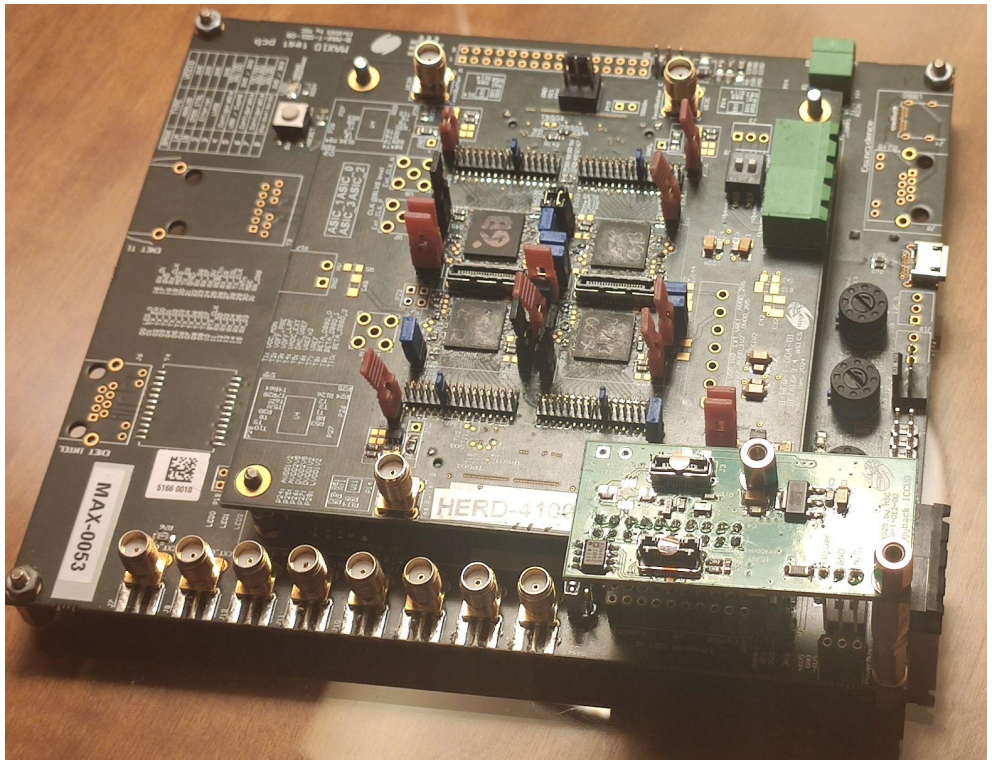
- FEB powered @ ∓6.5V
- FEB output by USB connection
- Piggyback ICCUB:
  - LVDS LED pulser
  - I2C concentrator
  - CLK & TrgIN from WUST piggyback
  - TrgOUT to WUST piggyback



Applications: Antarctic Demonstrator for APT (ADAPT).

FPGA + BETA16r3 ASIC x4 + Piggyback ICCUB

- SiPM Input by 2x LSHM 40 pin connector
  - Includes HV if needed
- FEB Data output by micro-USB cabling
  - USB-C connector footprint available
- BETA board populated with output buffer for debug
  - One SMA connector per BETA asic
- ICCUB Piggyback boar located as a mezzanine
  - 2 fixing holes match with FPGA board
  - Needs long THT pins to connect with FPGA board
  - No additional area needed
  - HLCD comes from the Z axis

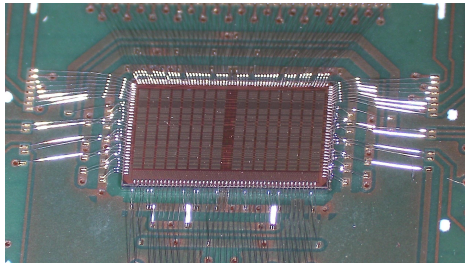


Summary

- Single photon resolution: SNR >5 for 10 µm microcells (> 10 for 50 µm)
- High dynamic range: >15 bits (no saturation for > 3800 firing cells)
- Tuneability: preamp gain and feedback resistor, shaping time, etc
- Trigger discriminator: time resolution < 200 ps rms (100 ps rms TBC)
- BETA is a versatile ASIC for low power and low-rate applications:
  - Fiber trackers, calorimeters, trigger/VETO, etc
  - Adopted for several missions
  - Considered for other aerospace and ground applications

Thanks a lot for your attention !!!

Questions ?



Many thanks to our collaborators in IFAE, INFN/Bari, University of Geneva and CONICET!

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IEEC Institut d'Estudis Espacials de Catalunya

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