

HDSoc

(High Density Digitizer System on Chip)

Status

Nov. 4, 2025

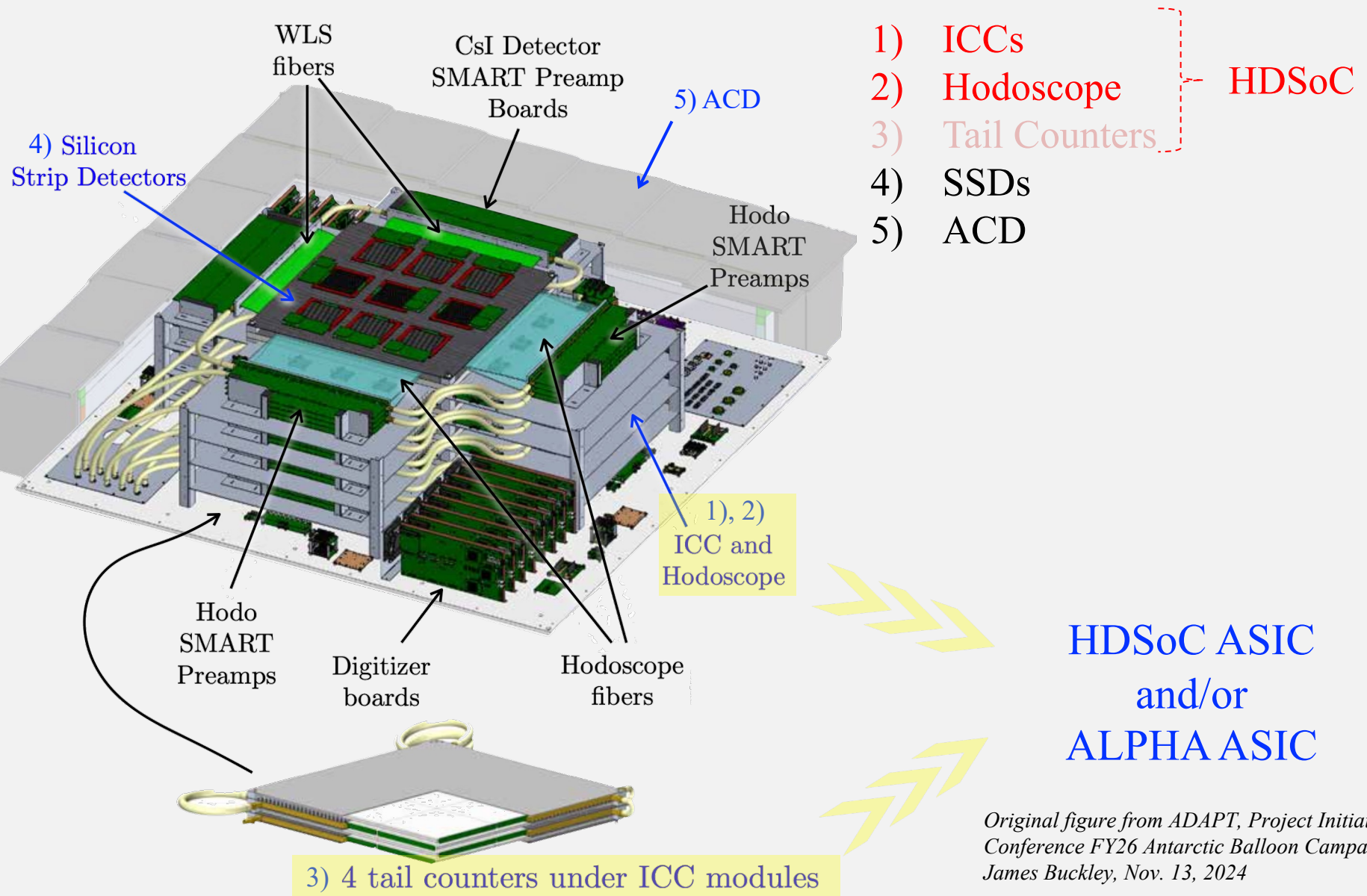
Aera Jung¹, Ben Rotter², Luca Macchiarulo², Marcus Luck²,
Christopher Chock², Isar Mostafanezhad², Jennifer Ott³,
Boris Murmann^{3,1}

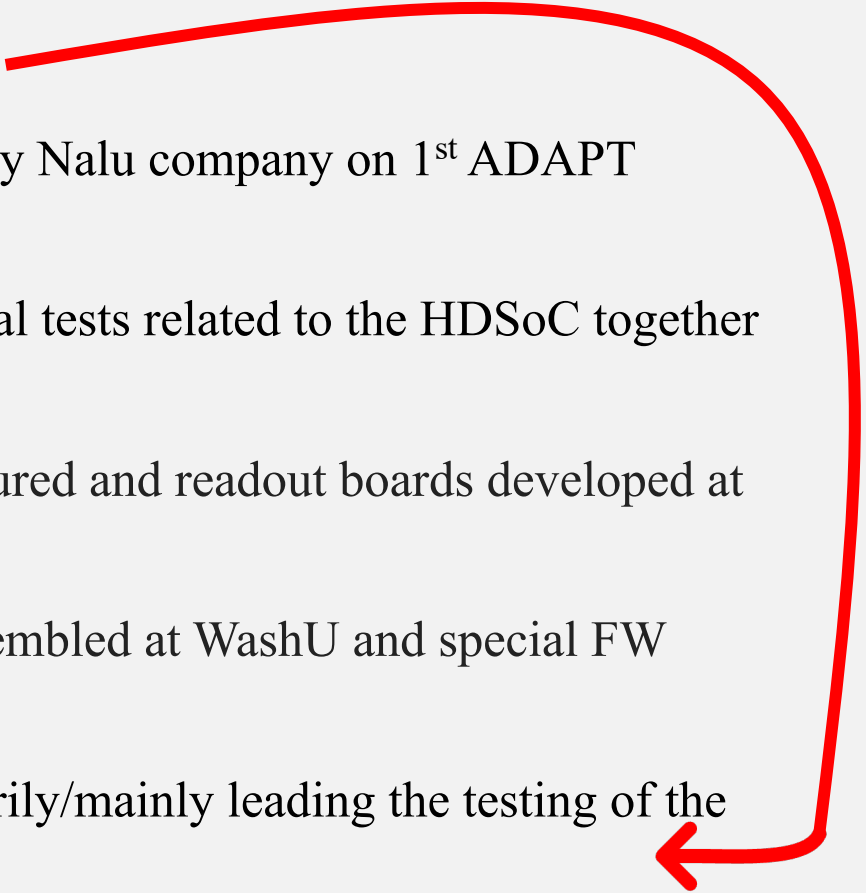
¹ Department of Physics and Astronomy, University of Hawai'i at Mānoa, Honolulu, HI 96822, USA

² Nalu Scientific, LLC, Honolulu, HI, 96822, USA

³ Department of Electrical and Computer Engineering, University of Hawai'i at Mānoa, Honolulu, HI 96822, USA

• Detectors

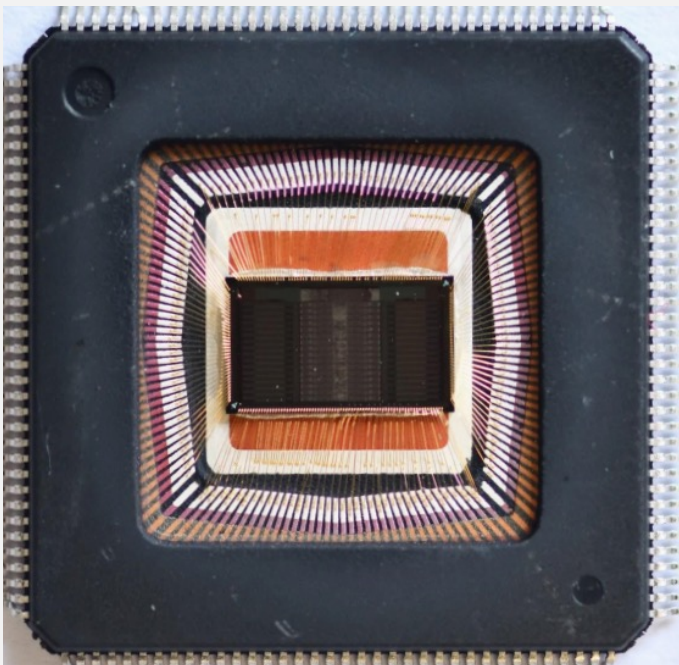


- Mar. 2023: ALPHA v2 was submitted.
 - May 2023: 40 ALPHA v2 ASICs arrived at UH from company.
 - July 2023: Gary Varner, professor of physics and astronomy at the UH and built and designed ALPHA, passed away on July 14, 2023.
 - Oct. 2023: The ALPHA v2 ASIC test board modified in WashU has arrived Oct. 19, 2023.
 - Oct. 23, 2023 ~ now: ALPHA v2 debugging.
 - Nov. 2023: Boris proposed the HDSoc made by Nalu company on 1st ADAPT collaboration meeting.
 - Dec. 2023 ~ Dec. 2025: Boris' group ran several tests related to the HDSoc together with Nalu company and nearly complete.
 - May 2024 ~ Mar. 2025: 75 HDSoc chips procured and readout boards developed at WashU.
 - Jan. 2025 ~ now: readout boards fabbed & assembled at WashU and special FW developed at WashU with help from Nalu.
 - Jan. 16, 2025 ~ now: Jennifer's group is primarily/mainly leading the testing of the ALPHA and also includes HDSoc.
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- HDSoc (High Density Digitizer System on Chip) description

Technology	CMOS 250 nm
Voltage Supply	2.5V
Input voltage range	0.5-2.2V
Power consumption	20-47mW/ch
Package	QFP 144-pin package (22 mm side)
Sampling Rate	1 – 1.8 GSPS

- HDSoc ver. 1 package



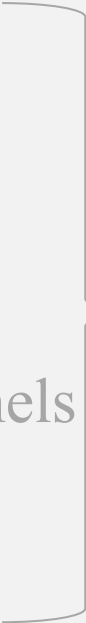
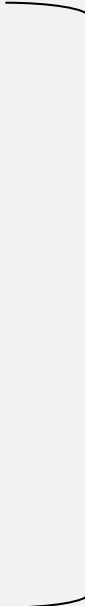
- Specifications:

- DLL (Delay-Locked Loop) based timing for the sampling
- Dynamic range: large dynamic range with 12 bits resolution
- Noise: low noise
- Power consumption: low power consumption
- Sampling frequency: ~250MHz up to ~1.8GHz
- Readout channels: 32ch (for ver. 1), 64ch (for ver. 2)

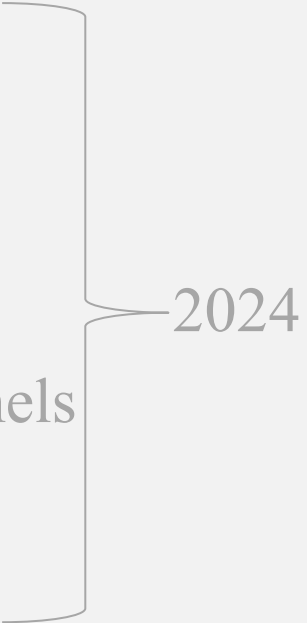
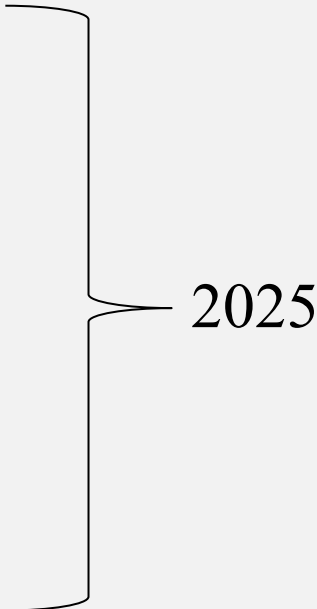
- Large number of adjustable parameters

▼ analog_registers	trigger_threshold_4	▼ digital_registers	pclk	▼ control_registers
bufbias_bias_0	trigger_threshold_5	chanmask0	pclkwidth	1v2_en
bufbias_bias_1	trigger_threshold_6	chanmask1	pedram_addr	2v5_en
bufbias_bias_10	trigger_threshold_7	chanmask2	pedram_data	3v3_i2c_en
bufbias_bias_11	trigger_threshold_8	chanmask3	pg_2v5	analog_debug_disable
bufbias_bias_12	trigger_threshold_9	convertresetwait	reg_data0	asic_clk_locked
bufbias_bias_13	ts_left	dig_to_an	reg_data1	auto_numwinds_en
bufbias_bias_14	ts_right	idconfig	regclr	ch_en15_0
bufbias_bias_15	tssel_left	readoutchannels	rx_en	ch_en31_16
bufbias_bias_16	tssel_right	readoutlookback	sel	clk1v8_en
bufbias_bias_17	tsgn_left	readoutwindows	ser_rx_crc_en	clk2v5_en
bufbias_bias_18	tsgn_right	readoutwindows	ser_rx_div	clk_i2c_sel
bufbias_bias_19	vadjn_left	regclr_bk	ser_rx_eof_en	clk_intr_n
bufbias_bias_2	vadjn_right	regclr_chan	ser_rx_neg_pol	clk_lol_n
bufbias_bias_20	vadjp_left	reglatchperiod_bk	ser_tx_clk_locked	clk_oeb
bufbias_bias_21	vadjp_right	reglatchperiod_chan	ser_tx_neg_pol	clk_reset
bufbias_bias_22	vanbuf_left	regloadperiod_bk	stopacq	clk_sync
bufbias_bias_23	vanbuf_right	regloadperiod_chan	sysrst	debug_addr
bufbias_bias_24	vapbuf_left	regmisc	t_user	debug_data
bufbias_bias_25	vapbuf_right	regspeed	timeout15_0	dhcp_addr15_0
bufbias_bias_26	wrstrb1_le_left	regwaitaddr	timeout31_16	eth_addr_sel
bufbias_bias_27	wrstrb1_le_right	regwaitread	tx_en	eth_ar_en
bufbias_bias_28	wrstrb1_te_left	scal0	tx_mode	eth_dest_addr15_0
bufbias_bias_29	wrstrb1_te_right	scal1	version	eth_dest_addr31_16
bufbias_bias_3	wrstrb2_le_left	scal10	wave_fifo_rst	eth_dest_port
bufbias_bias_30	wrstrb2_le_right	scal11	write_address	eth_dhcp_en
bufbias_bias_31	wrstrb2_te_left	scal12		eth_port_sel
bufbias_bias_4	wrstrb2_te_right			
⋮	⋮	⋮	⋮	⋮

UH's contributions

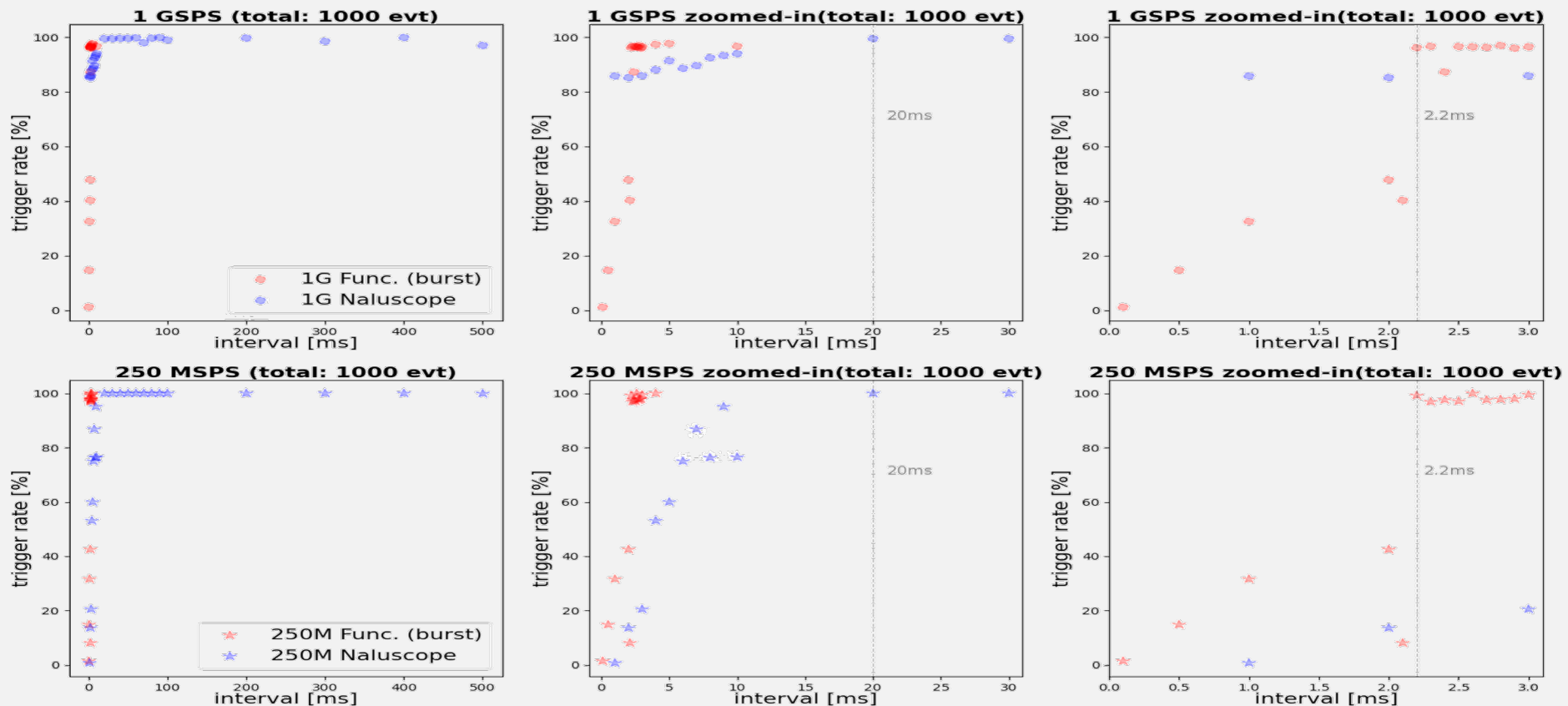
- Reducing sampling frequency to 250MHz
 - ~33% power savings
 - Residual noise rms error compared across 3 different channels
 - Single photo-electron measurement
- 
- 2024
- Serial interface data transfer rate
 - Resolution
 - Timing calibration
 - WashU's mother board + HDSoC daughter boards
- 
- 2025

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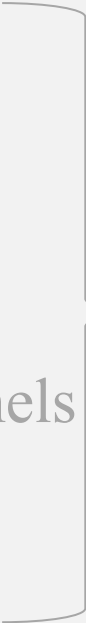
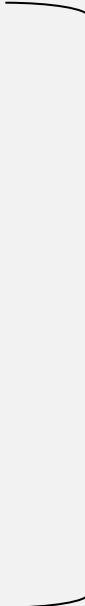
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Serial interface data transfer rate

- Parallel interface (default) → Serial interface between HDSoc and FPGA
- External trigger: Naluscope (~ 20 ms) for both 1 GSPS and 250 MSPS
Func. generator (~ 2.2 ms) for both 1 GSPS and 250 MSPS

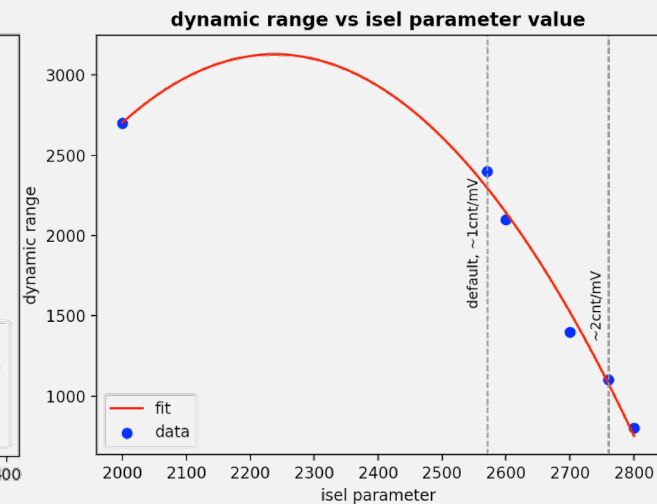
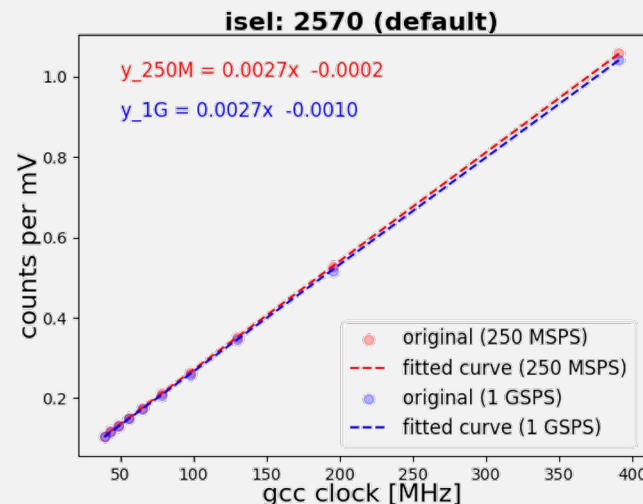
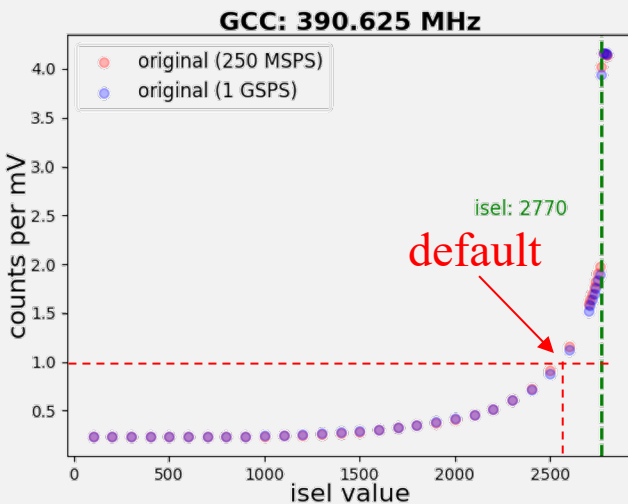


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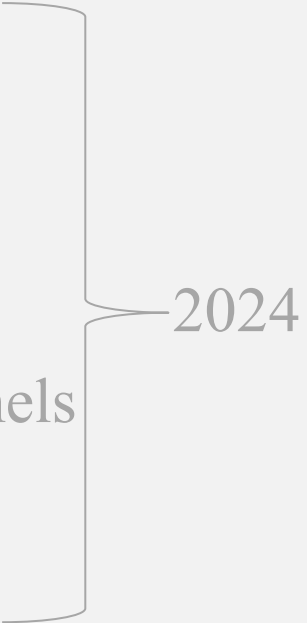
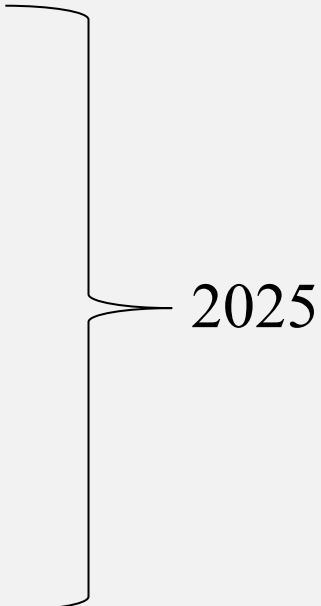
Resolution

- High resolution [cnt/mV]: higher isel value and higher GCC clock speed
- High isel value: reduction in dynamic range



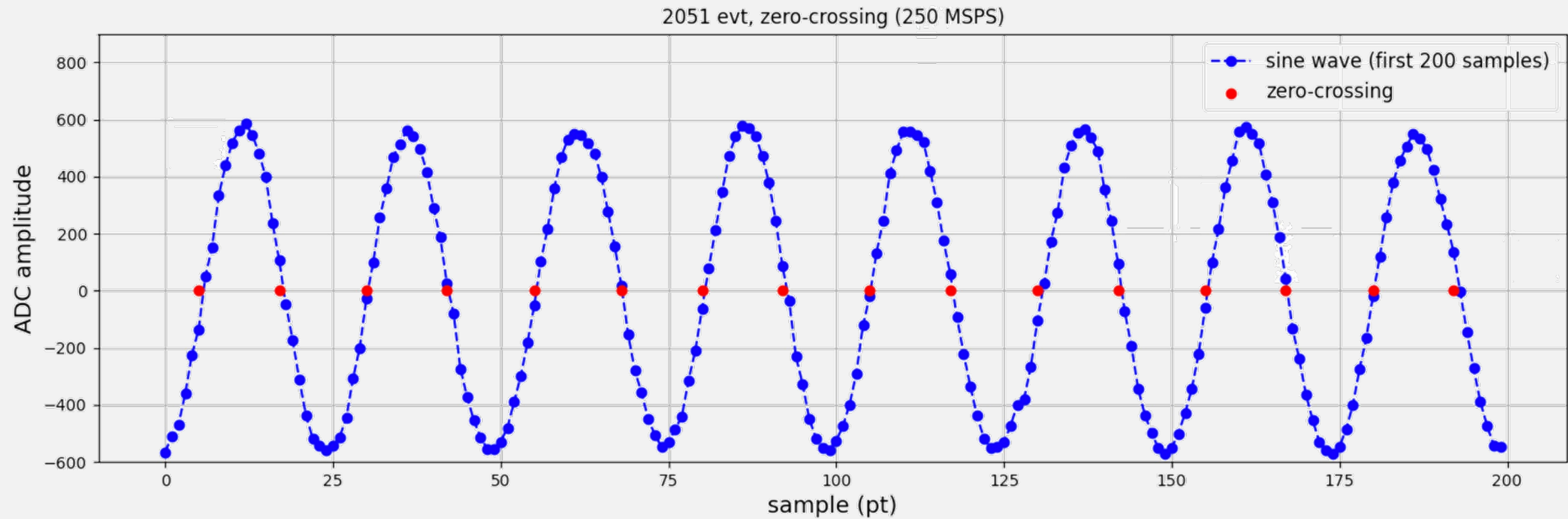
- Optimized value: 1 count / mV at 2570 (isel) and 390.625 MHz (GCC)
for both 1 GSPS and 250 MSPS

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Timing resolution using zero-crossing

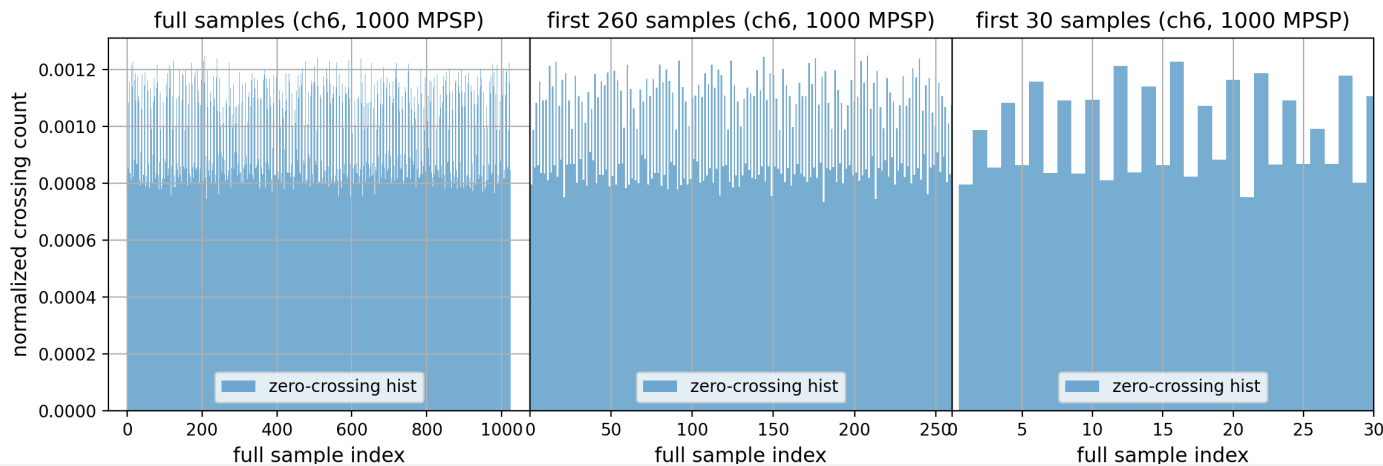
- Zero-crossing example



- Input: 2V, 11.1234 MHz sine wave to 3ch splitter

Results of timing resolution using zero-crossing

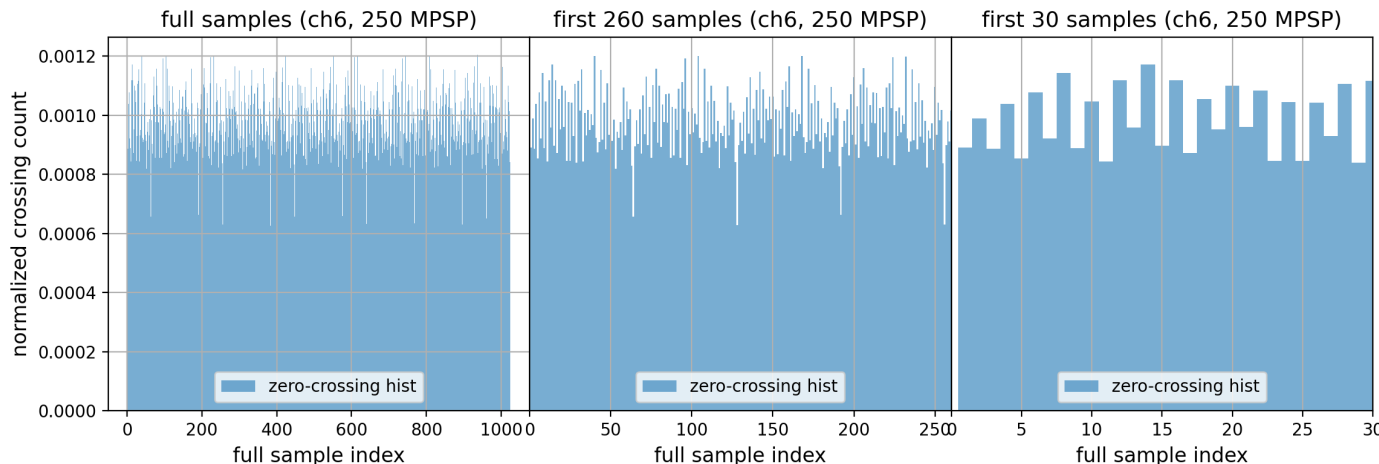
• 1 GSPS



STD: 0.1593731331416353

→ ~159 ps

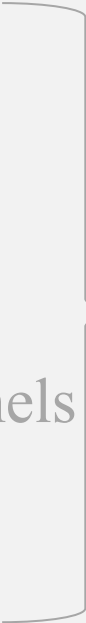
• 250 MSPS



STD: 0.10772778724178121

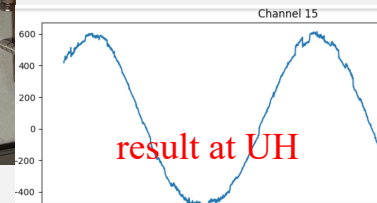
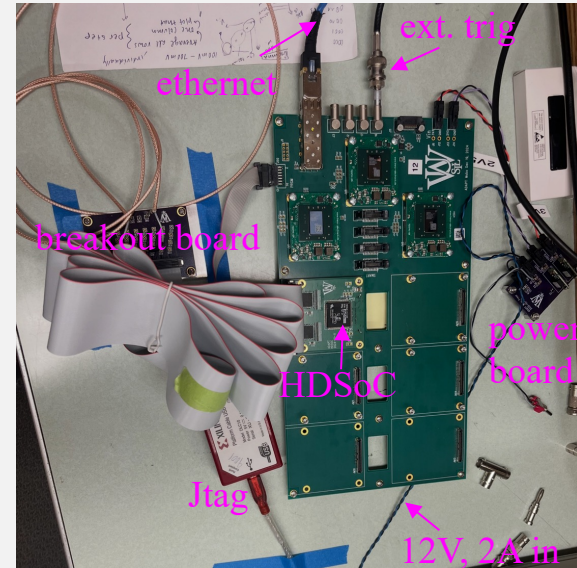
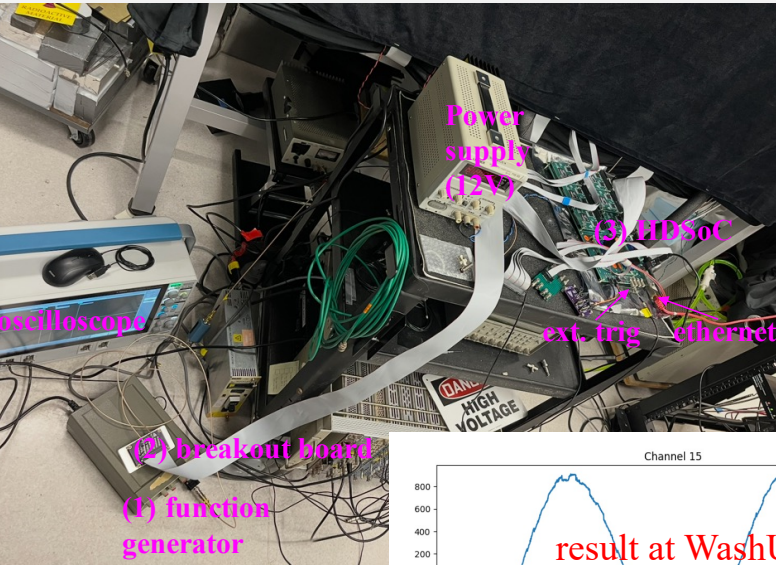
→ ~107 ps

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01 Setup duplication at UH

- Aera visited WashU on Oct. 16-17, 2025, and we have duplicated the WashU setup in UH.
 - WashU setup
 - UH setup



- There were several issues along the way, but thanks to Marion, we now have a working setup at UH.
- Contact people

Ashtar Aggelopoulos	Undergraduate + master course
Guanchen Wu	Undergraduate + master course
Lawrence Zheng	3 rd year undergraduate

← Lawrence helped me the most.