HDSoC
(**H**igh **D**ensity Digitizer **S**ystem **o**n **C**hip)
Status

Nov. 4, 2025

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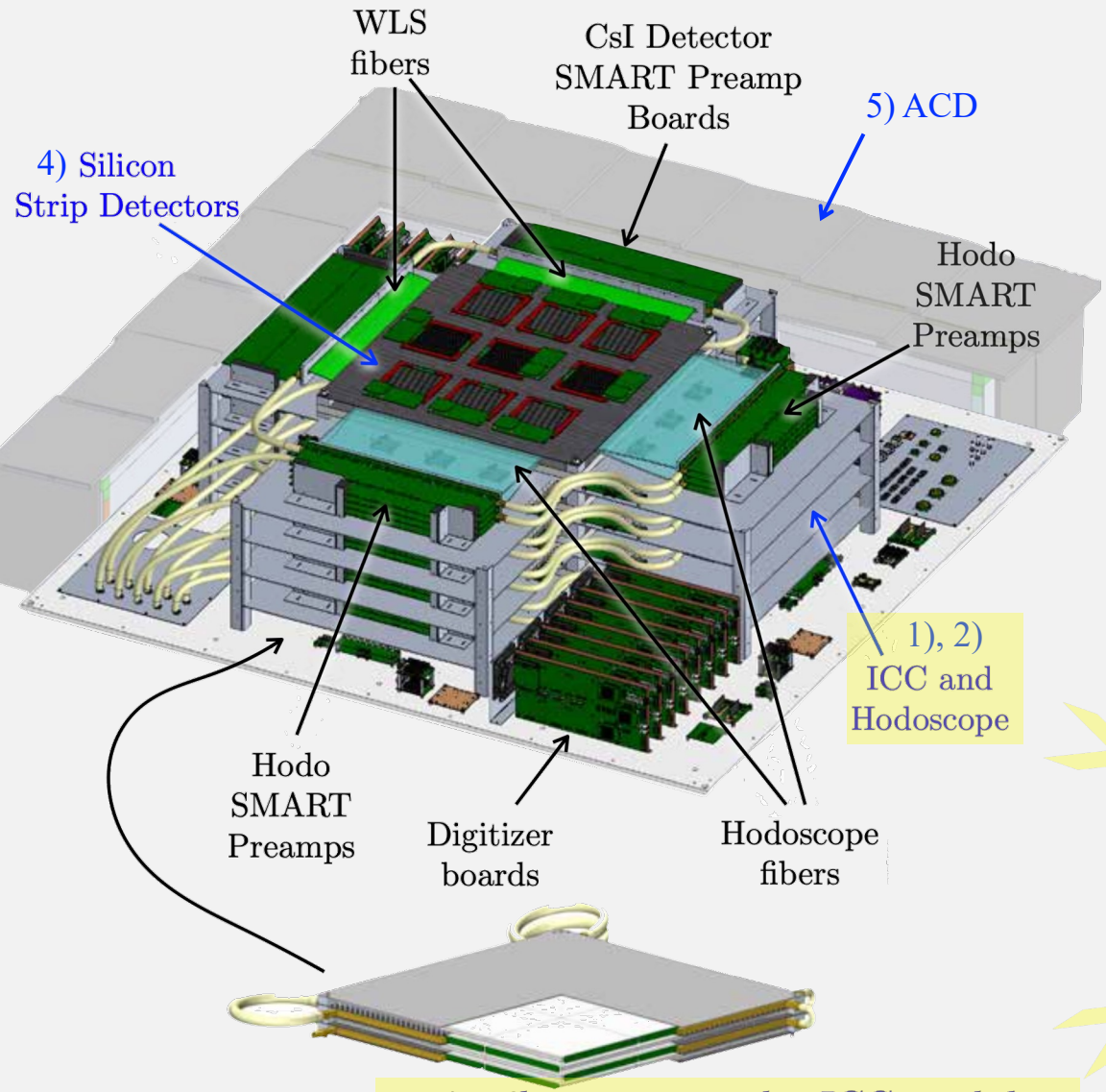
01 ADAPT payload

- Detectors



1) ICCs
2) Hodoscope
3) Tail Counters
4) SSDs
5) ACD

HDSoC

HDSoC ASIC and/or ALPHA ASIC

Original figure from ADAPT, Project Initiation Conference FY26 Antarctic Balloon Campaign, James Buckley, Nov. 13, 2024

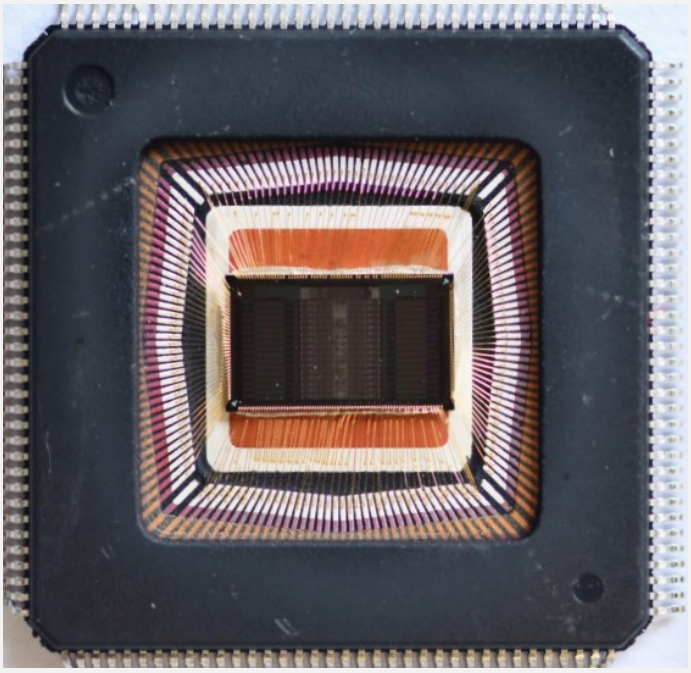
01 History

- Mar. 2023: ALPHA v2 was submitted.
- May 2023: 40 ALPHA v2 ASICs arrived at UH from company.
- July 2023: Gary Varner, professor of physics and astronomy at the UH and built and designed ALPHA, passed away on July 14, 2023.
- Oct. 2023: The ALPHA v2 ASIC test board modified in WashU has arrived Oct. 19, 2023.
- Oct. 23, 2023 ~ now: ALPHA v2 debugging.
- Nov. 2023: Boris proposed the HDSoC made by Nalu company on 1st ADAPT collaboration meeting.
- Dec. 2023 ~ Dec. 2025: Boris' group ran several tests related to the HDSoC together with Nalu company and nearly complete.
- May 2024 ~ Mar. 2025: 75 HDSoC chips procured and readout boards developed at WashU.
- Jan. 2025 ~ now: readout boards fabbed & assembled at WashU and special FW developed at WashU with help from Nalu.
- Jan. 16, 2025 ~ now: Jennifer's group is primarily/mainly leading the testing of the ALPHA and also includes HDSoC.

- HDSoC (**H**igh **D**ensity Digitizer **S**ystem **o**n **C**hip) description

Technology	CMOS 250 nm
Voltage Supply	2.5V
Input voltage range	0.5-2.2V
Power consumption	20-47mW/ch
Package	QFP 144-pin package (22 mm side)
Sampling Rate	1 – 1.8 GSPS

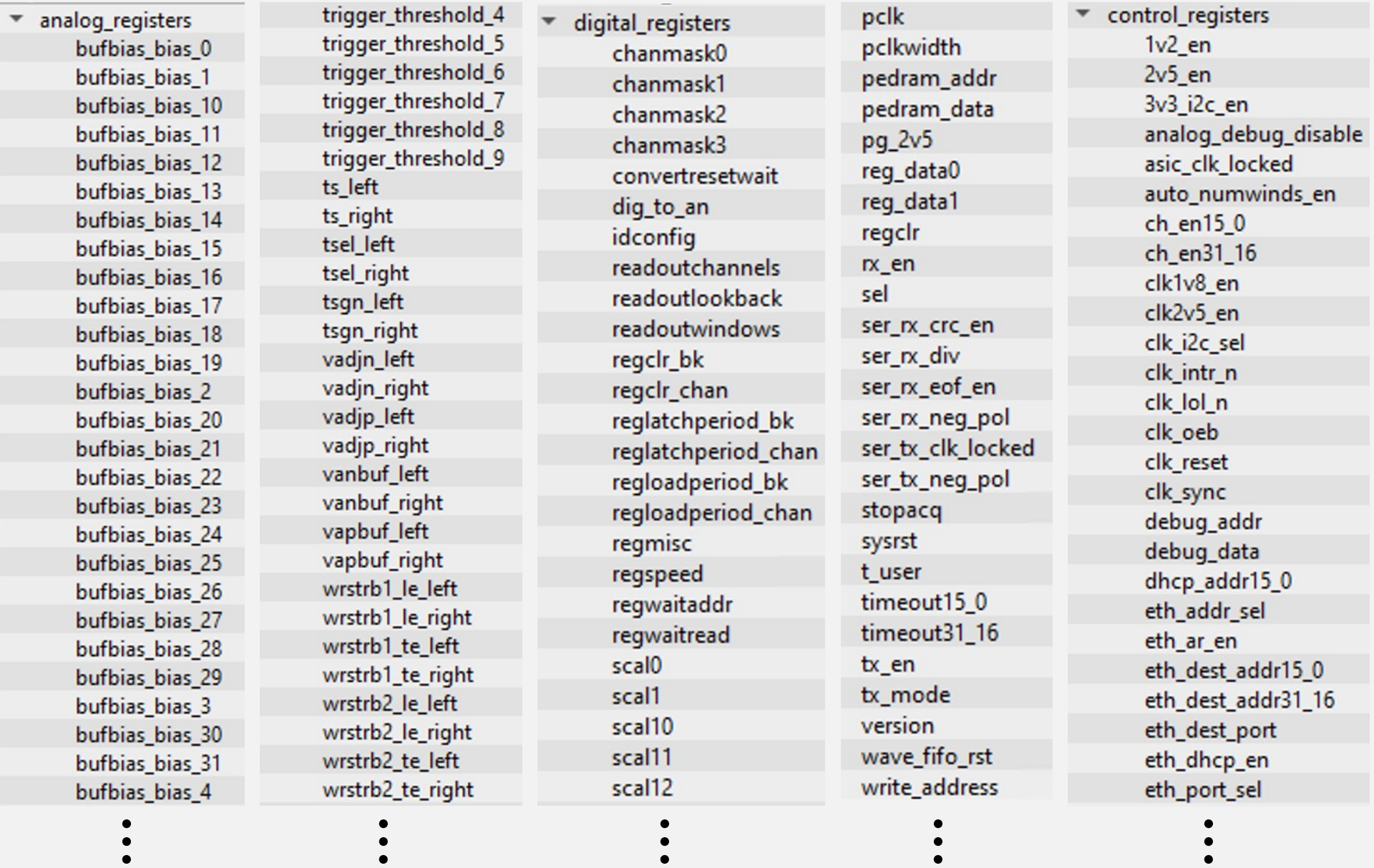
- HDSoC ver. 1 package



- Specifications:
  - DLL (Delay-Locked Loop) based timing for the sampling
  - Dynamic range: large dynamic range with 12 bits resolution
  - Noise: low noise
  - Power consumption: low power consumption
  - Sampling frequency: ~250MHz up to ~1.8GHz
  - Readout channels: 32ch (for ver. 1), 64ch (for ver. 2)

01 HDSoC ASIC

- Large number of adjustable parameters



01 UH's contributions

- Reducing sampling frequency to 250MHz
- ~33% power savings
- Residual noise rms error compared across 3 different channels
- Single photo-electron measurement

2024

- Serial interface data transfer rate
- Resolution
- Timing calibration
- WashU's mother board + HDSoC daughter boards

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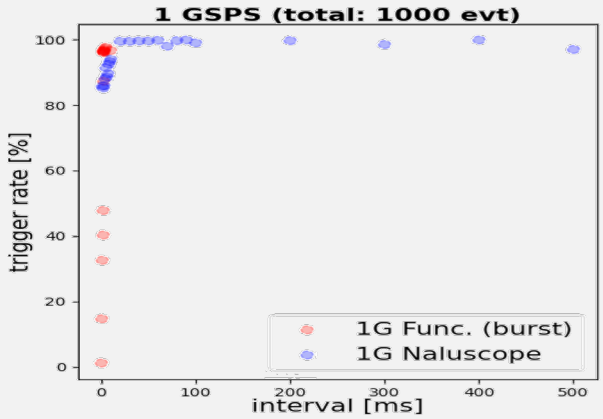
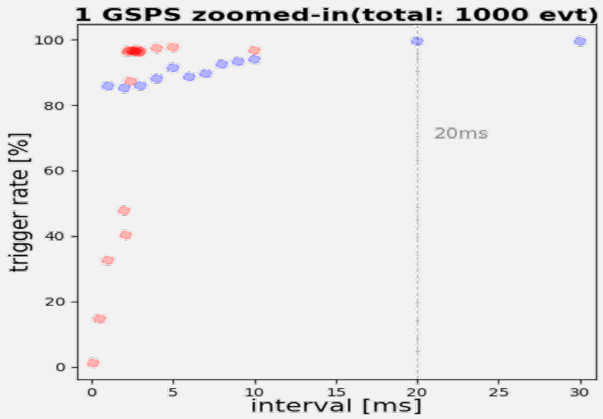
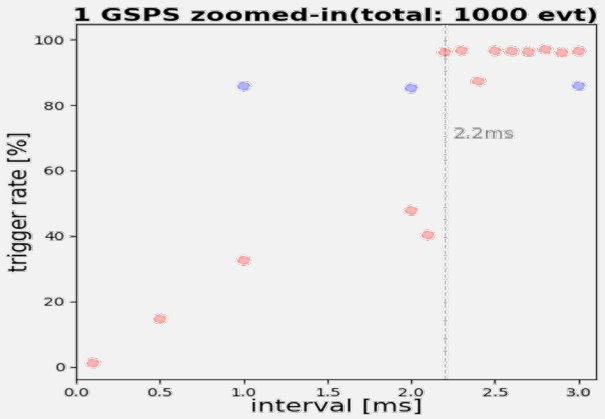
01 Serial interface data transfer rate

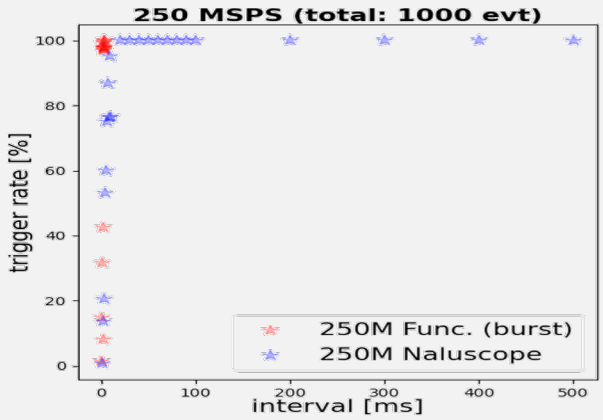
- Parallel interface (default) → Serial interface between HDSoC and FPGA

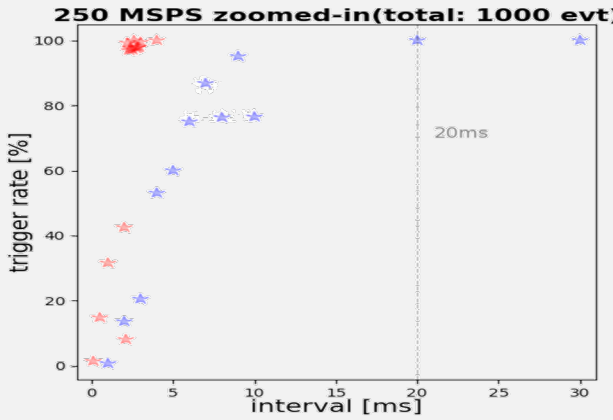
- External trigger: Naluscope (~ 20 ms) for both 1 GSPS and 250 MSPS
  Func. generator (~ 2.2 ms) for both 1 GSPS and 250 MSPS

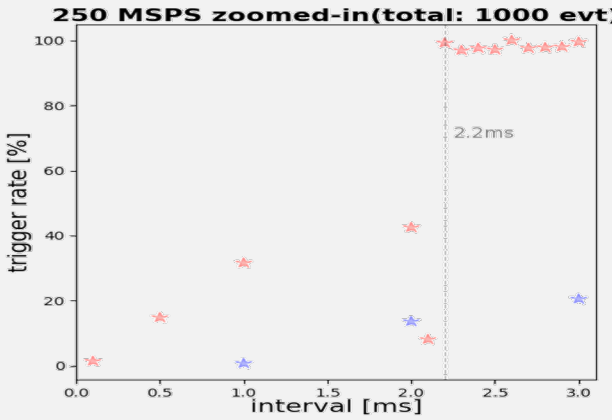












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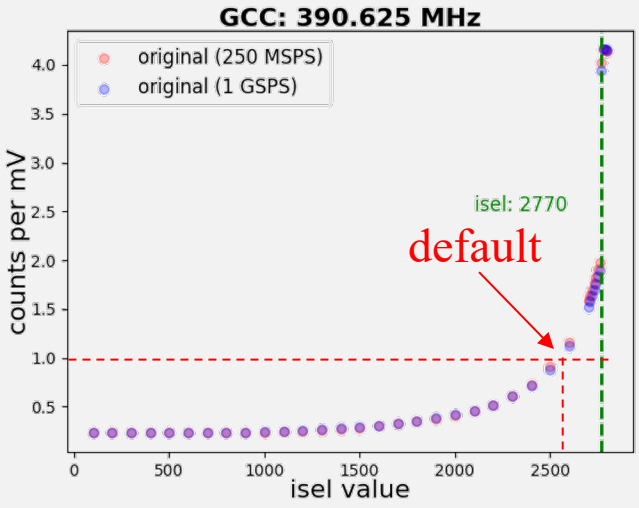
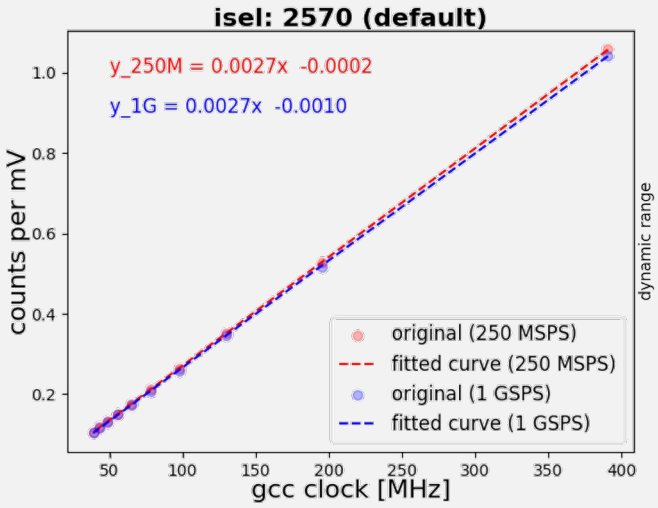
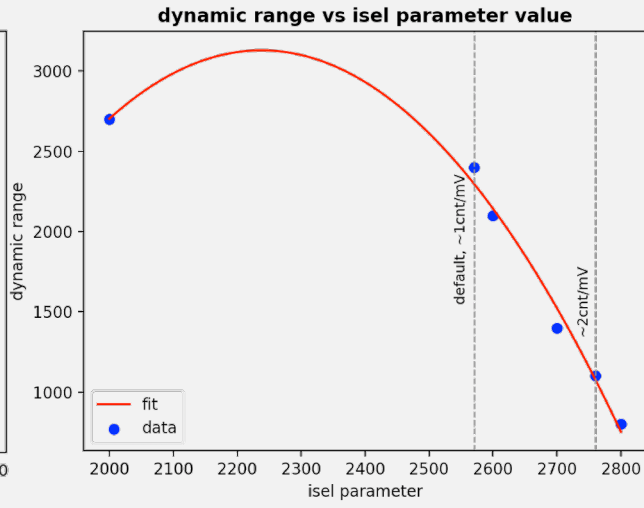
01 Resolution

- High resolution [cnt/mV]: higher isel value and higher GCC clock speed

- High isel value: reduction in dynamic range







- Optimized value: 1 count / mV at 2570 (isel) and 390.625 MHz (GCC) for both 1 GSPS and 250 MSPS

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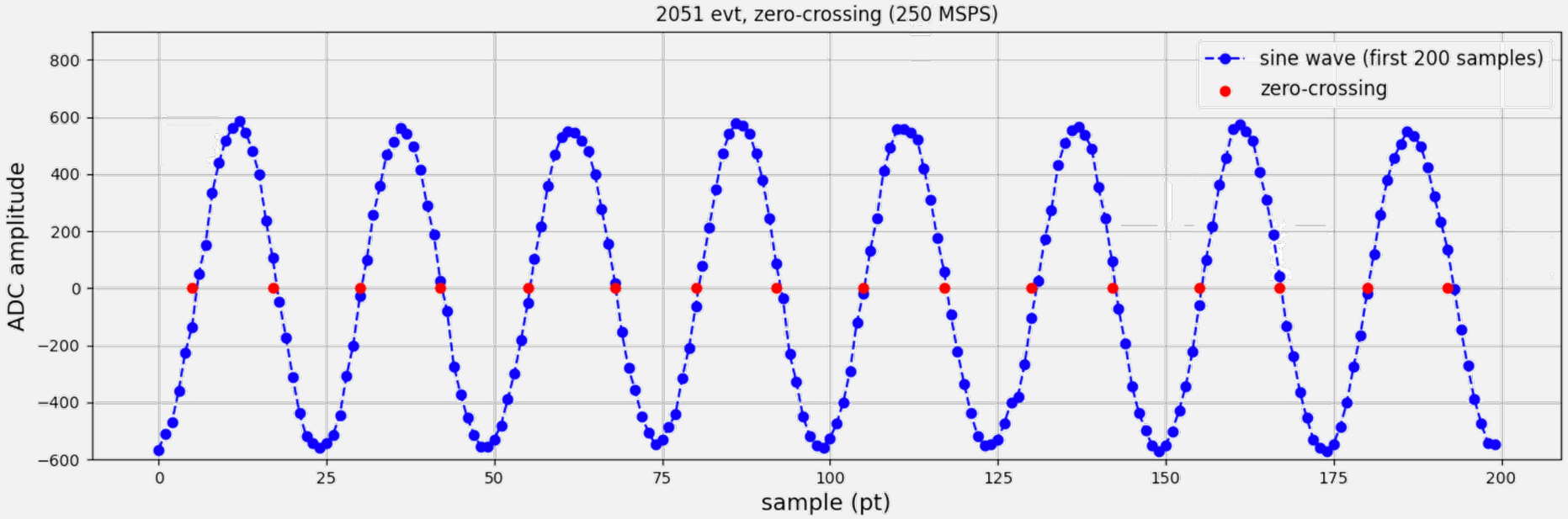
01 Timing resolution using zero-crossing

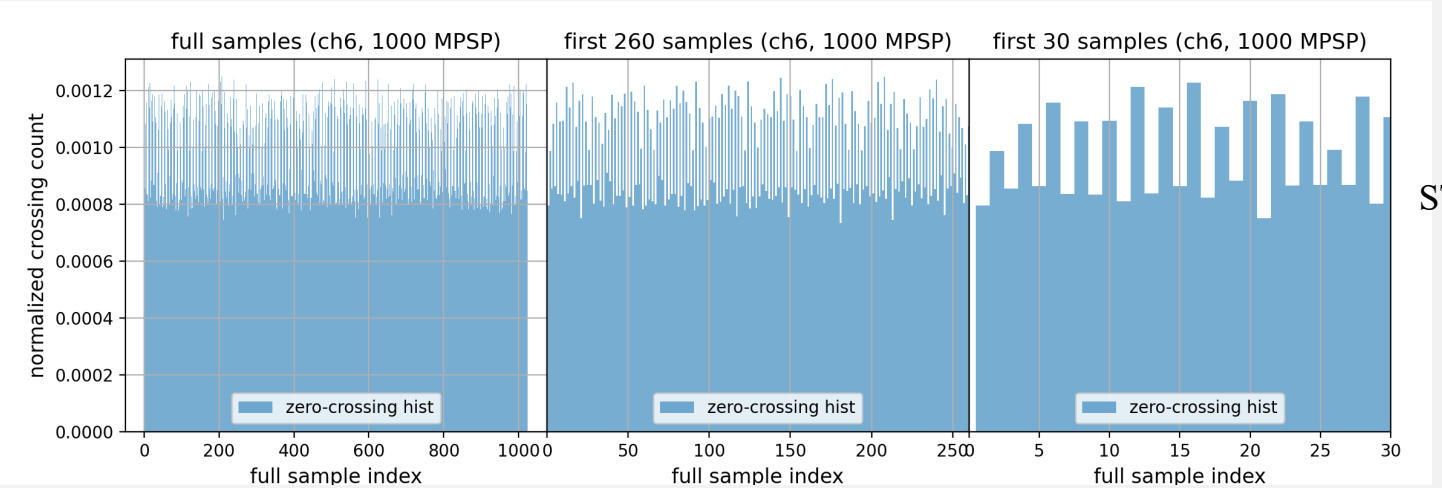
- Zero-crossing example



- Input: 2V, 11.1234 MHz sine wave to 3ch splitter

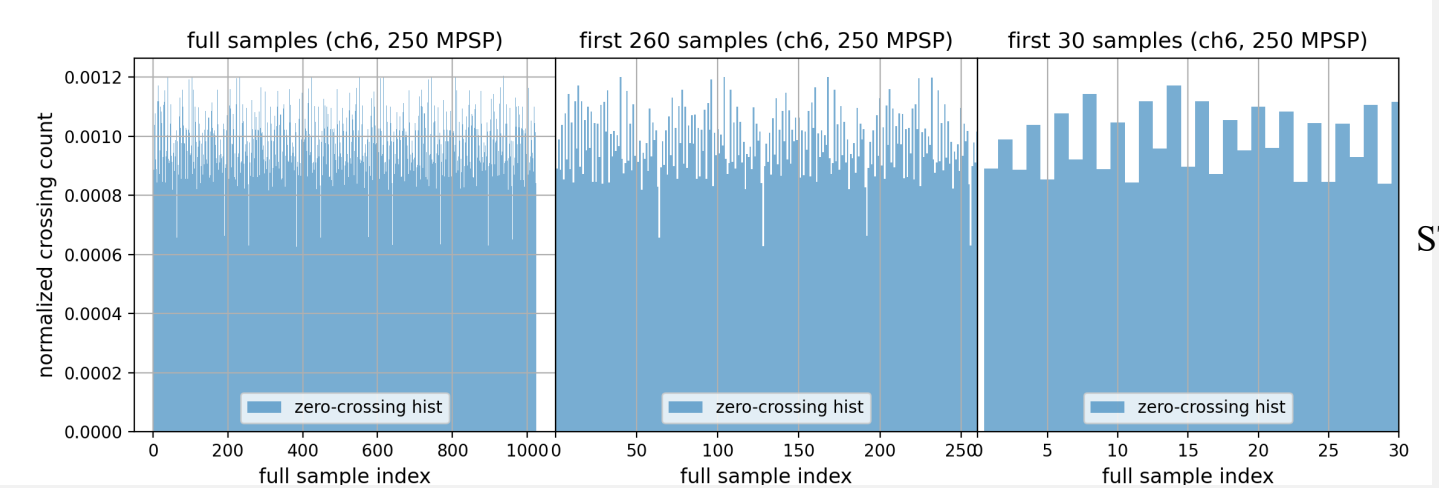
01 Results of timing resolution using zero-crossing

- 1 GSPS



STD: 0.1593731331416353
➔ ~159 ps

- 250 MSPS



STD: 0.10772778724178121
➔ ~107 ps

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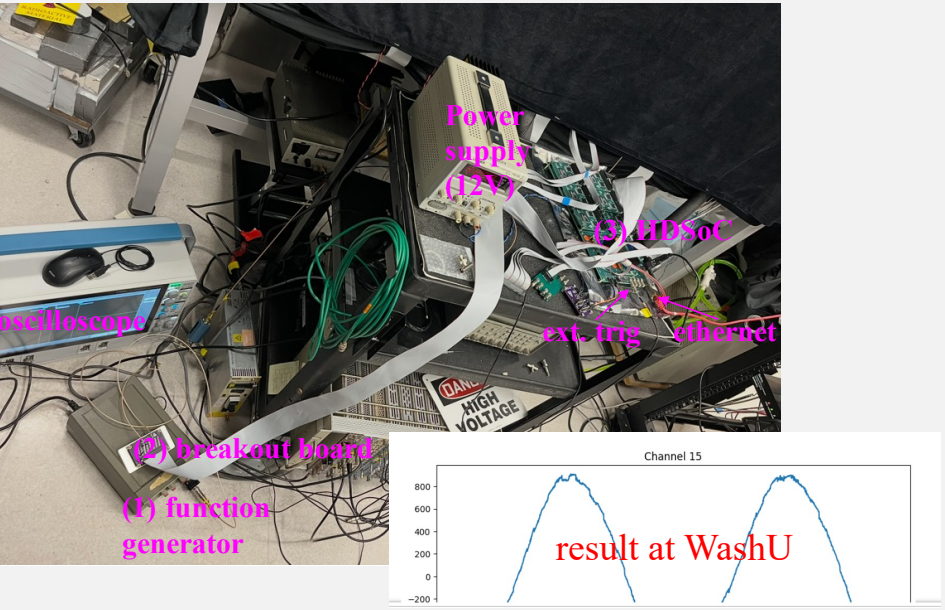
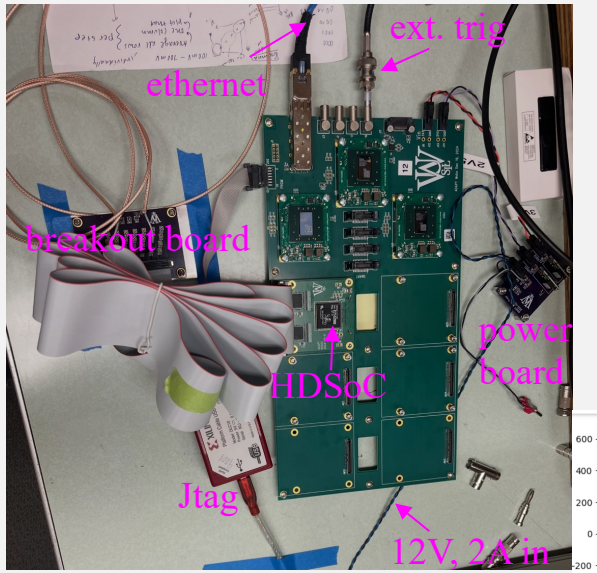
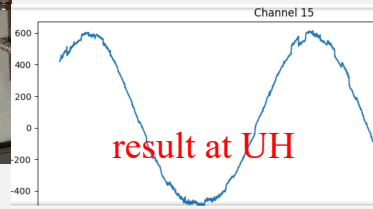
01 Setup duplication at UH

- Aera visited WashU on Oct. 16-17, 2025, and we have duplicated the WashU setup in UH.
  - WashU setup



  - UH setup





- There were several issues alone the way, but thanks to Marion, we now have a working setup at UH.

- Contact people

Ashtar Aggelopoulos	Undergraduate + master course
Guanchen Wu	Undergraduate + master course
Lawrence Zheng	3rd year undergraduate

← Lawrence helped me the most.