Karlsruhe Institute of Technology

BULLKID-DM Readout Electronics

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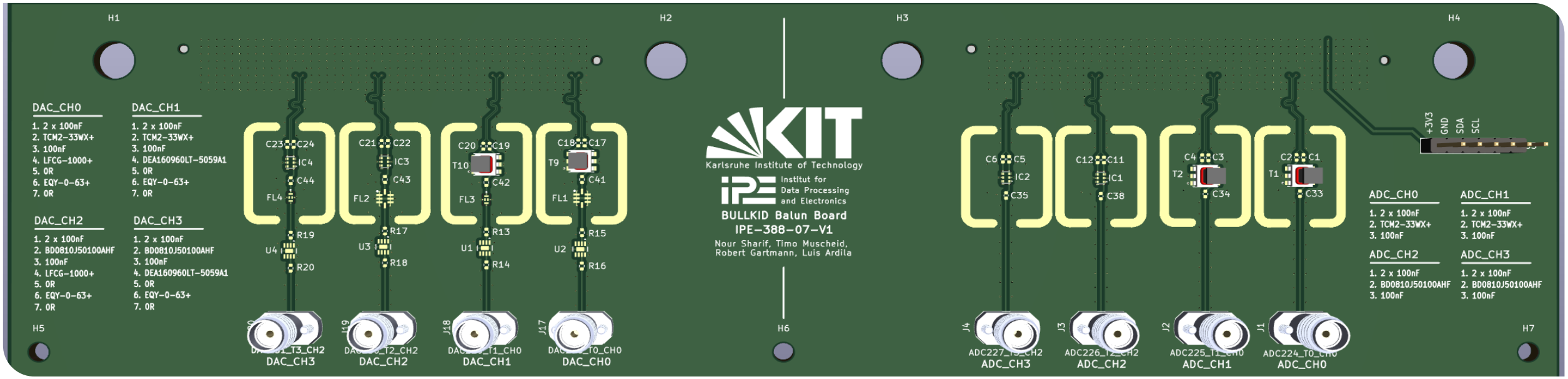
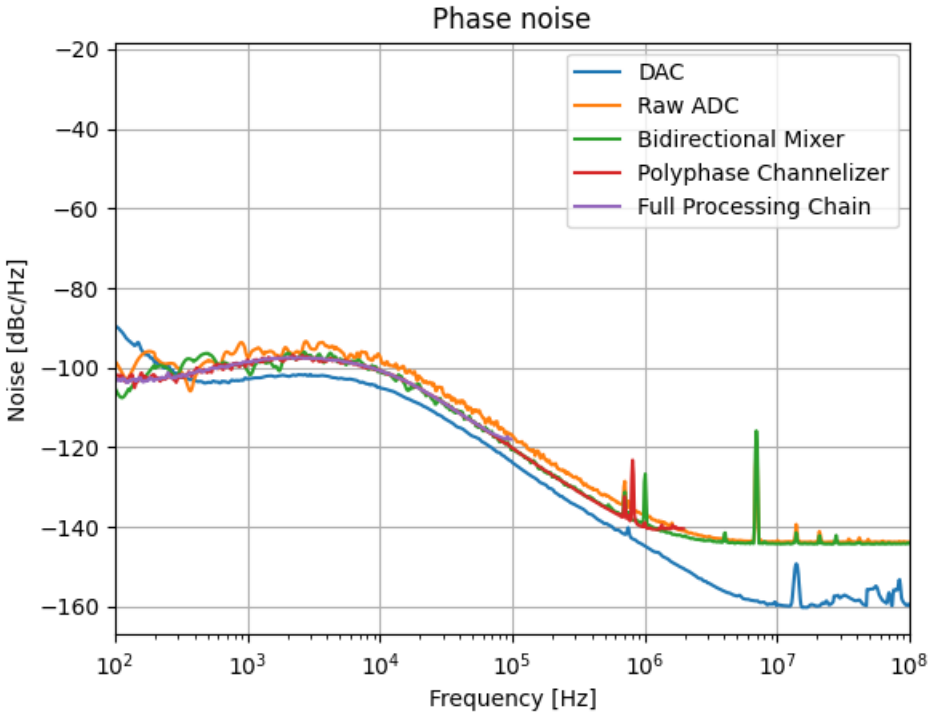
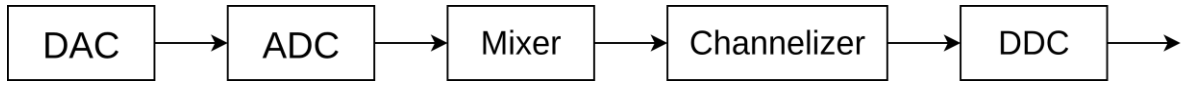


Phase Noise Analysis

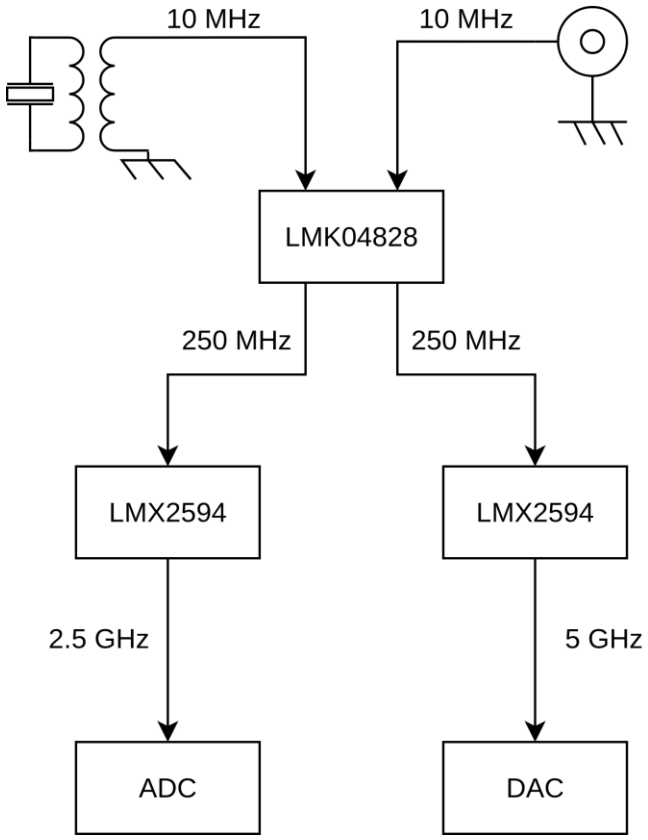


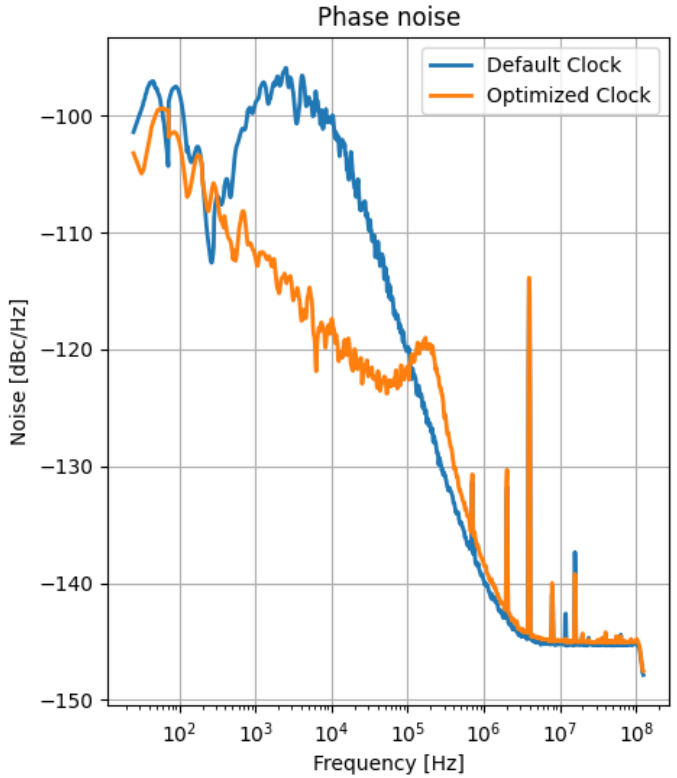
- Evaluation of noise contributions of individual signal processing stages
- Measurement setup:
  - Single tone, f = 831 MHz, max. amp
  - DAC output -> Spectrum Analyzer
  - Loopback -> Python library „pylpsd“
- Target: -100 dBc @ 0.1-10 kHz
- Detailed phase noise analysis results: agenda.infn.it/event/48327

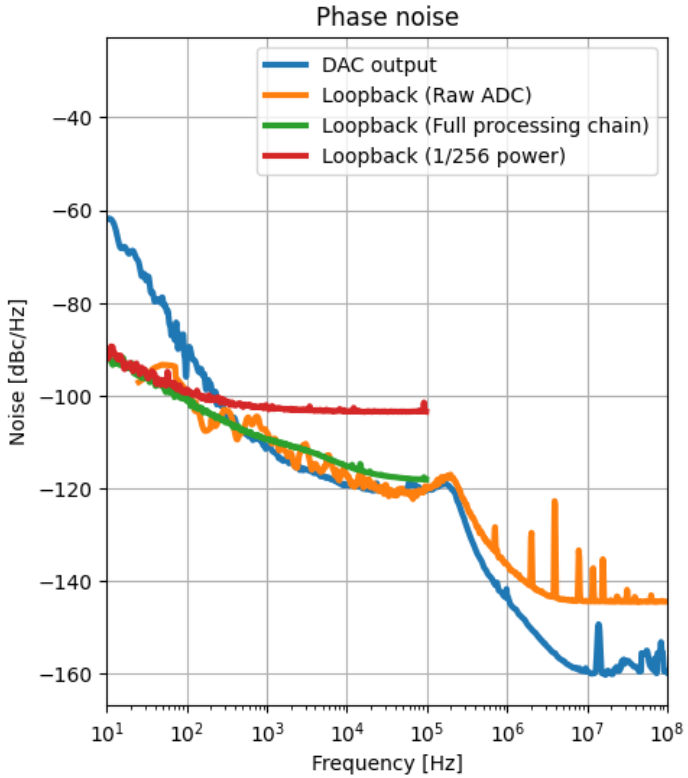


DAC output is limiting phase noise!

Optimization of Clock Tree



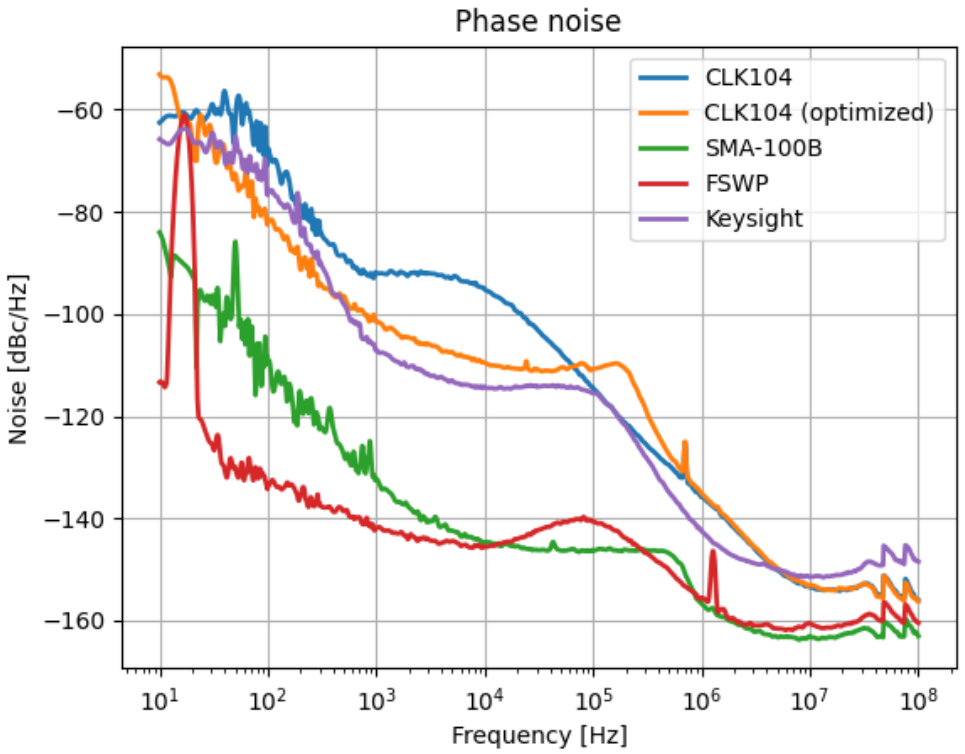




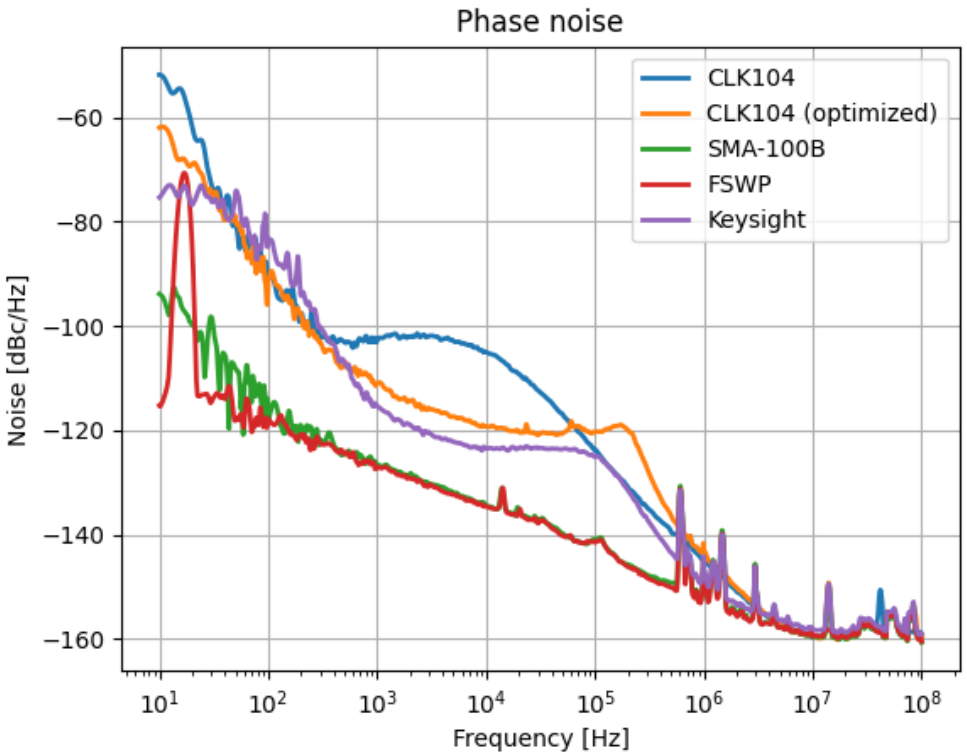
For weak readout tones,
quantization noise becomes dominant

Further Improvement of DAC Output

5 GHz clock signal:

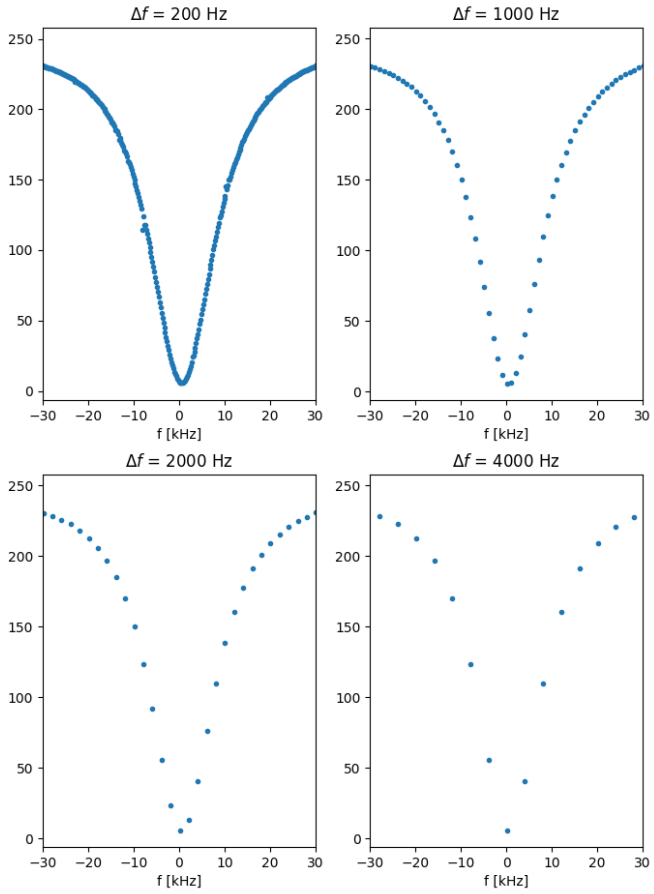


831 MHz DAC output:



External clock source improves the system phase noise

Readout Tone Frequency Resolution



Number of required samples depends on resolution:

$$n = \frac{f_s}{\Delta f} \quad \text{with } f_s = 250\ MHz$$

$$W_s = 2\ x\ 16\ Bit \text{ with } W_s := Bitwidth\ per\ sample$$

For 16 readout lines:

Δf	**Memory**
200 Hz	640 Mb
4 kHz	32 Mb

Available Memory:
60.5 Mb

Possible Solutions:
- Store samples in DDR
- Tone generation based on DSP

Note:
Resonance circle acquisition is not affected, Δf < 1 Hz

Other News

- LTD proceedings ready, will be submitted this week
- Migration of firmware to ZCU208 to evaluate faster ADCs
- New PhD student in KIT group: Daniel Crovo
- New Master student started working on the integration of LANTERN into the DAQ system (Hardware + Firmware)