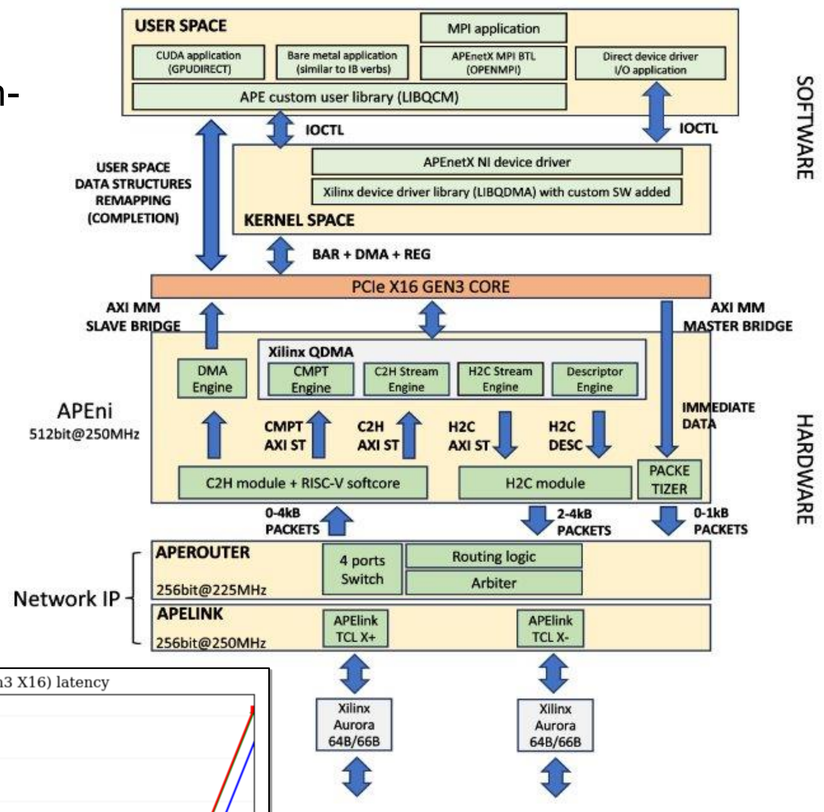
INFN OPEN DAY SEPTEMBER 2025

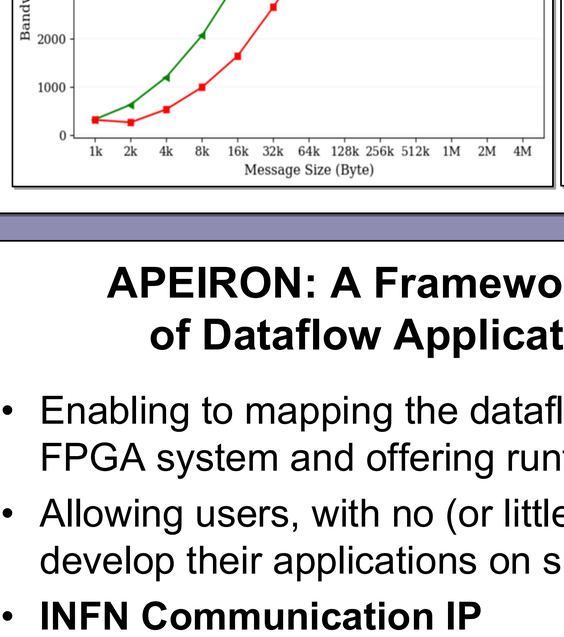
HPC Network Architecture: Multi-FPGA Systems and Upcoming Projects

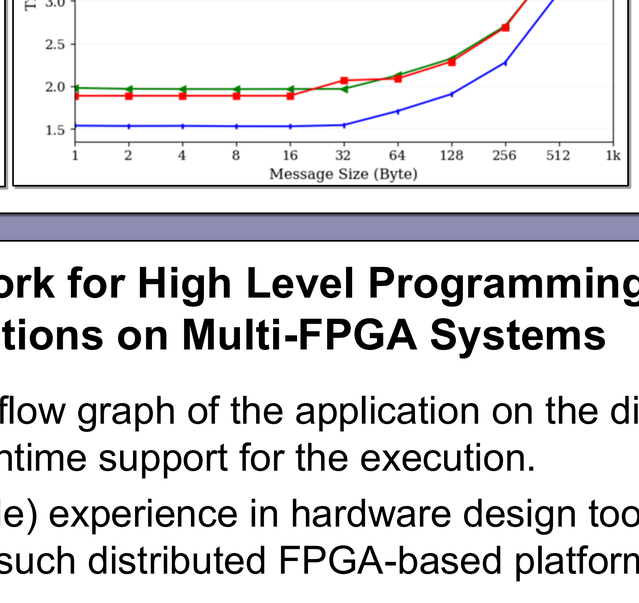
INFN APE Lab Team

APEnetX: INFN Network Interface Card

- **Direct network topology** for low latency and high-throughput
- Use of **FPGA** (programmable component) for architecture exploration and fast&safe desigN
- PCIe x16 Gen3/Gen4 interface
- N-Dim **toroidal** mesh topology
- **RDMA** semantics + **GPUdirect** support
- Custom software stack:
  - **Optimized Linux device driver**
  - **Low-level user library** (similar to verbs)
  - **OpenMPI** integration via BTL
  - **Omnet++ network simulator module**



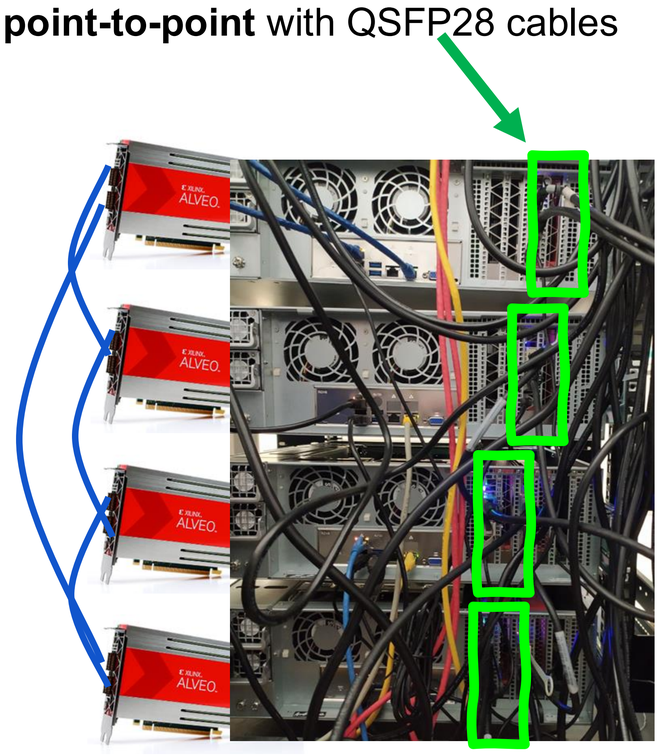




FPGA- based testbed

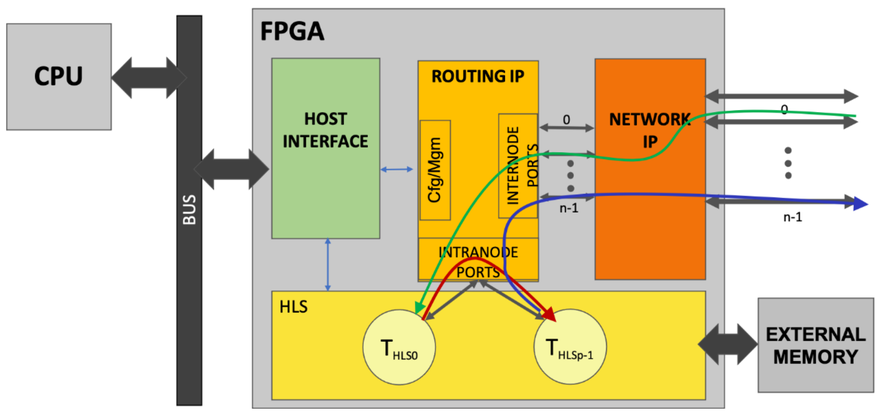
- **AMD Xilinx FPGA U200**
- 4x Supermicro servers
- Sapphire Rapids CPUs
- Gen3 PCIe

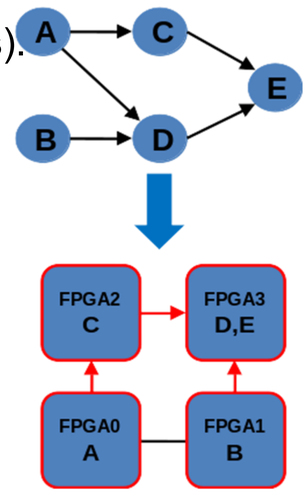
APEnetX prototypes connected point-to-point with QSFP28 cables



APEIRON: A Framework for High Level Programming of Dataflow Applications on Multi-FPGA Systems

- Enabling to mapping the dataflow graph of the application on the distributed FPGA system and offering runtime support for the execution.
- Allowing users, with no (or little) experience in hardware design tools, to develop their applications on such distributed FPGA-based platforms.
- **INFN Communication IP**
- Tasks are implemented in C++ using HLS tools (Xilinx® Vitis).





APEIRON Physics use case

Development of intelligent **Read-Out systems based on Neural networks**

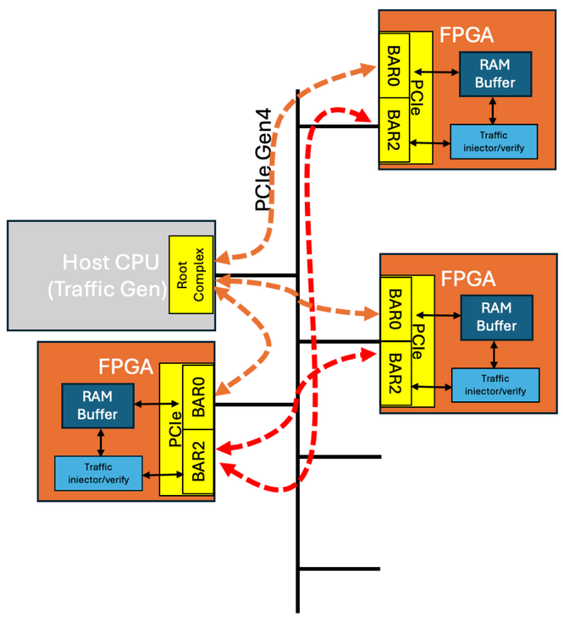
- **Data streams** from different data sources (detectors or sub-detectors) can be recombined through the processing layers using **a low-latency, modular and scalable network infrastructure**
- **Online processing** will be distributed on computing devices (FPGAs for the moment) in *n* subsequent layers.

Real-time inference on FPGAs: why?

- **Customizable I/O**
- **Deterministic latency**
- Useful in **heavy computation**

Project DARE (EuroHPC)
HPC Digital Autonomy with RISC-V in Europe

The **DARE** consortium aims to establish a clear path for software and hardware development in Europe, leveraging early access to **RISC-V** hardware emulation and simulation, with the goal of deploying the developed technologies in European HPC systems



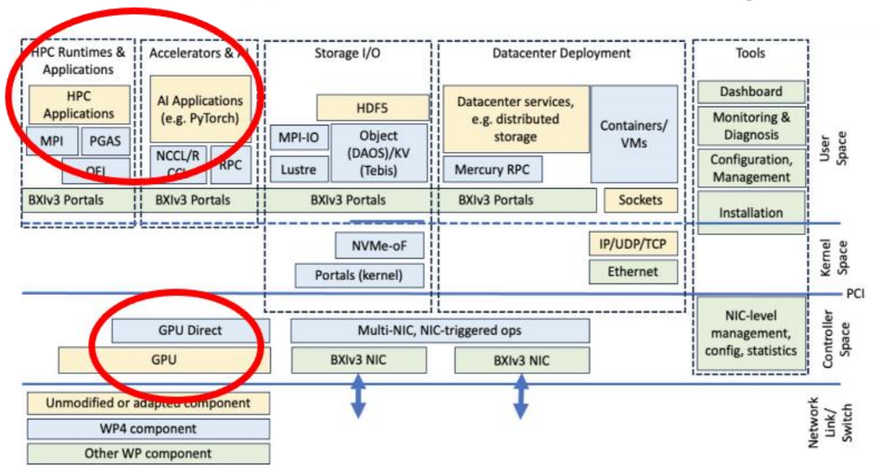
- INFN will contribute with **AI-Direct Engine** enabling the deployment of large scale NN models over multiple AIPU (Artificial Intelligence Processor Unit) accelerators to boost performance of applications like AI-accelerated HPC and Generative AI.
- **AI-Direct Specialized hardware** and its companion system software (linux device driver, user library) will be prototyped on a FPGA-based testbed

Project NET4EXA (EuroHPC)
NETwork for EXascale Architectures

NET4EXA aims to develop a next-generation high-speed interconnect for HPC and AI systems, building on the success of the **BXI European HOC Interconnect** and the advancements made through research in the RED-SEA project and other previous European RIA initiatives.

INFN contribution

- Innovative mechanisms for **congestion control management**
- **ON-NIC processing** for task streaming computing,
- Prototyping new features supporting **GPU triggered computing**
- INFN **scientific applications** for benchmarking network



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APE Lab website: https://apegate.roma1.infn.it