Online Data reduction for the dual-radiator RICH detector readout system in the ePIC experiment

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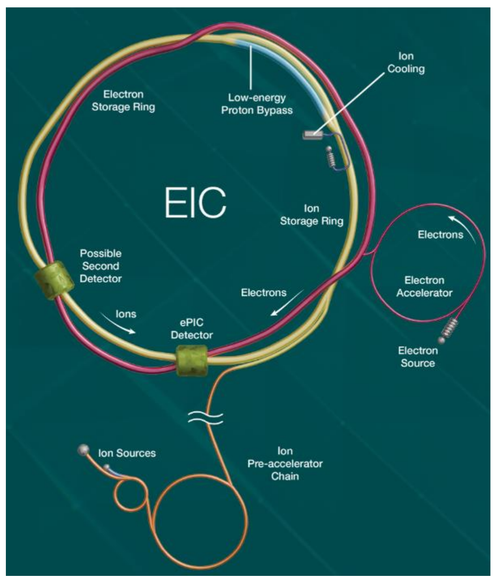
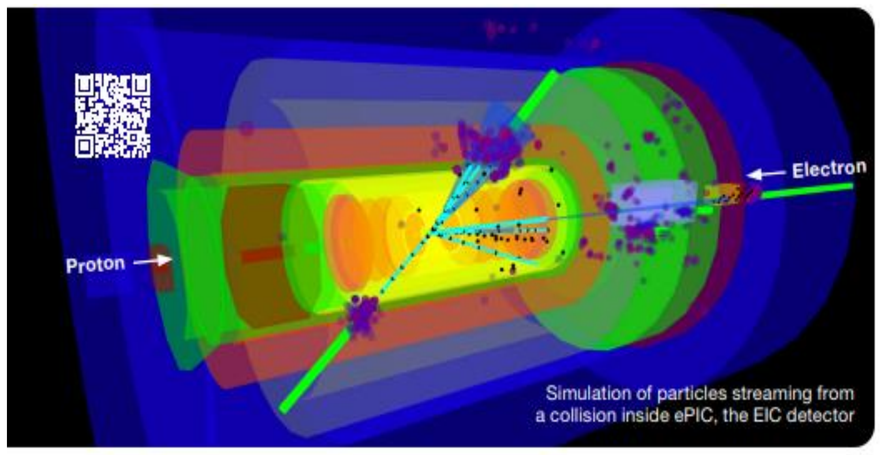
Meeting the demands of online computing in High Energy Physics (HEP) increasingly requires the adoption of advanced hardware and software technologies, many of which stem from related fields like High Performance Computing (HPC) and Artificial Intelligence (AI).
The ePIC experiment at EIC employs a dual-radiator RICH (dRICH) detector for forward particle identification, using silicon photomultipliers (SiPMs) with single-photon sensitivity over ~3 m^2. Its ~320k channels are read out by 4,992 Front-End Boards (FEBs), grouped into 1,248 Readout Boards (RDOs), which transmit data via VRTX+ optical links to FPGA-based FELIX-155 DAMs. Each DAM handles data from 42 RDOs and forwards it through 100 GbE links to the ePIC data buffer (Echelon 0).
To manage the high output bandwidth caused by rising SiPM dark count rates (up to 300 kHz), a AI-based real-time data reduction system will be deployed. It will use distributed processing on the DAMs and a dedicated FELIX-155 Trigger Processor to filter out noise-only events, reducing data volume by at least a factor of ten.



ePIC experiment at Electron-Ion Collider (EIC)

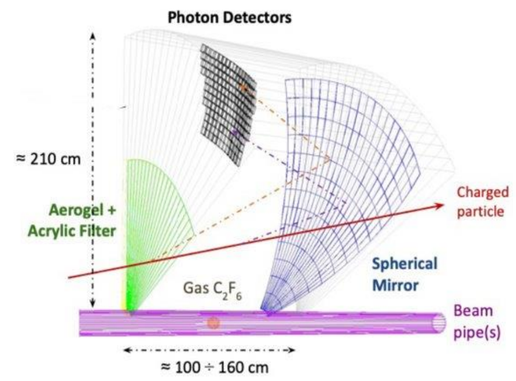
- The **Electron-Ion Collider** (**EIC**) - under development at Brookhaven National Laboratory - is a cutting-edge particle accelerator designed to collide polarized electrons with various ion species. Its goal is to explore hadron structure and the horizons of Quantum Chromodynamics (**QCD**).
- Using high-precision detectors, the EIC will probe the spatial and momentum distributions of quarks and gluons, offering insights into the origins of nucleon spin and mass. The **ePIC detector** will serve as the main experimental tool at Interaction Point 6 (IP6) to support these investigations.

- ~1.7 Tesla superconducting magnet
- High-precision silicon detectors for particle tracking
- Precise calorimeters for measuring particles electromagnetic energy
- Suite of **particle identification** (PID) detectors
- Dense calorimetric detectors to allow the measurement of "jets"



dual-radiator RICH detector (dRICH)

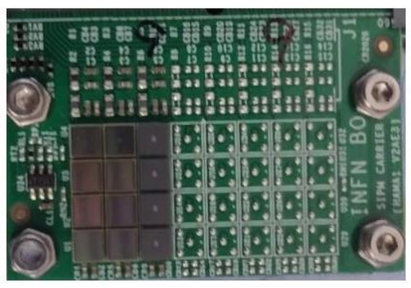
- A **d**ual-radiator **R**ing **I**maging **CH**erenkov detector (**dRICH**) will be employed in the forward region to provide efficient hadron PID from 3 GeV/c to 50 GeV/c.



- **SiPM based photosensors** placed in six spherical sectors to detect Cherenkov photons ⇒ **319488 readout channels**

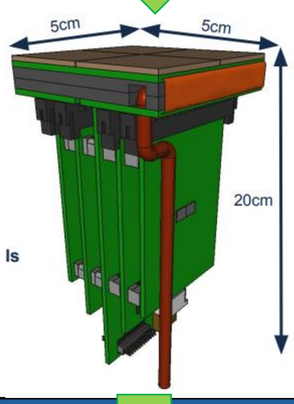
Pros
1. Single photon sensitivity
2. Good **timing performance**
3. Insensitive to magnetic fields
4. Cheap

Cons
1. High radiation sensitivity
2. High **dark count rate** at room temperature



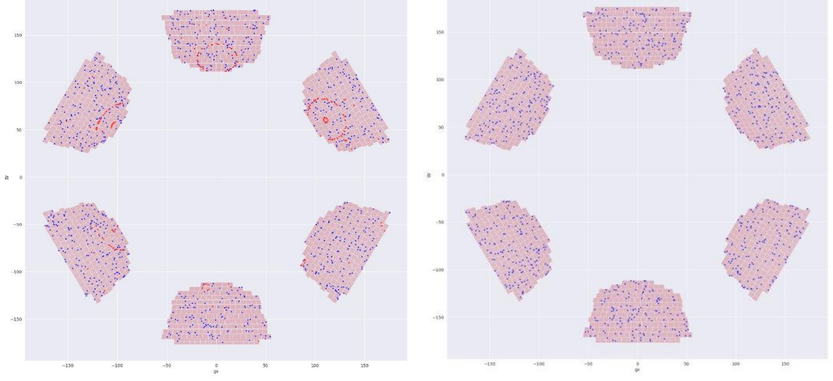
PhotoDetection Unit (**PDU**):
- integrates 256 SiPMs with a pixel size of 3 × 3 mm2
- 4 ALCOR-based Front-End boards (FEBs)
- 1 FPGA-base Readout board (RDO)

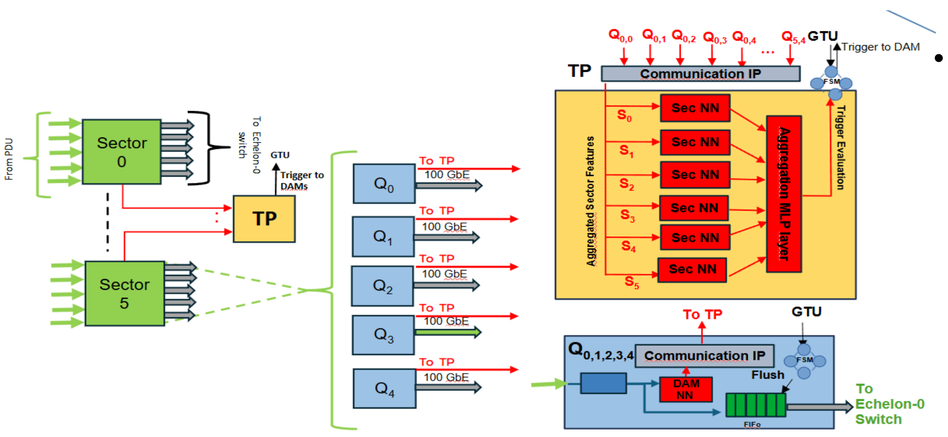
⇒ **~1248 PDUs for full dRICH readout**



Online Data reduction ⇒ Signal/ Noise discrimination using ML classifier

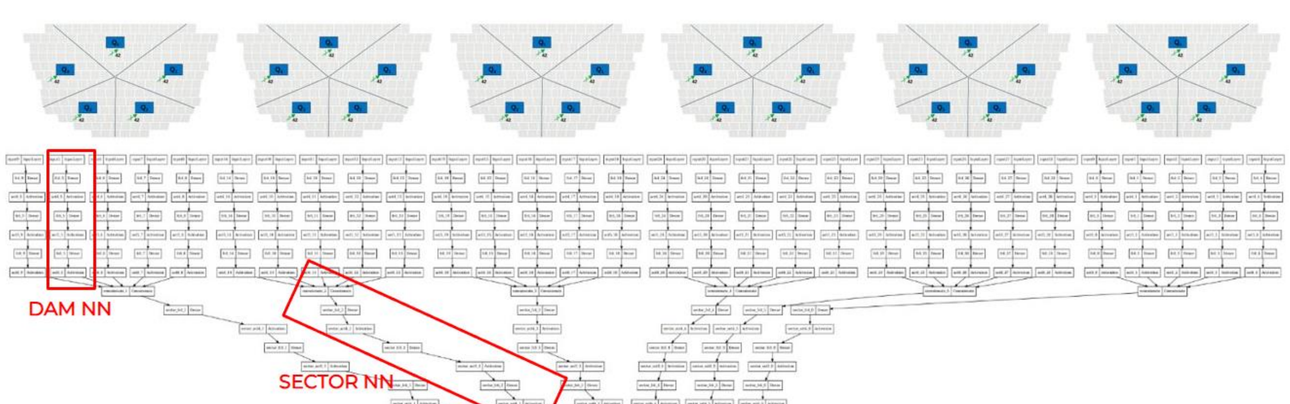
- SiPM DCR expected to reach up to **300 kHz**
  ⇒ risking **excessive dRICH output bandwidth**
  ⇒ **real-time data reduction system** designed to cut bandwidth by **at least a factor 5**.
- **Event-level classification**:
  - **Keeps** events with physics signal (including background) + noise
  - **Discards** DCR noise-only events



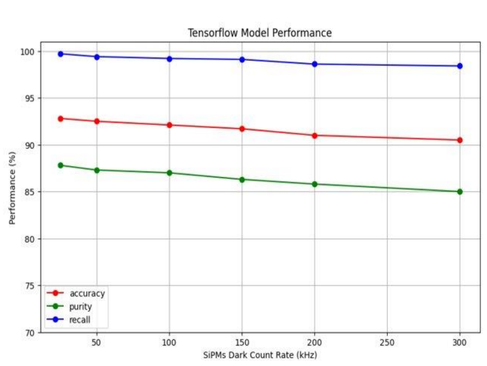


- **Distributed dataflow process** on:
  - **DAMs**
  - **Trigger Processor (TP)**

⇒ data reduction signal (aka, trigger) sent via GTU to allow standard readout event-flow through ePIC storage and processing units

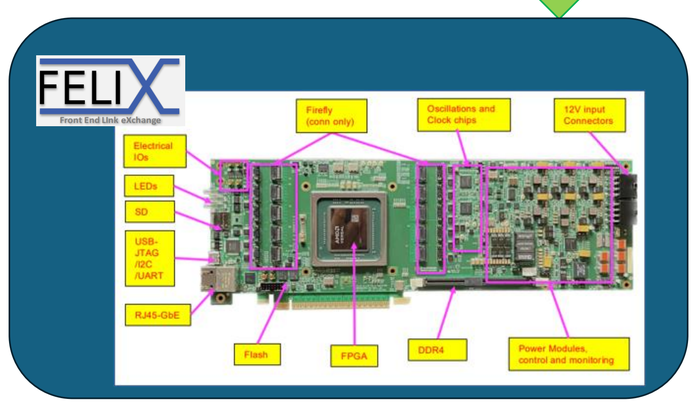


- **Distributed Multi-Layer Perceptron Neural Network (MLP)**
  - Each DAM runs **30 sub-network replicas**
  - Processes event fragments to extract key features
  - Sends features to the TP via **low-latency link**

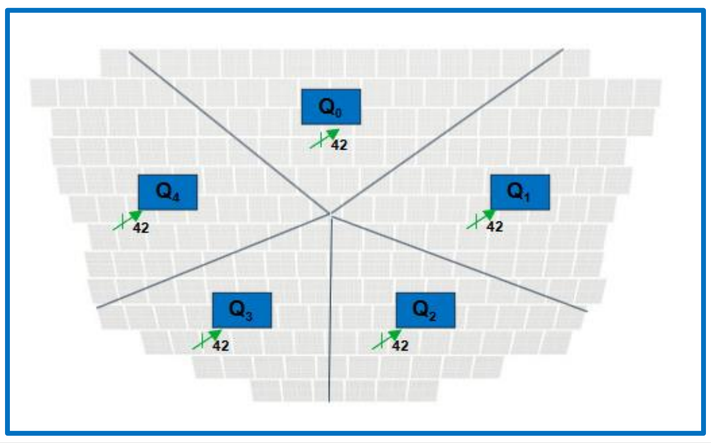


Data Aggregation Module (DAM)

- Next generation **FELIX** boards (developed for the Phase-II upgrade of the ATLAS experiment at LHC) adopted as **DAM** boards.



- FELIX FLX-155 board is built around the new **Xilinx Versal FPGA/SoC** family:
  - **48 serial links** running at speeds up to 25Gbps
  - **100Gb ethernet** link off the board
  - **DDR4 16GB RAM** slot available to support buffering
  - **PCIe Gen5x16 bus**



VPK-180 Total PL mem 994 Mb

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