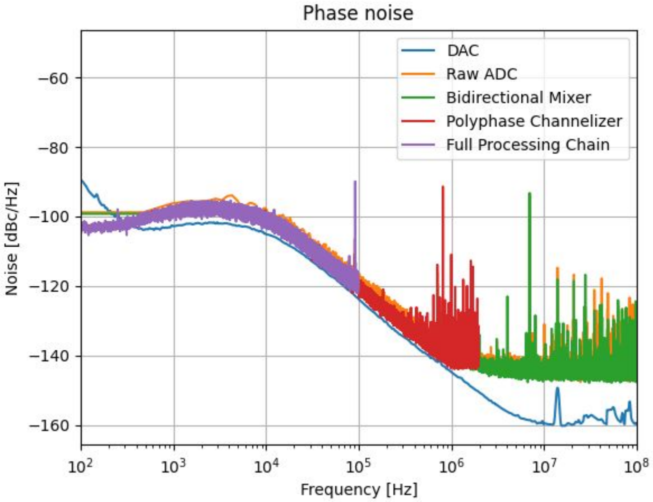
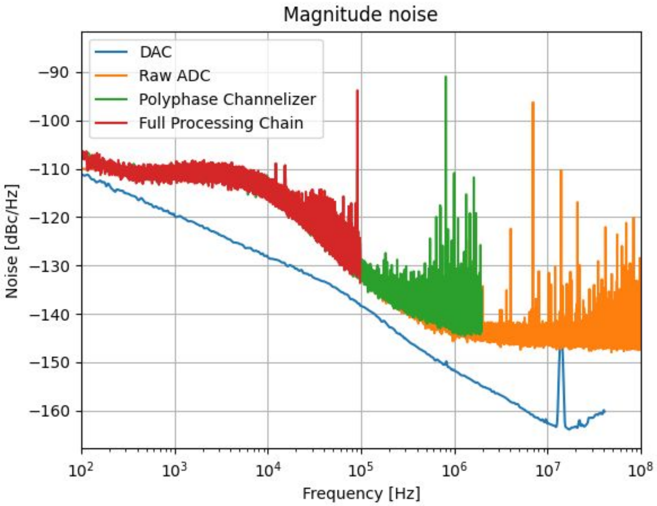
Phase Noise Analysis

BULLKID-DM readout electronics

Noise contributions

DAC → ADC → Mixer → Channelizer → DDC →



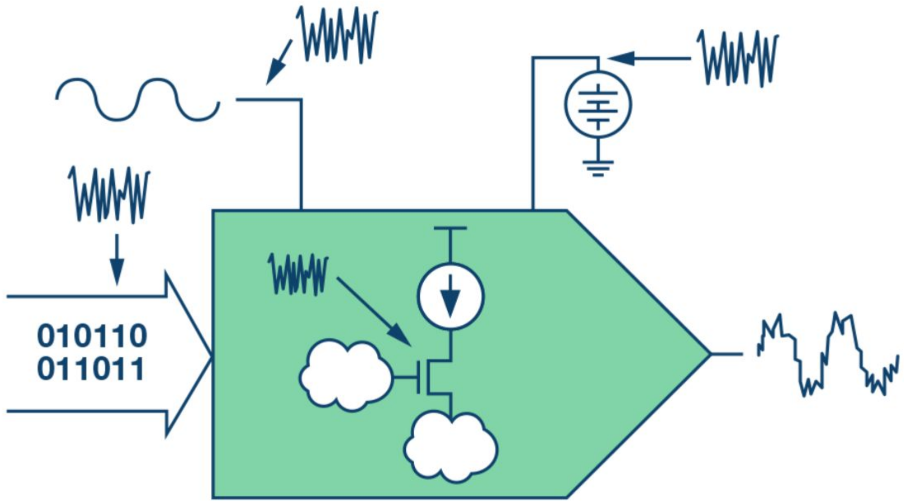


Measurement setup:
- Single tone
- f = 831 MHz
- Max. amplitude

- DAC output measured with FSWP
- Other measurements in loopback mode

Phase noise seems to be limited by the DAC

DAC Noise analysis



DAC noise sources:

1. Digital input

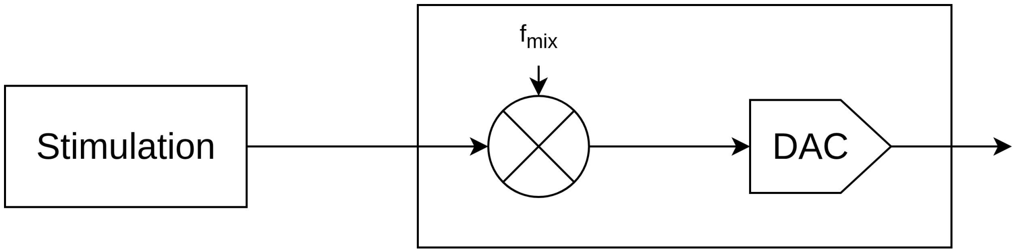
2. Clock source

3. Power supply

4. Analog output

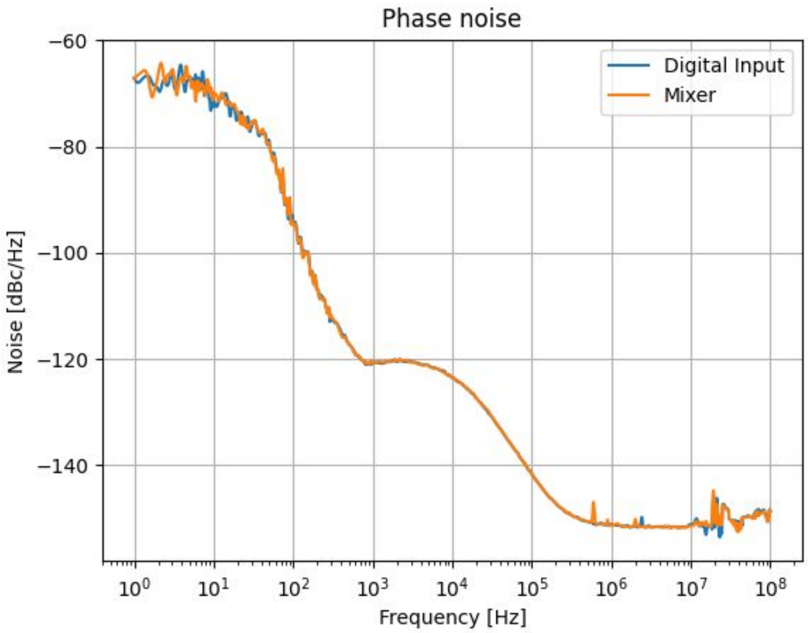
https://www.analog.com/en/resources/analog-dialogue/articles/analyzing-and-managing-the-impact-of-supply-noise-and-clock-jitter-on-high-speed-dac-phase-noise.html

DAC Phase Noise – Digital input



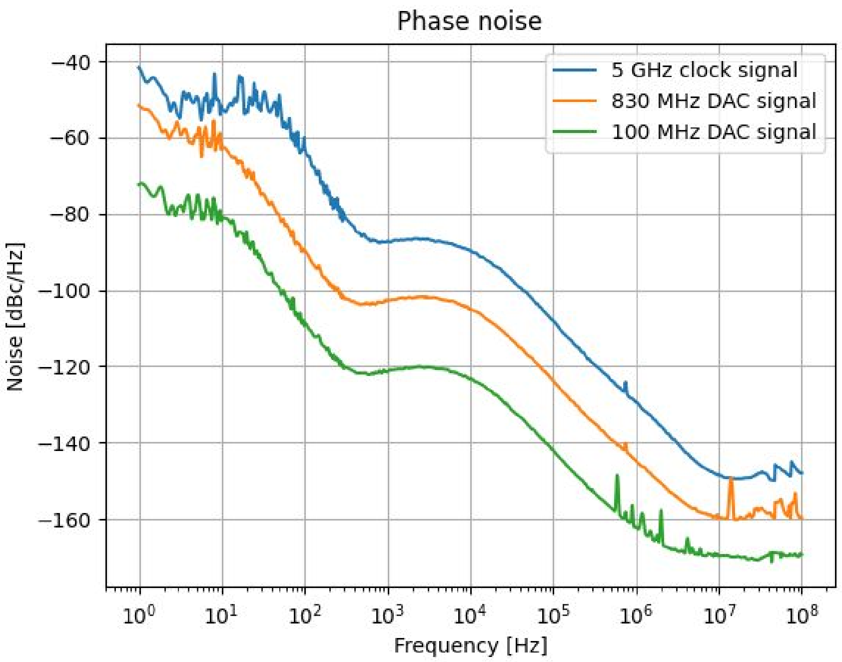
Two measurements:

- Generate 100 MHz tone with stimulation module
- Use DC signal + mixer to generate 100 MHz tone



Digital input of the DAC is not the limiting factor

DAC Phase Noise – Clock source



Spot noise [dBc/Hz]:

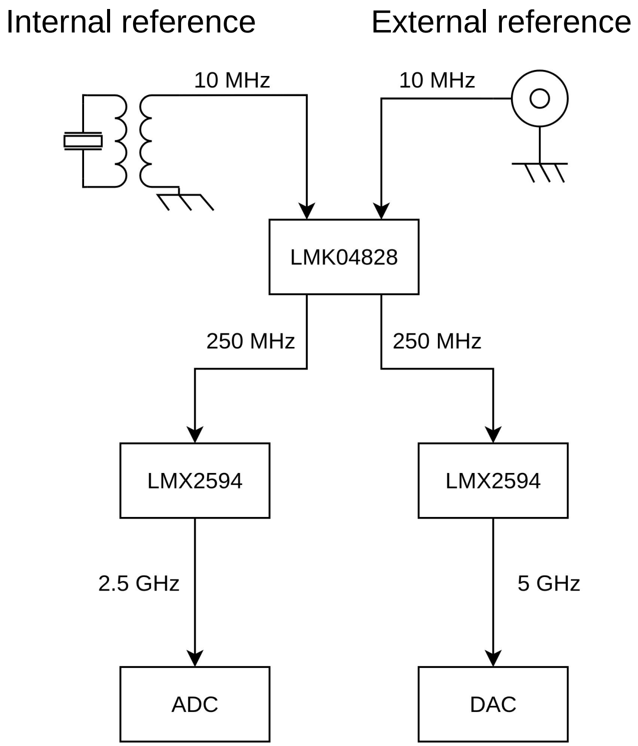
	100 Hz	1 kHz	10 kHz	100 kHz
5 GHz clock	-62.5	-87.2	-89.7	-108.1
830 MHz DAC	-89.7	-102.8	-105.1	-123.8
100 MHz DAC	-108.6	-121.4	-123.2	-142.0

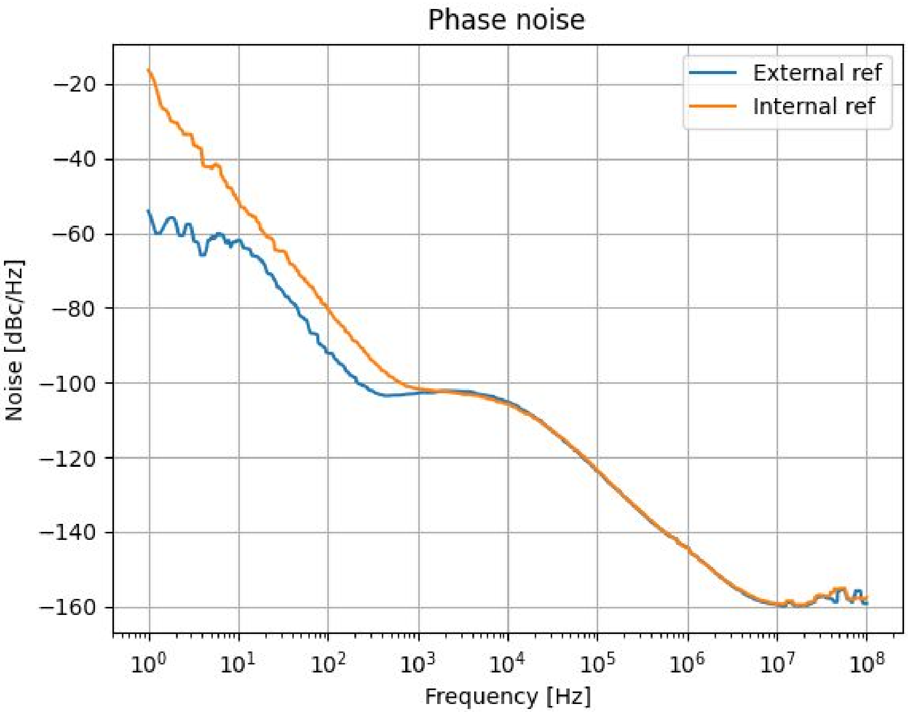
Dependence of DAC noise from clock source noise:

$$N_{sig} = N_{clk} + 20 * \log 10\left(\frac{f_{sig}}{f_{clk}}\right)$$

Clock source seems to be the main source for DAC phase noise

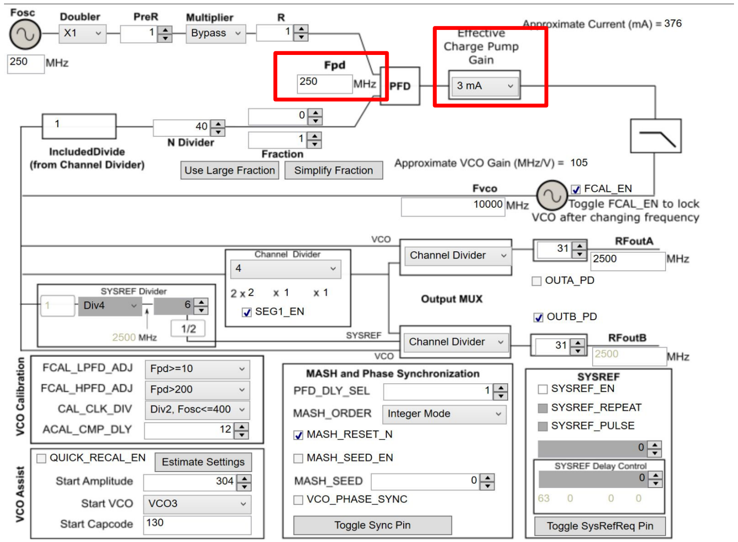
Clock Tree Analysis



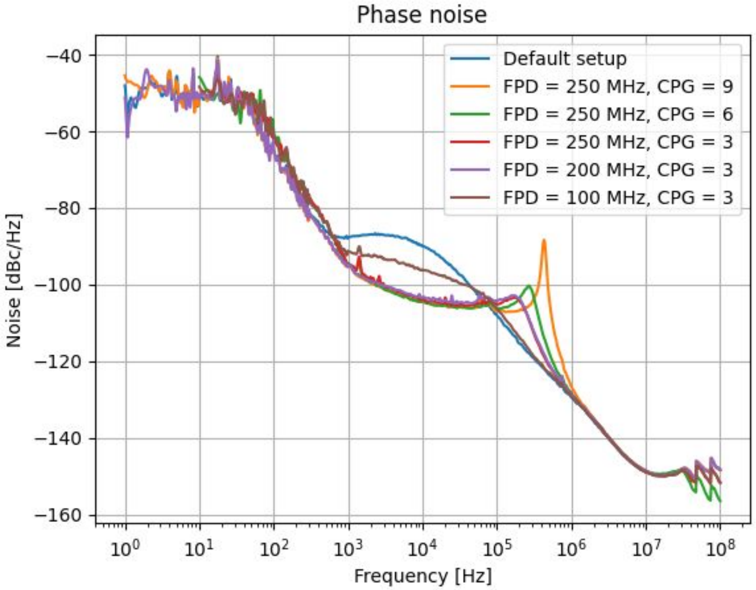


DAC clock optimization

LMX2594 configuration tool:



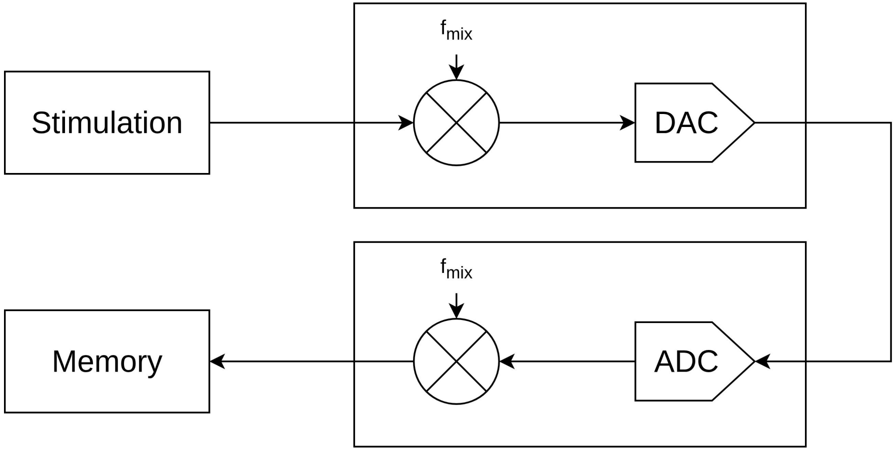
5 GHz clock output analysis:

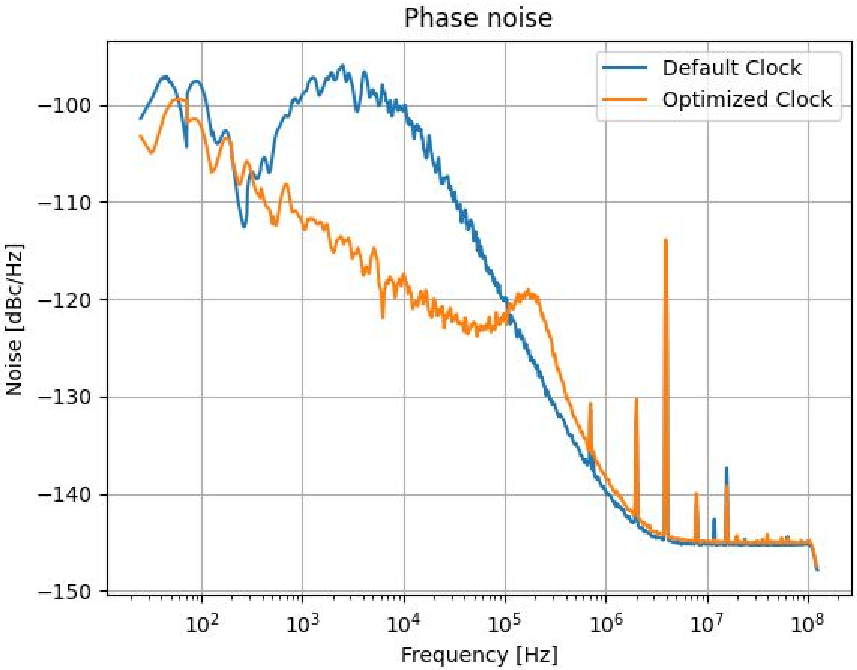


Optimal configuration (DAC, ADC): Charge Pump Gain: 3 mA, f_{pd} = 250 MHz

Improvement in loopback mode

Measurement setup:



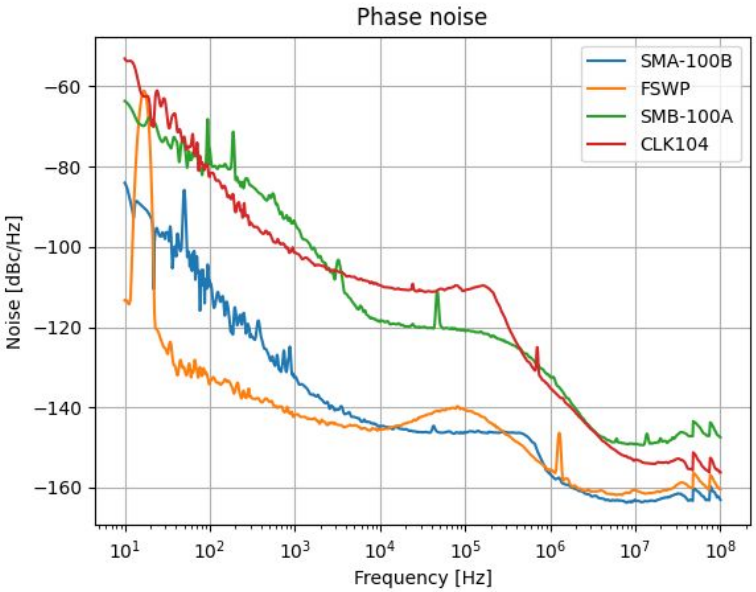


- Single tone, 831 MHz
- DDC calculated offline in Python

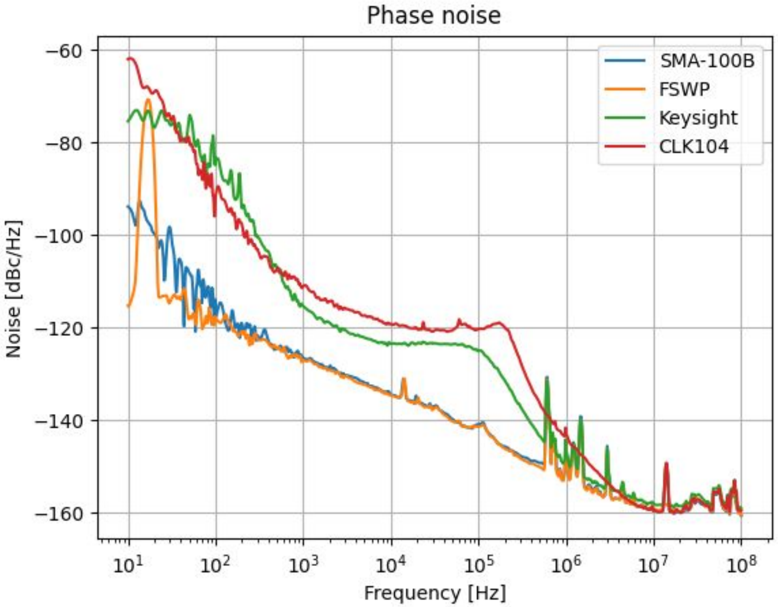
New clock config improves phase noise!

Further improvements possible?

2.5 GHz clock signal:

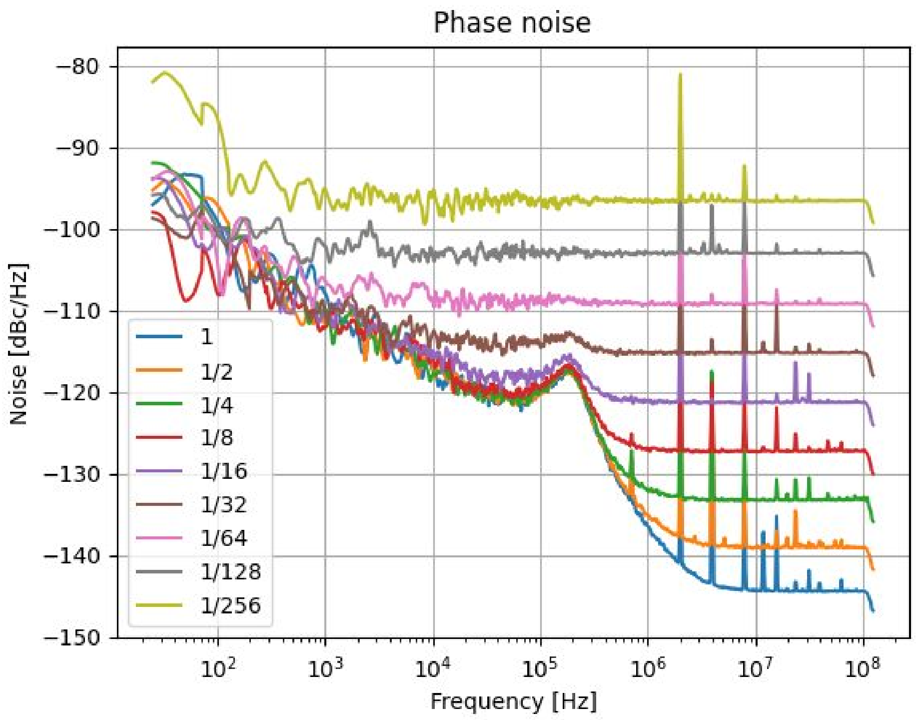


831 MHz DAC output



Custom clock board further improves the phase noise

Towards full-scale frequency comb

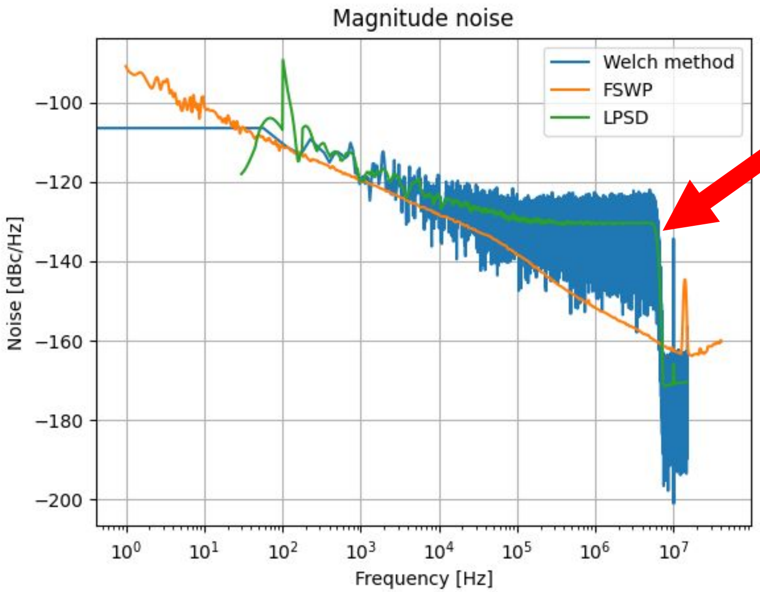


Measurement setup:
- Single tone, 831 MHz
- Decreasing amplitude

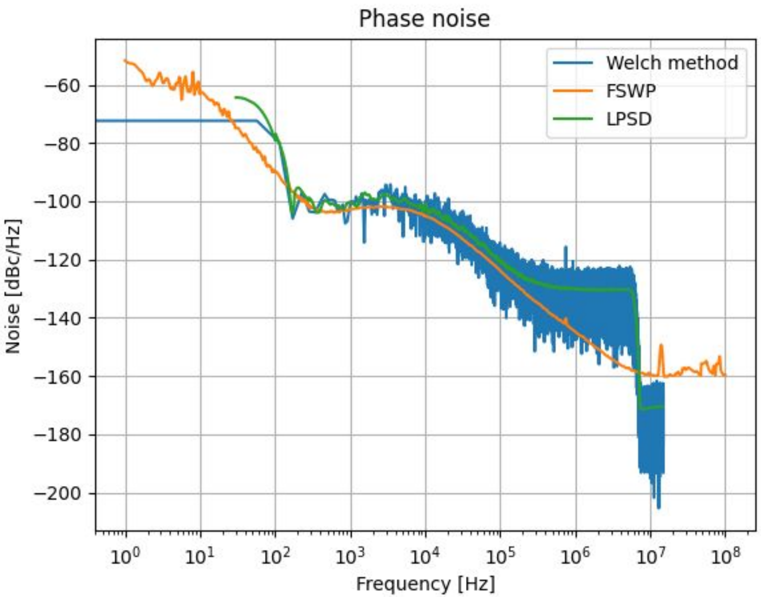
Result:
- With low carrier power, additive noise becomes dominant
- Can be reduced with amplifiers (Clipping!)

Backup

Analysis method verification

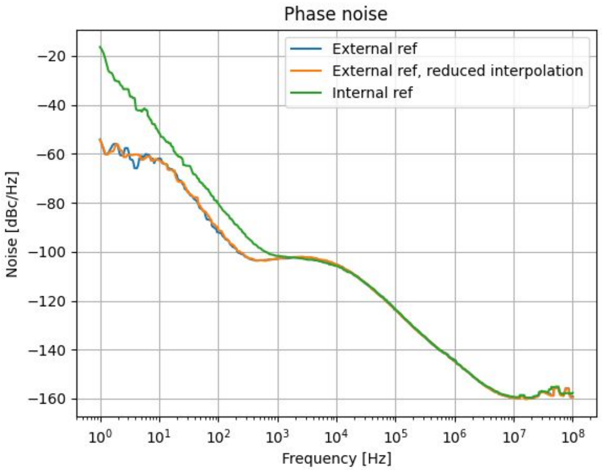


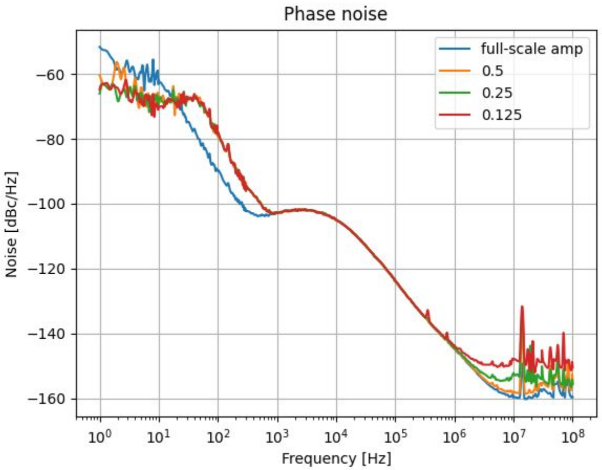
Analysis
BW limit

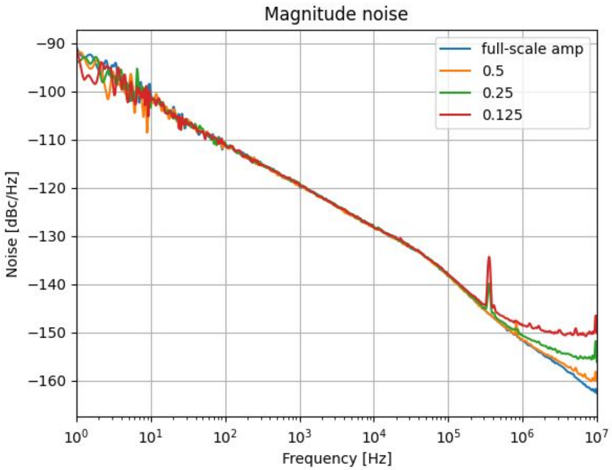


- Comparison of build-in phase/magnitude noise measurement with custom analysis
- Limits of I/Q trace:
  - max. sample rate: 30 MHz
  - max. analysis BW: 10 MHz
  - max. number of points: 1000000

DAC Characterization



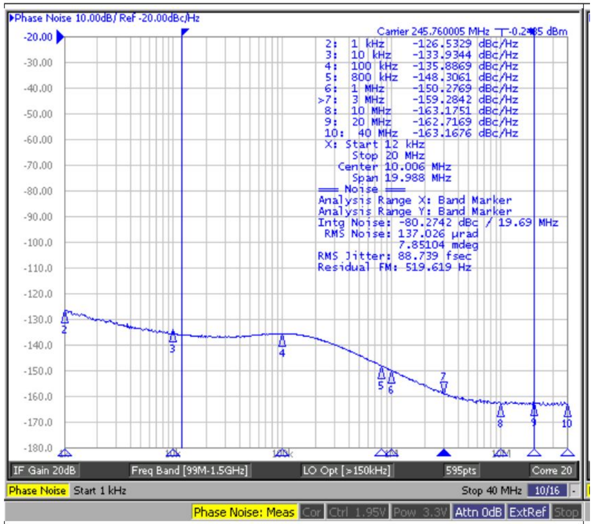




- Locking to external 10 MHz reference clock improves phase noise
- Reducing interpolation factor has no effect
- Reducing tone power does not deteriorate noise (phase and magnitude)

Clock chip performance

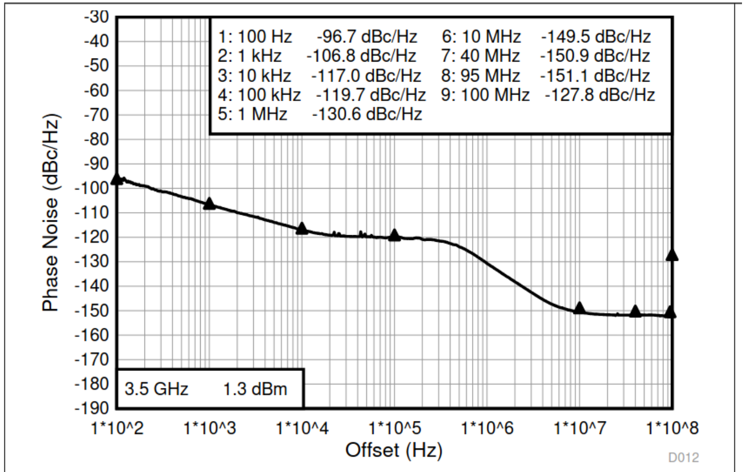
LMK04828 (Jitter = 88.7 fs)



VCO_MUX = 0 (VCO0)   PLL2 Loop Filter Bandwidth = 288 kHz
VCO0 = 1966.08 MHz   PLL2 Phase Margin = 72°
DCLKout2_DIV = 8

Figure 2. LMK04821 DCLKout2 Phase Noise

LMX2594 (Jitter = 49.4 fs)



f_{OSC} = 100 MHz
f_{PD} = 200 MHz
f_{VCO} = 14 GHz
f_{OUT} = 14 GHz / 4 = 3.5 GHz
Jitter = 49.4 fs (100 Hz - 100 MHz)

Figure 9. Closed-Loop Phase Noise at 3.5 GHz