dRICH Back-End:
FLX 182 status/updates

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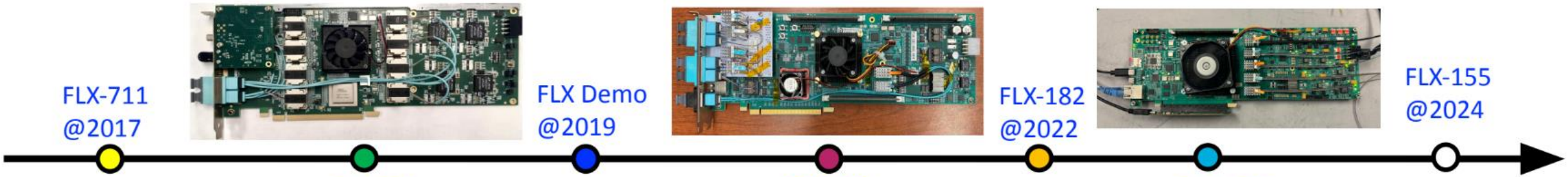
FELIX Hardware Development at BNL



FLX-711 @2017

PCIe Gen3 x16
48x 10 Gb/s
DDR3

FLX-712 @2018

PCIe Gen3 x16
48x 10 Gb/s

FLX Demo @2019

PCIe Gen3 x16
25 Gb/s with various optical modules

FLX-181 @2021

PCIe Gen4 x16
FMC+ 16x 25 Gb/s
12x 16 Gb/s
SoC / DDR4

FLX-182 @2022

PCIe Gen4 x16
28x 10/25 Gb/s
100 GbE
SoC / DDR4

FLX-182B @2023

FLX-155 @2024

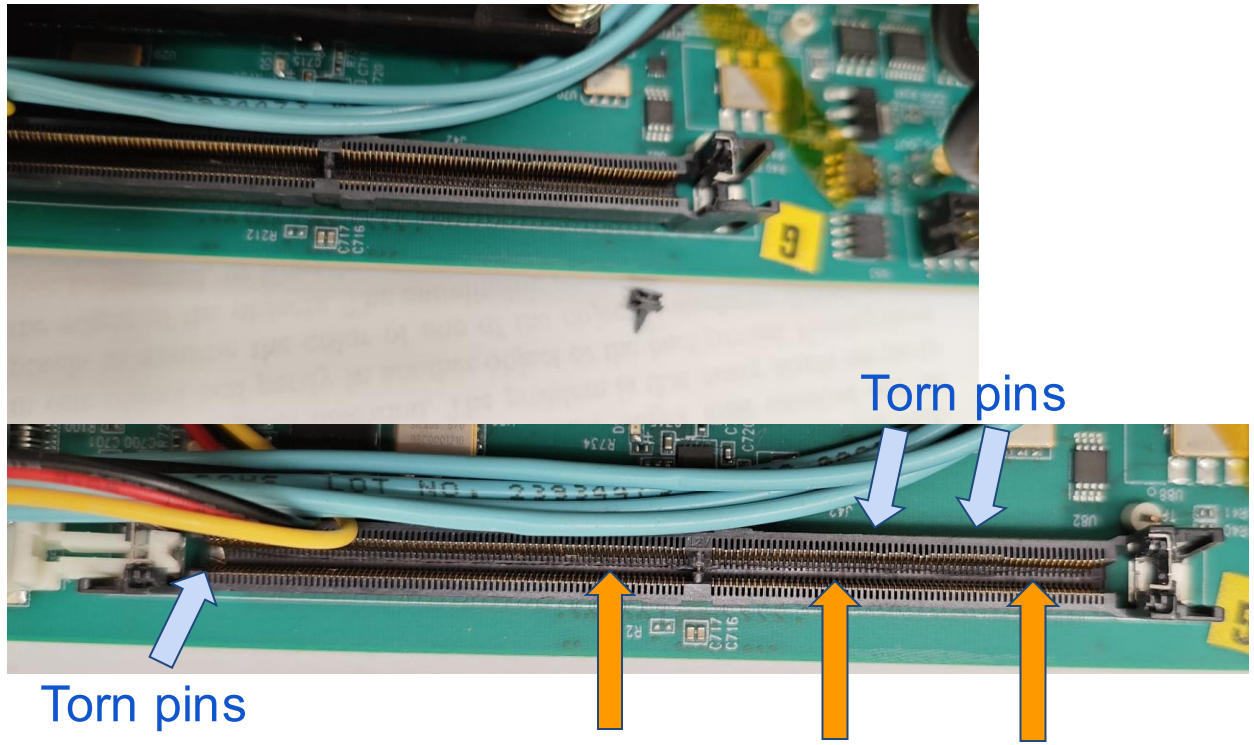
PCIe Gen5 x16
48x 10/25 Gb/s
100/400 GbE
SoC / DDR4

FLX-182B Hardware

Assembled FLX-182B

- FPGA: Xilinx Versal Prime XCVM1802
- PCIe Gen4 x16, 256 GT/s
- 24 FireFly links with 3 possible configurations
  - 24 links up to 25 Gb/s
  - 24 links up to 10 Gb/s (CERN-B FireFly)
  - 12 links up to 25 Gb/s + 12 links up to 10 Gb/s
- 4 FireFly links with 2 possible configurations with 14 or 25 Gb/s FireFly TRx
  - LTI interface
  - 100 GbE
- Built-in self test, online configuration and monitoring
- White Rabbit
- DDR4 Mini-UDIMM
- GbE/SD3.0/PetaLinux

Procurement of a Felix-182 Card



Felix-182 board on loan from Jlab arrived in Rome end of December ’24 (thanks David Abbott!).

Unfortunately it showed damages to the DRAM slot:

- **torn contact pins**
- **a crack along the inner side of the slot**

They likely occurred due to the pressure of a DRAM module left in the slot during the delivery.

As a consequence, DRAM is not detected by the system.

We attempted to load official firmware onto the board (https://gitlab.cern.ch/atlas-tdaq-felix/firmware/) but the process failed due to a DRAM check error.

We consulted:

- the INFN Electronics Laboratory in Rome
- CERN EP-ESE Electronic Systems for Experiments (thanks Markus Joos!)

Both agreed that is extremely difficult to repair the DRAM slot and not worth the effort considering the costs and the likely not optimal result, we were ready to send it back…

Installation of a Felix-182 Card @ APE Lab

Homemade fix: We experimented with various imaginative tools to better connect the DRAM.

The issue persisted!

- We got advice from Carlo Alberto Gottardo (Coordinator of the FELIX project) about the fact that the DRAM is used only by the PS (ARM SoC) and that in current FW versions the PS performs just ancillary functions (BIST,…), while all the design core functionalities are implemented in the PL.

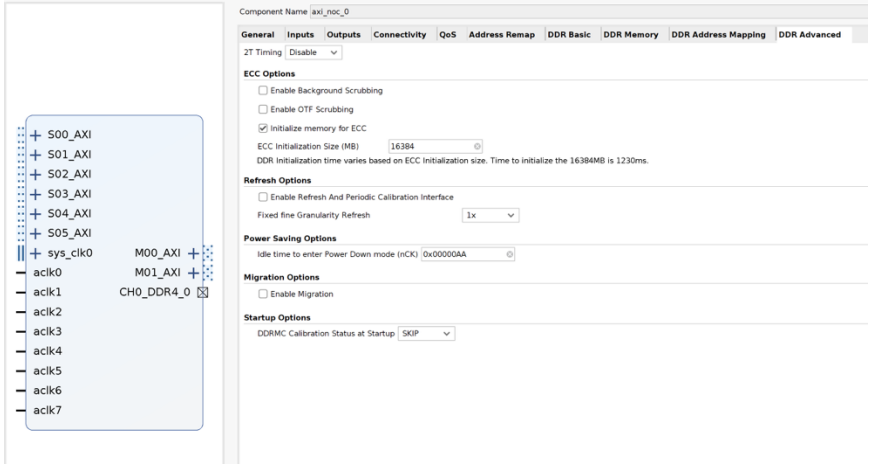
Preliminary solution: we modified the release FW removing the PS (and DRAM) from the design -> modified FW loaded and board detected!

The issue was solely related to the unconnected DDR

Installation of a Felix-182 Card @ APE Lab

Final solution:

- in the FELIX-182 FW (in cips_BD_BNL182 block design) there is a component, the Xilinx AXI NoC that functions as a high-bandwidth scalable fabric to connect blocks. Xilinx AXI NoCcan be configured to include one or more integrated DDR memory controllers (MCs).
- Startup Options: DDRMC Calibration Status at Startup to SKIP. The default behavior for the Versal PLM at boot is to gate the assertion of the Configuration DONE signal if a DDRMC fails calibration. If this option is set to SKIP then the DDRMC calibration status will be ignored at startup and DONE will assert regardless of the DDRMC status.



FW loaded and board detected!

```
[locicero@apestation0 ~]$ lspci -vvvvvv | grep CERN
34:00.0 Network controller: CERN/ECP/EDU Device 0428
        Subsystem: CERN/ECP/EDU Device 0038
35:00.0 Network controller: CERN/ECP/EDU Device 0427
        Subsystem: CERN/ECP/EDU Device 0038
```

2 PCIe Gen4 x8 (on a bifurcated x16 slot)

Project Summary

Synthesis

Status:	✓ Complete
Messages:	! 992 warnings
Active run:	synth_1
Part:	xcvm1802-vsva2197-1MP-e-S
Strategy:	Flow_PerfOptimized_high
Report Strategy:	Vivado Synthesis Default Reports
Incremental synthesis:	Automatically selected checkpoint

Implementation

Status:	✓ write_device_image Complete!
Messages:	! 11 critical warnings
	! 95 warnings
Active run:	impl_1
Part:	xcvm1802-vsva2197-1MP-e-S
Strategy:	Performance_ExplorePostRoutePhysOpt
Report Strategy:	Vivado Advanced Implementation Default Reports
Incremental implementation:	None

DRC Violations

Summary: ! 929 warnings

Implemented DRC Report

Timing

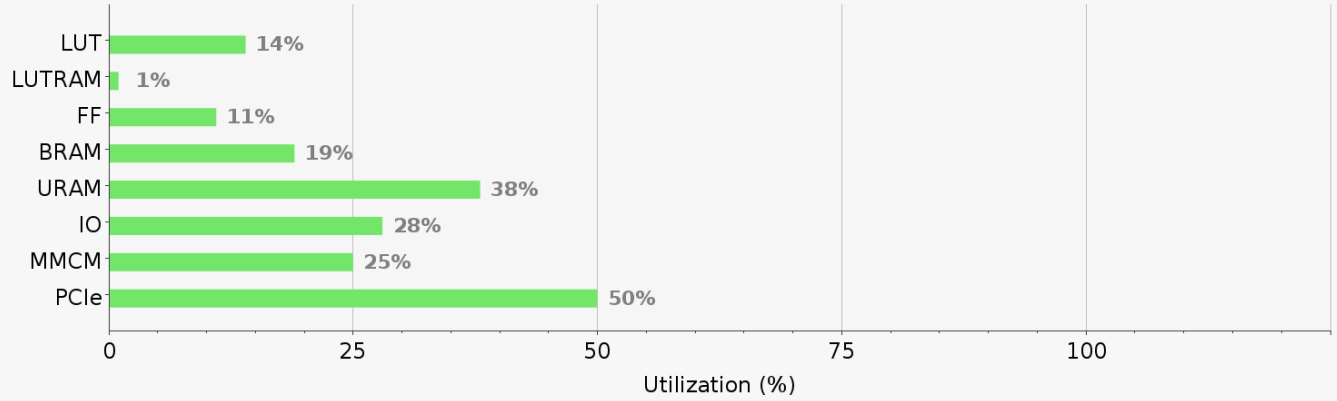
Worst Negative Slack (WNS):	0.01 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	490240

Implemented Timing Report

Utilization

Post-Synthesis | **Post-Implementation**

Graph | Table



Power

Total On-Chip Power:	**23.056 W**
Junction Temperature:	**100.0 °C**
Thermal Margin:	0.0 °C (8.7 W)
Effective ϑJA:	3.3 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

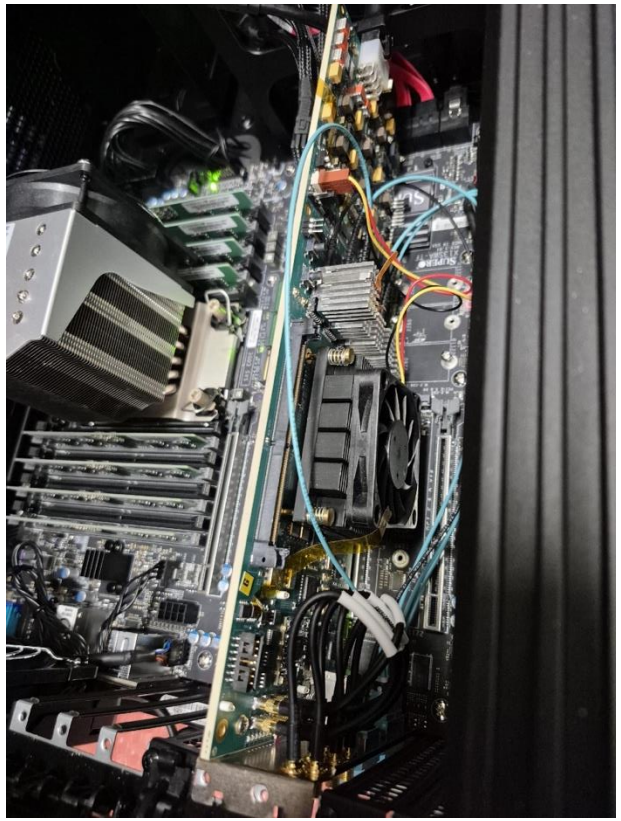
Implemented Power Report

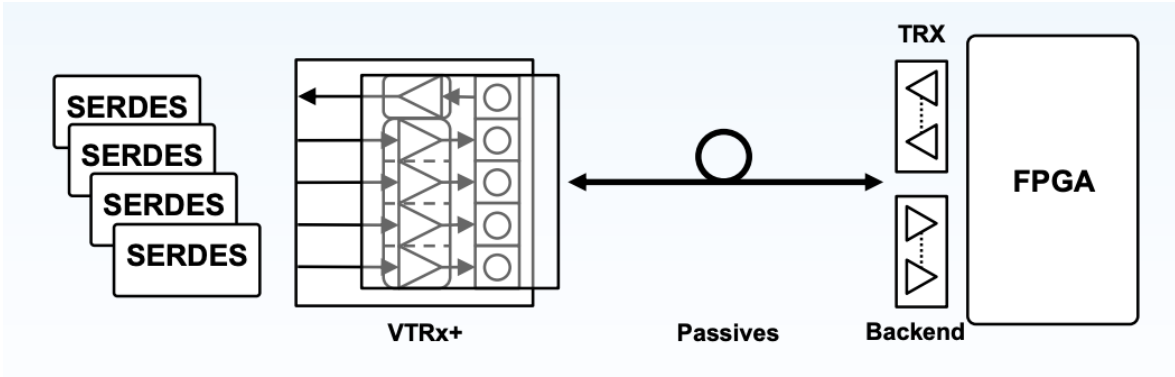
Implementation: Report utilization

Name	Registers (1799680)	CLB LUTs (899840)	LUT as Logic (899840)	LUT as Memory (449920)	LOOKAHEAD8 (112480)	SLICE (112480)	CLB Registers (1799680)	Block RAM Tile (967)	URAM (463)	Bonded IOB (692)	BUFGCE_DIV/MBUFGCE_DIV (40)	BUFG_PS/MBUFG_PS (12)
N felix_top	203420	122179	116949	5230	1267	30221	203420	186	174	192	1	2
axi_dbg_hub (axi_dbg_hub_axi_dbg_hub_0)	955	669	669	0	7	177	955	0	0	0	0	0
axi_noc (design_axi_noc_axi_noc_0)	0	0	0	0	0	0	0	0	0	0	0	0
busy0 (ttc_busy)	86	96	96	0	0	23	86	0	0	0	0	0
clk0 (clock_and_reset)	19	16	16	0	0	8	19	0	0	0	0	0
g_endpoints[0].crth0 (CRToHost__xdcDup__1)	8156	2480	2476	4	80	1157	8156	0.5	27	0	0	0
g_endpoints[0].decoding0 (decoding__xdcDup__1)	2358	1227	1039	188	16	359	2358	5	0	0	0	0
g_endpoints[0].encoding0 (encoding__xdcDup__1)	24428	21805	21805	0	0	4464	24428	42	0	0	0	0
g_endpoints[0].g_enableFromHost.crfh0 (CRFromHostAxis__xdcDup__1)	1754	1760	1344	416	4	361	1754	16	0	0	0	0
g_endpoints[0].g_EnableFullModeEmulator.emu0 (FullModeDataEmulator__xdcDup__1)	1314	1009	1009	0	16	234	1314	12	0	0	0	0
g_endpoints[0].g_EnableFullModeEmulator.fosel0 (axis_32_fanout_selector__xdcDup__1)	4	70	70	0	0	36	4	0	0	0	0	0
g_endpoints[0].pcie0 (wupper)	53896	26800	25004	1796	489	8631	53896	16	60	0	0	0
g_endpoints[0].resetmgr_fromhost (CRresetManager__xdcDup__1)	10	69	69	0	0	62	10	0	0	0	0	0
g_endpoints[0].resetmgr_tohost (CRresetManager__xdcDup__2)	10	11	11	0	0	4	10	0	0	0	0	0
g_endpoints[0].sync_fromhost_fifo_flush (xpm_cdc_sync_rst__parameterized2__79)	2	0	0	0	0	1	2	0	0	0	0	0
g_endpoints[0].sync_fromhost_reset (xpm_cdc_sync_rst__parameterized2__80)	2	0	0	0	0	1	2	0	0	0	0	0
g_endpoints[1].crth0 (CRToHost)	8156	2496	2492	4	80	1193	8156	0.5	27	0	0	0
g_endpoints[1].decoding0 (decoding)	2358	1236	1048	188	16	351	2358	5	0	0	0	0
g_endpoints[1].encoding0 (encoding)	24420	21827	21827	0	0	4440	24420	42	0	0	0	0
g_endpoints[1].g_enableFromHost.crfh0 (CRFromHostAxis)	1754	1753	1337	416	4	360	1754	16	0	0	0	0
g_endpoints[1].g_EnableFullModeEmulator.emu0 (FullModeDataEmulator)	1314	990	990	0	16	245	1314	12	0	0	0	0
g_endpoints[1].g_EnableFullModeEmulator.fosel0 (axis_32_fanout_selector)	4	68	68	0	0	35	4	0	0	0	0	0
g_endpoints[1].pcie0 (wupper__parameterized0)	53645	26532	24736	1796	489	8855	53645	16	60	0	0	0
g_endpoints[1].resetmgr_fromhost (CRresetManager__xdcDup__3)	10	69	69	0	0	62	10	0	0	0	0	0
g_endpoints[1].resetmgr_tohost (CRresetManager)	10	11	11	0	0	4	10	0	0	0	0	0
g_endpoints[1].sync_fromhost_fifo_flush (xpm_cdc_sync_rst__parameterized2__106)	2	0	0	0	0	1	2	0	0	0	0	0
g_endpoints[1].sync_fromhost_reset (xpm_cdc_sync_rst__parameterized2)	2	0	0	0	0	1	2	0	0	0	0	0
hk0 (housekeeping_module)	3554	2702	2653	49	12	597	3554	3	0	0	0	2
linkwrapper0 (link_wrapper)	5613	2940	2936	4	10	1142	5613	0	0	0	0	0
proc_sys_reset (proc_sys_reset_proc_sys_reset_0)	35	20	19	1	0	6	35	0	0	0	0	0
TTCLTI.ltittc0 (ltittc_wrapper)	9549	5738	5370	368	28	1437	9549	0	0	0	1	0

Installation of a Felix-182 Card @ APE Lab

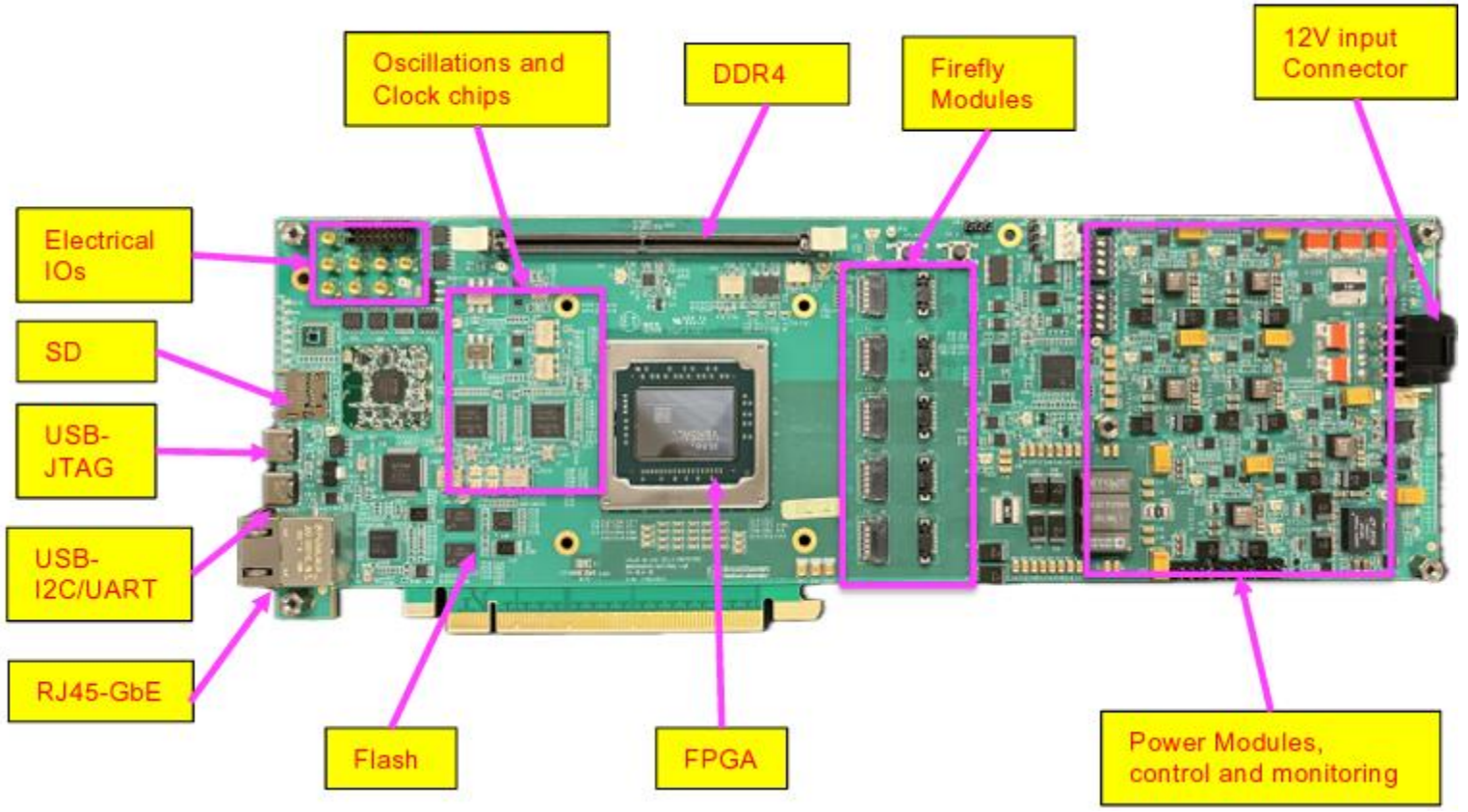
```
lonardo@apestation0 x86_64-el9-gcc13-opt]$  bin/flx-init
2025-05-14 18:06:05 Opening card 0 (device 0)...
2025-05-14 18:06:05 Card type: FLX-182
2025-05-14 18:06:05 Firmware : FULL
2025-05-14 18:06:05 Clock    : Local
2025-05-14 18:06:05 FLX soft reset
2025-05-14 18:06:05 SI5345A hard reset
2025-05-14 18:06:07 ### SI5345A part nr: read 0xFF, expected 0x45; device not
present/accessible?
2025-05-14 18:06:07 Found SI5345A_BETA
…
2025-05-14 18:06:12 Links soft reset
2025-05-14 18:06:12 Setting up links...
2025-05-14 18:06:19 Links set up
2025-05-14 18:06:19 WARNING: 4 channels not aligned
2025-05-14 18:06:19 Resetting FireFly devices...
2025-05-14 18:06:19 FIREFLY_TX1: PartNr="CERNBY12040213M ",
SerNr="UA2042001A"
2025-05-14 18:06:19 FIREFLY_RX1: PartNr="CRRNBY12040213M ",
SerNr="UA2042001A"
2025-05-14 18:06:20 FIREFLY_TX2: PartNr="CERNBY12040213M ",
SerNr="UA2042001F"
2025-05-14 18:06:20 FIREFLY_RX2: PartNr="CRRNBY12040213M ",
SerNr="UA2042001F"
2025-05-14 18:06:20 FIREFLY_TXRX: PartNr="B042804005170",
SerNr="UA231005DX"
2025-05-14 18:06:20   WARNING: CDR not changed, part expected "B042504005170"
2025-05-14 18:06:20 FireFly done
…
2025-05-14 18:06:20 INA226 configured
2025-05-14 18:06:20 Initializing LTI...
2025-05-14 18:06:20 LTI alignment: NO
```





Backup Slides

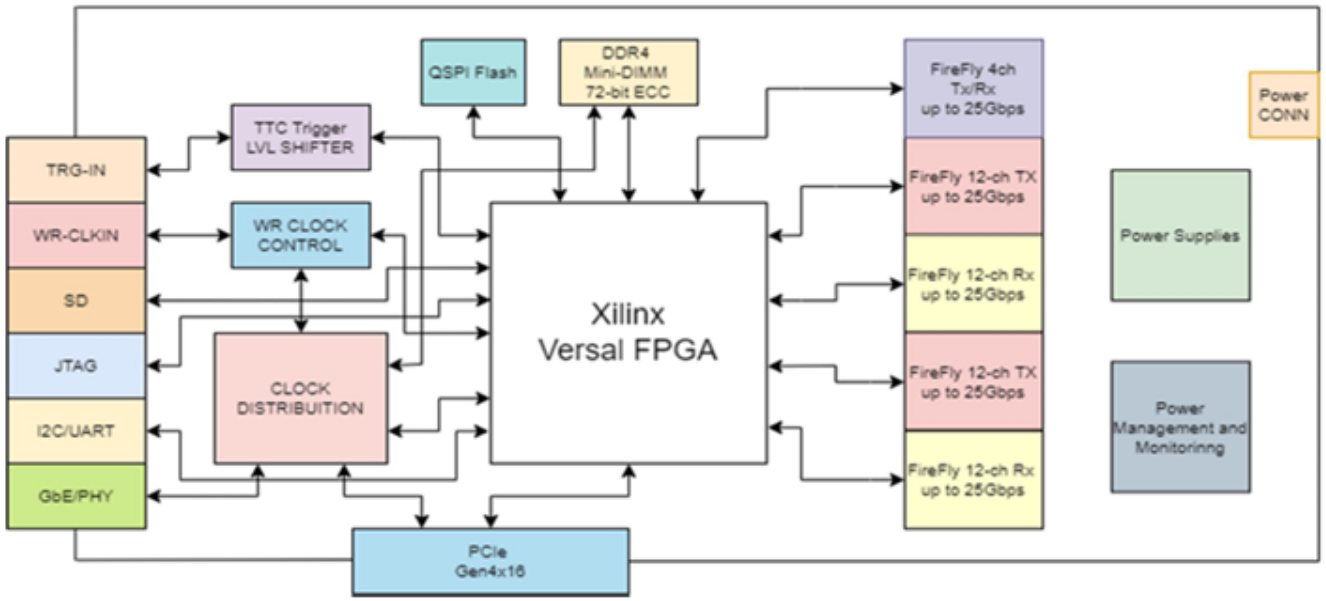
FLX-182B


Oscillations and Clock chips
DDR4
Firefly Modules
12V input Connector
Electrical IOs
SD
USB-JTAG
USB-I2C/UART
RJ45-GbE
Flash
FPGA
Power Modules, control and monitoring

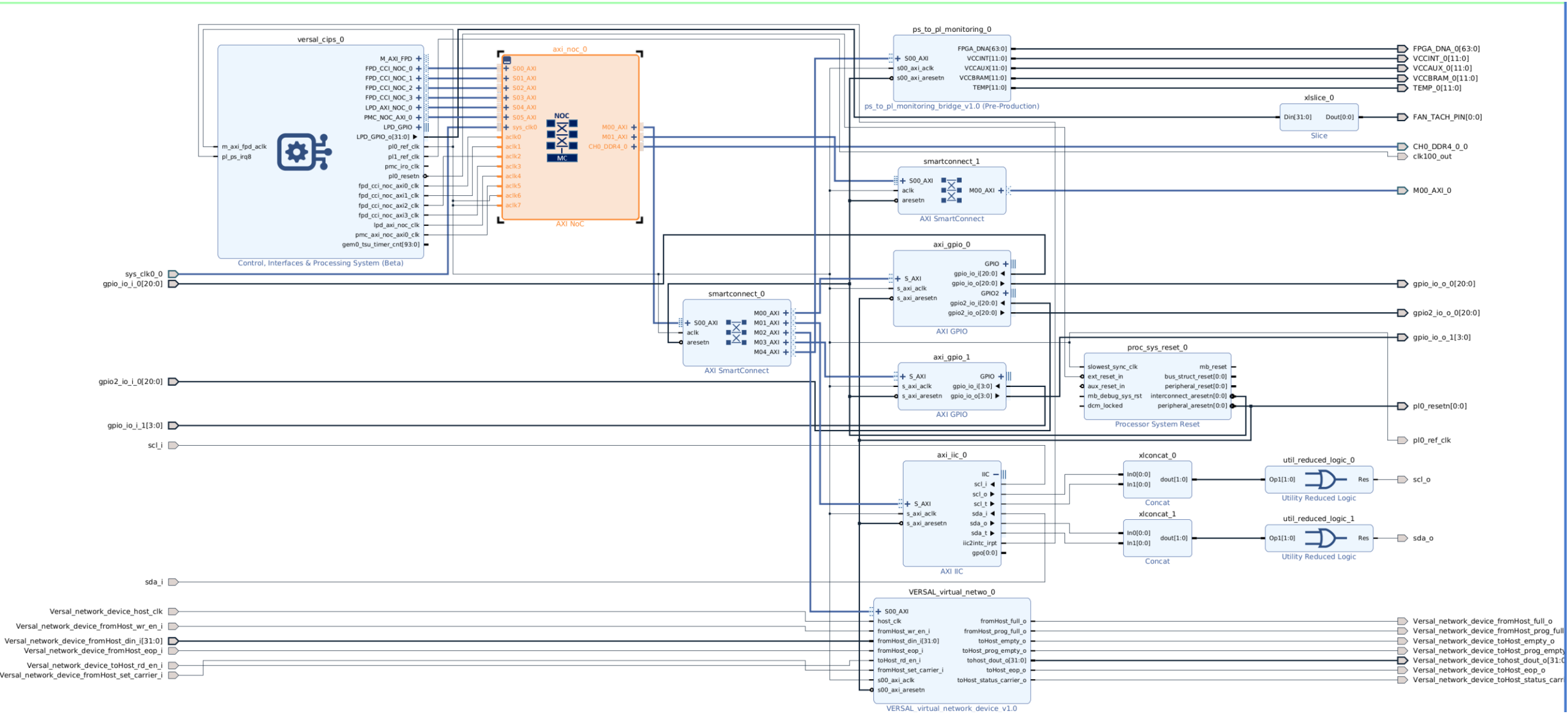
FLX-182 Features

Main features of FLX-182

- XCVM1802 production chip
- PCIe Gen4 x16: PL and CPM compatible
  - PL: Hard PCIe endpoint like in earlier FPGA series
  - CPM: Hard PCIe endpoint integrated in SoC, data transferred over NoC
- 24 FireFly links with 3 possible configurations
  - 24 links up to 25 Gb/s
  - 24 links up to 10 Gb/s (CERN-B FireFly)
  - 12 links up to 25 Gb/s + 12 links up to 10 Gb/s
- 4 FireFly links with 2 possible configurations with 14 or 25 Gb/s FireFly TRx
  - LTI interface
  - 100 GbE
- 1 DDR4 Mini-UDIMM
- USB-JTAG/USB-UART
- SD3.0/QSPI
- GbE



Block diagram of FLX-182


versal_cips_0
M_AXI_FPD
FPD_CCI_NOC_0
FPD_CCI_NOC_1
FPD_CCI_NOC_2
FPD_CCI_NOC_3
LPD_AXI_NOC_0
PMC_NOC_AXI_0
LPD_GPIO
LPD_GPIO_o[31:0]
pl0_ref_clk
pl1_ref_clk
pmc_iro_clk
pl0_resetn
fpd_cci_noc_axi0_clk
fpd_cci_noc_axi1_clk
fpd_cci_noc_axi2_clk
fpd_cci_noc_axi3_clk
lpd_axi_noc_clk
pmc_axi_noc_axi0_clk
gem0_tsu_timer_cnt[93:0]
m_axi_fpd_aclk
pl_ps_irq8
Control, Interfaces & Processing System (Beta)
axi_noc_0
S00_AXI
S01_AXI
S02_AXI
S03_AXI
S04_AXI
S05_AXI
sys_clk0
aclk0
aclk1
aclk2
aclk3
aclk4
aclk5
aclk6
aclk7
NOC
MC
M00_AXI
M01_AXI
CH0_DDR4_0
AXI NoC
ps_to_pl_monitoring_0
S00_AXI
s00_axi_aclk
s00_axi_aresetn
FPGA_DNA[63:0]
VCCINT[11:0]
VCCAUX[11:0]
VCCBRAM[11:0]
TEMP[11:0]
ps_to_pl_monitoring_bridge_v1.0 (Pre-Production)
xlslice_0
Din[31:0]
Dout[0:0]
Slice
smartconnect_1
S00_AXI
aclk
aresetn
M00_AXI
AXI SmartConnect
smartconnect_0
S00_AXI
aclk
aresetn
M00_AXI
M01_AXI
M02_AXI
M03_AXI
M04_AXI
AXI SmartConnect
axi_gpio_0
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
gpio_io_i[20:0]
gpio_io_o[20:0]
GPIO2
gpio2_io_i[20:0]
gpio2_io_o[20:0]
AXI GPIO
axi_gpio_1
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
gpio_io_i[3:0]
gpio_io_o[3:0]
AXI GPIO
proc_sys_reset_0
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
axi_iic_0
S_AXI
s_axi_aclk
s_axi_aresetn
IIC
scl_i
scl_o
scl_t
sda_i
sda_o
sda_t
iic2intc_irpt
gpo[0:0]
AXI IIC
xlconcat_0
In0[0:0]
In1[0:0]
dout[1:0]
Concat
xlconcat_1
In0[0:0]
In1[0:0]
dout[1:0]
Concat
util_reduced_logic_0
Op1[1:0]
Res
Utility Reduced Logic
util_reduced_logic_1
Op1[1:0]
Res
Utility Reduced Logic
VERSAL_virtual_netwo_0
S00_AXI
host_clk
fromHost_wr_en_i
fromHost_din_i[31:0]
fromHost_eop_i
toHost_rd_en_i
fromHost_set_carrier_i
s00_axi_aclk
s00_axi_aresetn
fromHost_full_o
fromHost_prog_full_o
toHost_empty_o
toHost_prog_empty_o
tohost_dout_o[31:0]
toHost_eop_o
toHost_status_carrier_o
VERSAL_virtual_network_device_v1.0
sys_clk0_0
gpio_io_i_0[20:0]
gpio2_io_i_0[20:0]
gpio_io_i_1[3:0]
scl_i
sda_i
Versal_network_device_host_clk
Versal_network_device_fromHost_wr_en_i
Versal_network_device_fromHost_din_i[31:0]
Versal_network_device_fromHost_eop_i
Versal_network_device_toHost_rd_en_i
Versal_network_device_fromHost_set_carrier_i
FPGA_DNA_0[63:0]
VCCINT_0[11:0]
VCCAUX_0[11:0]
VCCBRAM_0[11:0]
TEMP_0[11:0]
FAN_TACH_PIN[0:0]
CH0_DDR4_0_0
clk100_out
M00_AXI_0
gpio_io_o_0[20:0]
gpio2_io_o_0[20:0]
gpio_io_o_1[3:0]
pl0_resetn[0:0]
pl0_ref_clk
scl_o
sda_o
Versal_network_device_fromHost_full_o
Versal_network_device_fromHost_prog_full
Versal_network_device_toHost_empty_o
Versal_network_device_toHost_prog_empty
Versal_network_device_tohost_dout_o[31:0]
Versal_network_device_toHost_eop_o
Versal_network_device_toHost_status_carr