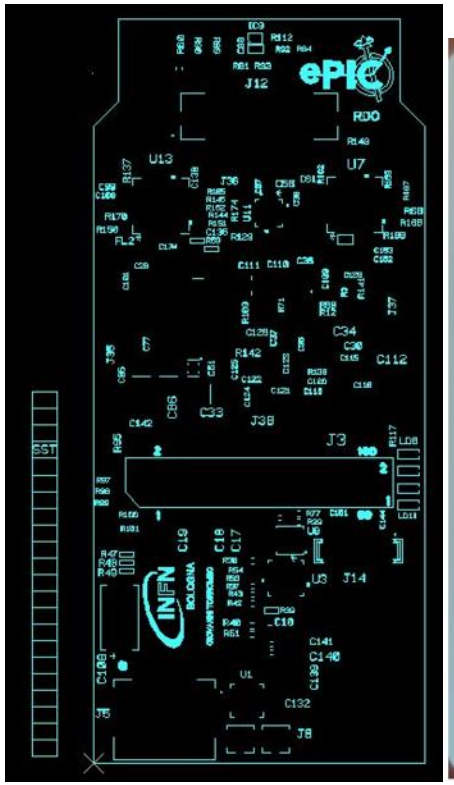
# dRICH RDO project planning





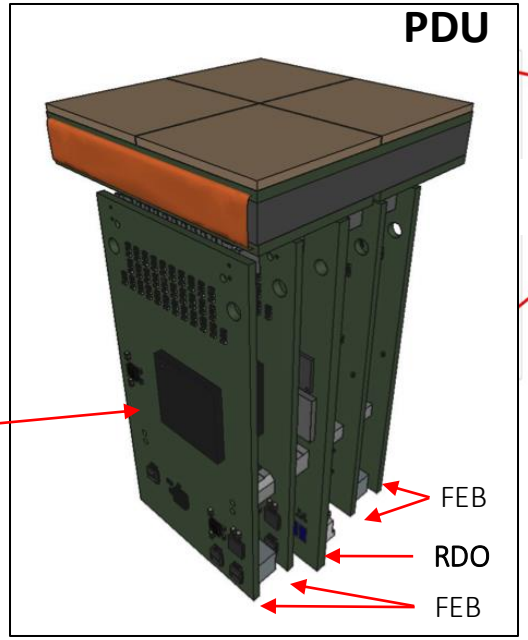
P. Antonioli, D. Falchieri, S. Geminiani, L. Rignanese, G. Torromeo

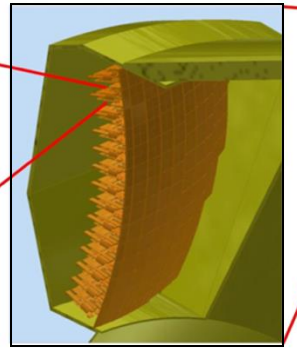
(INFN Bologna)

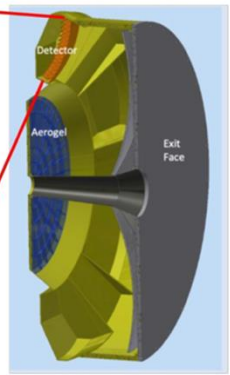
dRICH DAQ kick-off meeting
Zoom, 5 September 2025

# dRICH RDO re-cap in two slides (I)

dRICH status: M. Contalbrigo at April 2025 PID Review
dRICH SiPM status: R. Preghenella at April 2025 PID Review






RDO is inside dRICH **PDU** photo detection unit

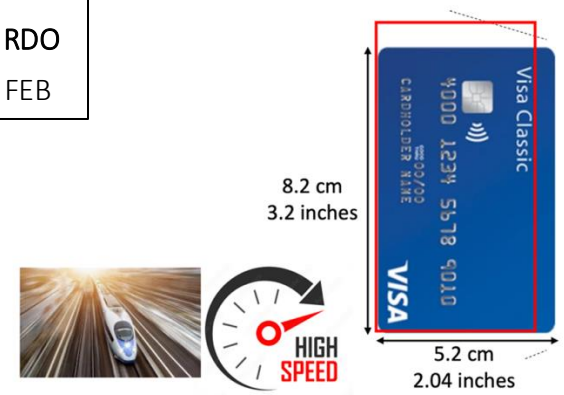
dRICH RDO **requirements** (from DAQ PDR review June 2024)

- **space**: 40 x 90 mm area
- RDO not accessible: **remote firmware upgrade** must be possible

- RDO FPGA need **high speed** (“high performance”) 120 I/O pins to implement ALCOR bus towards FEBs
- RDO connector need high speed specs. and (minimum) 60 I/O pins each

- RDO must implement clean **clock** multiplication (ALCOR@394 MHz, EIC clock 98.5 MHz)
- RDO must reconstruct clock via optical link
- RDO must produce clean clock (minimize jitter)

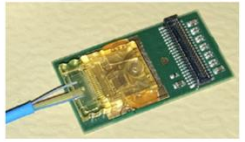
- **opt. tranceiver** must minimize space/power consumption + “rad hard” and bandwitdh up to 10 Gbps







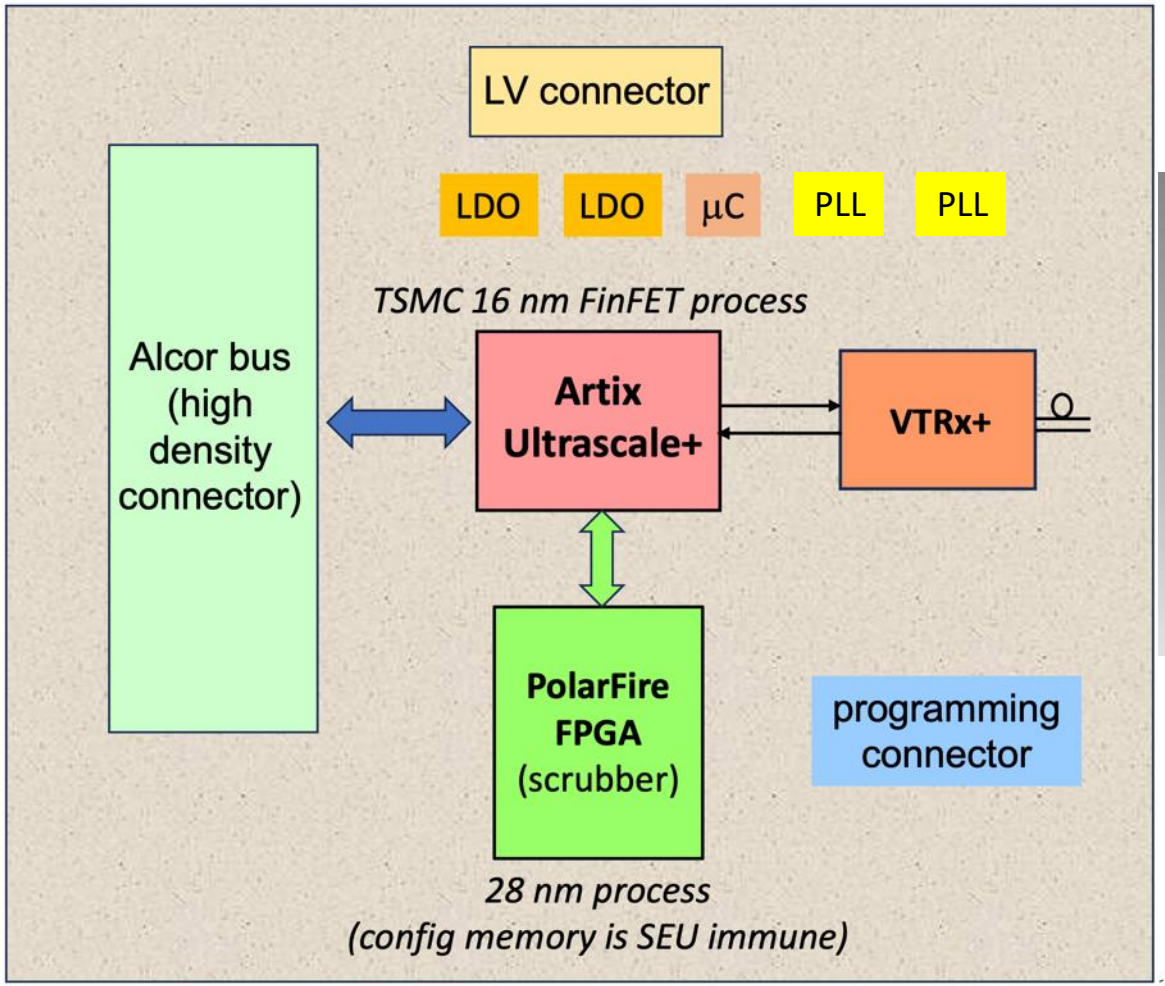


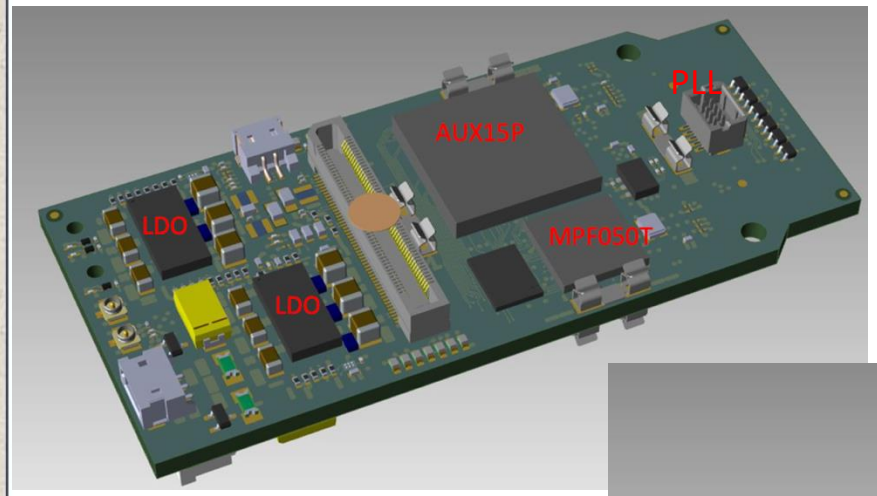
# dRICH RDO re-cap in two slides (II)

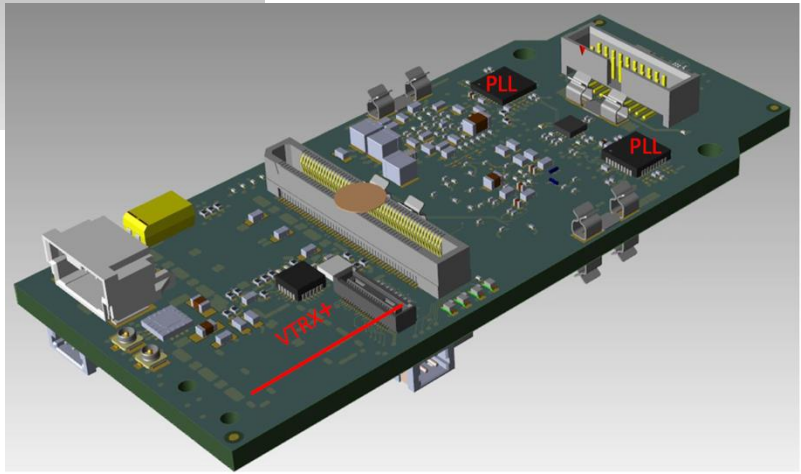
**Main design choices**

- a performing RAM-based FPGA + scrubbing implemented via a Flash-based FPGA
- devoted PLLs to manage clock (SkyWorks 5319 / 5326)
- VTRX+ as optical tranceiver
- a small uC acts as RDO power manager

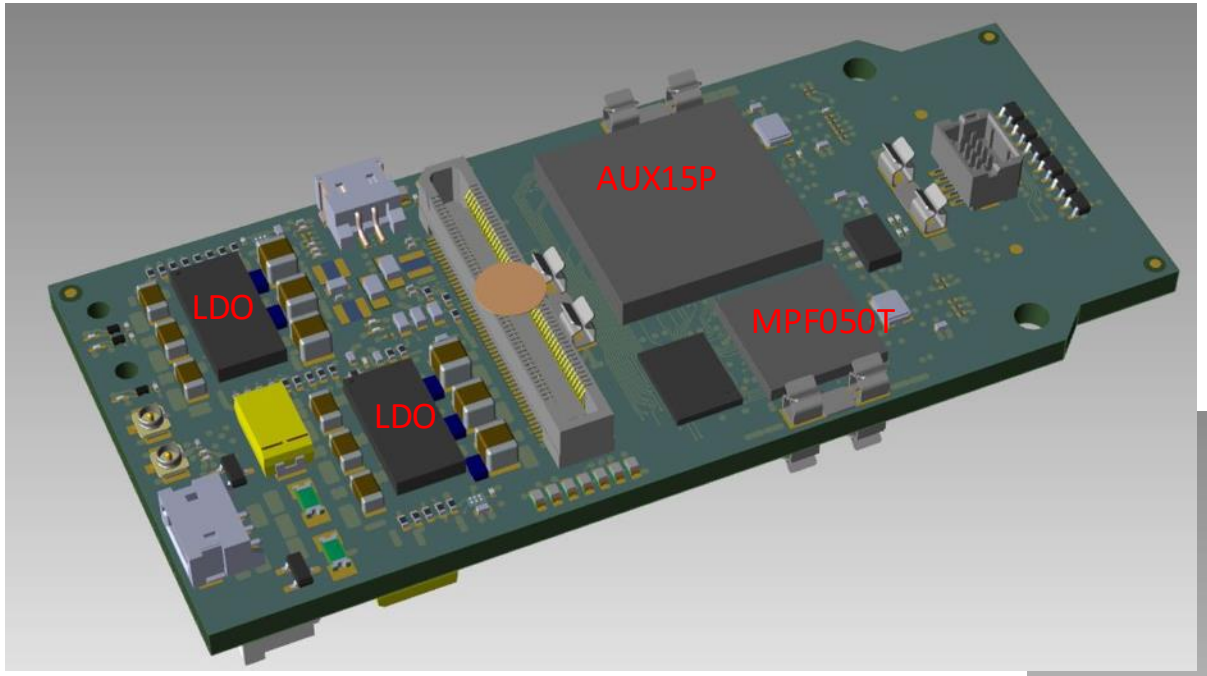



Long and painful elaboration of exact RDO specifications
+ components selection + schematics preparation + layout time +
production time: design started January 2024

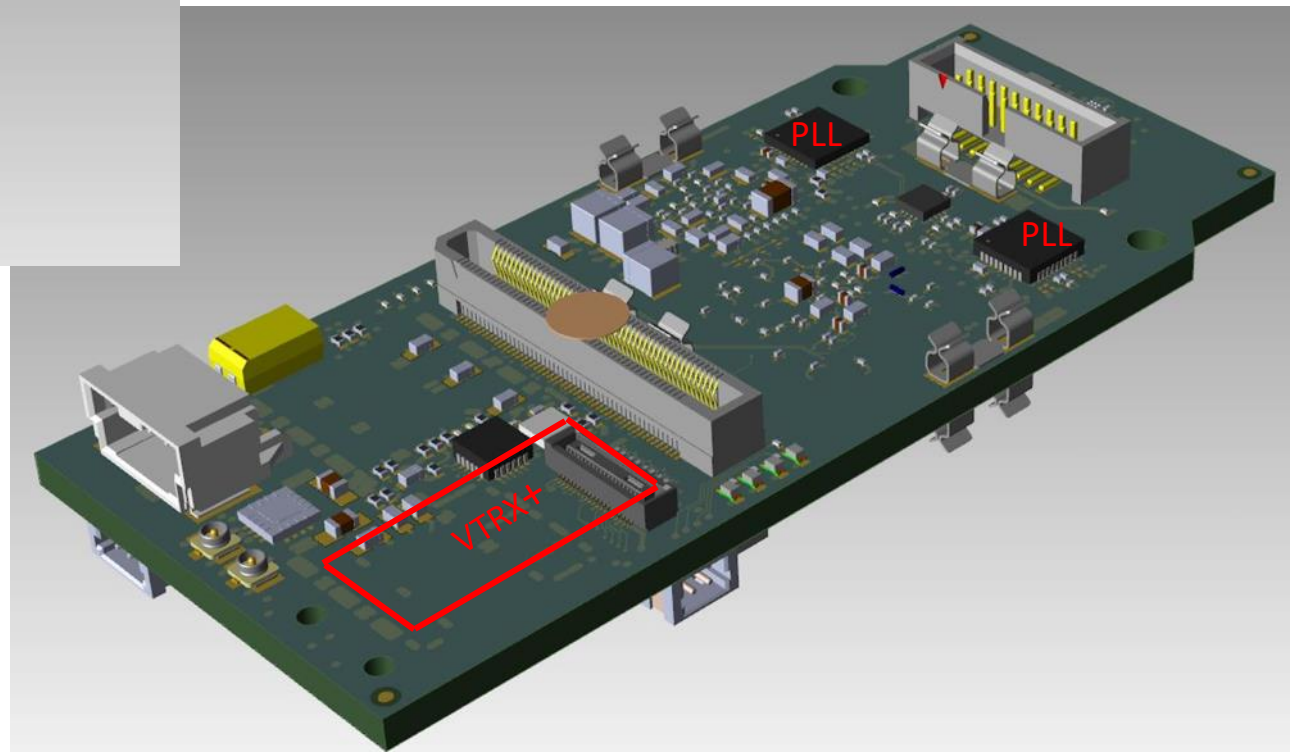


# dRICH RDO: layout




Complex and small card, 16 layers layout




A small uC (ATTiny 417) acts as RDO power manager controlling LDOs

# RDO project: a little bit of history

dRICH is somehow special because:
- it has been the first group saying “we neeed our own RDO”
- we had almost immediately (2021) an ASIC “up and running”
- we have, IMHO, much more experience on radiation tolerance test than other groups in ePIC (ALICE background)
- we have been the first group bringing to ePIC attention VTRX+
- we have been the first group desperately asking for a RDO protocol definition

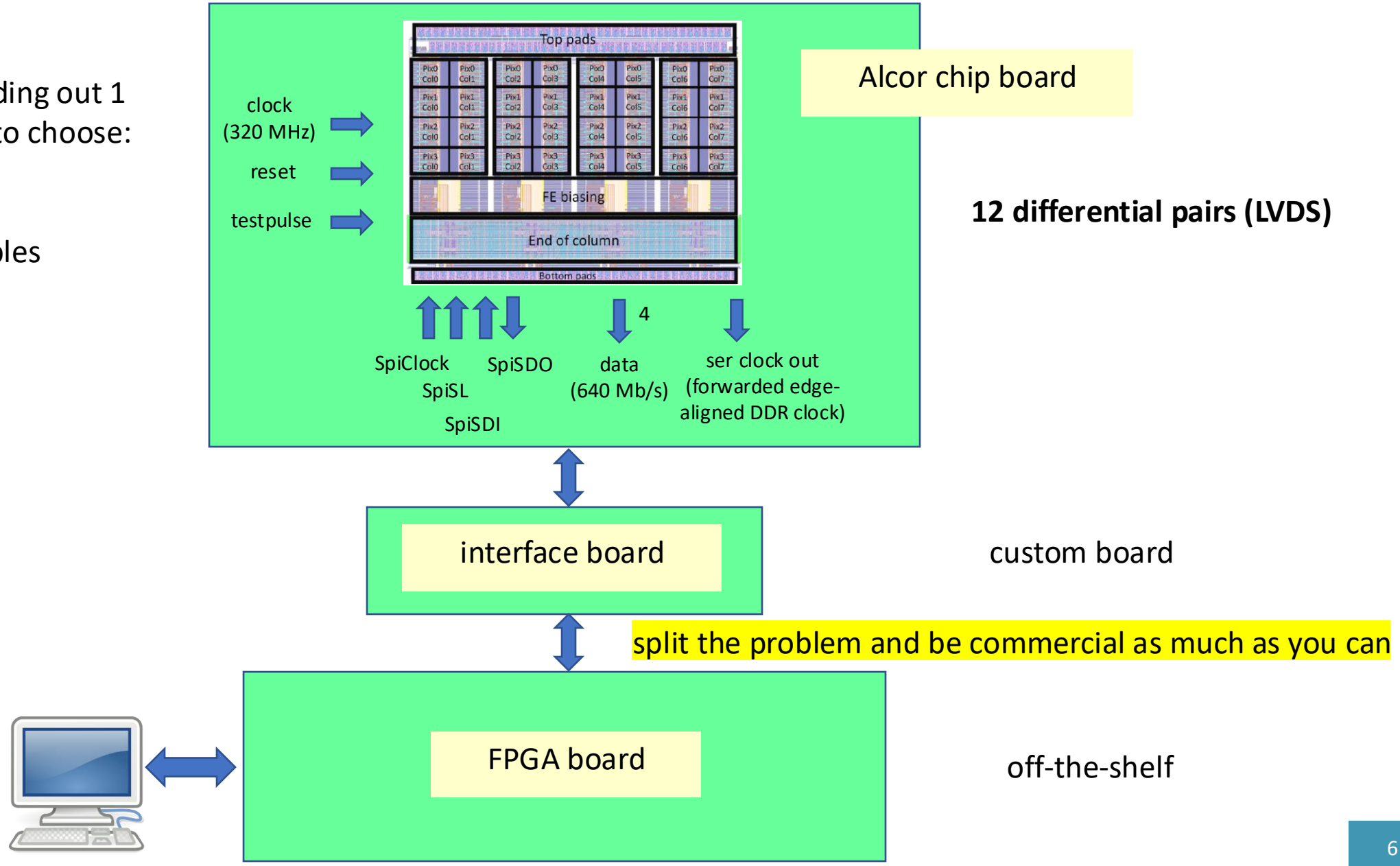
Key point: nowadays many ePIC sub-detectors are using VTRX+/lpGBT. We evolved our design differently. Ex-post we might have explored that option too. Few years ago we were working under primary spec that we would have operated the link re-building at 100 MHz clock, excluding CERN-like (lpGBT, GBT, …) protocols.

In practice:
- we started brainstorming on how to design RDO in late 2022, but we initiated requirements & specs definition only in late 2023
- actual design started in January 2024, with some critical specs changed in March 2024. In June 2024 we were still working on schematics

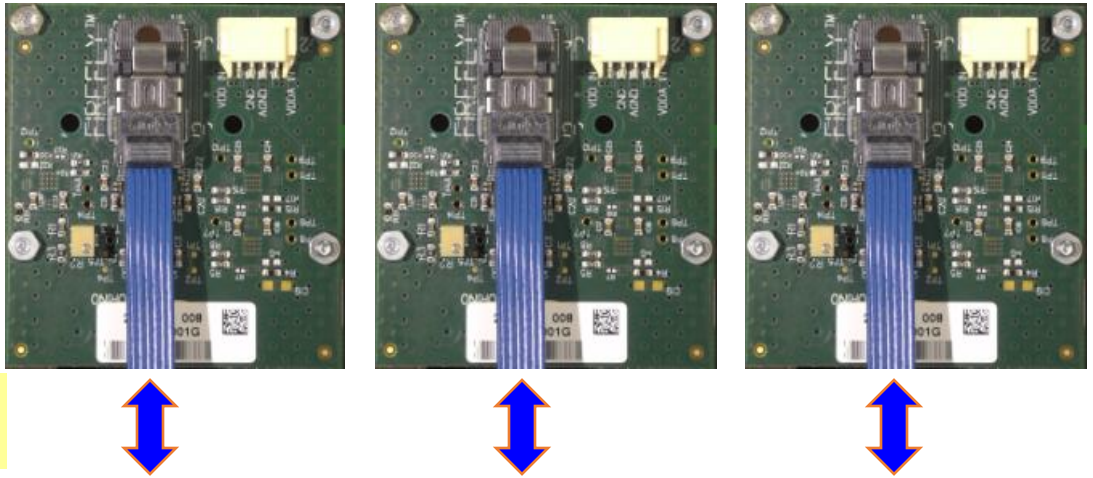
# R&D toward RDO: reading the ASIC (I)

We started in 2021 reading out 1 Alcor chip, we needed to choose:

- FPGA board
- interface board
- interconnection cables

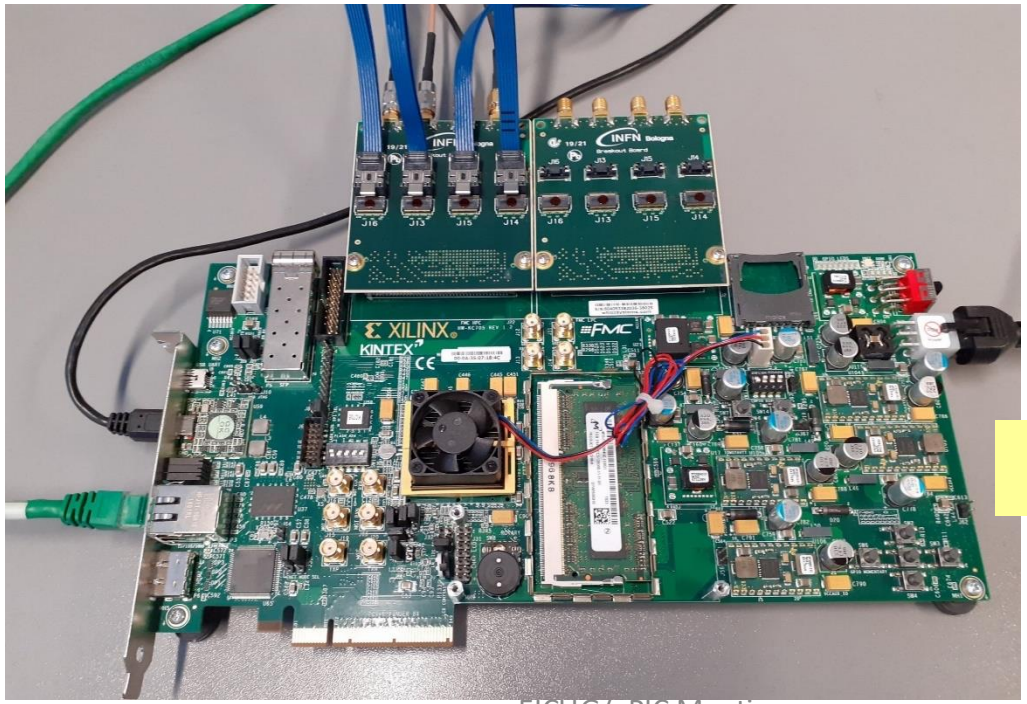


# R&D toward RDO: reading the ASIC (II)



Alcor front end boards

Samtec Firefly cables




custom FMC→ Firefly breakout board

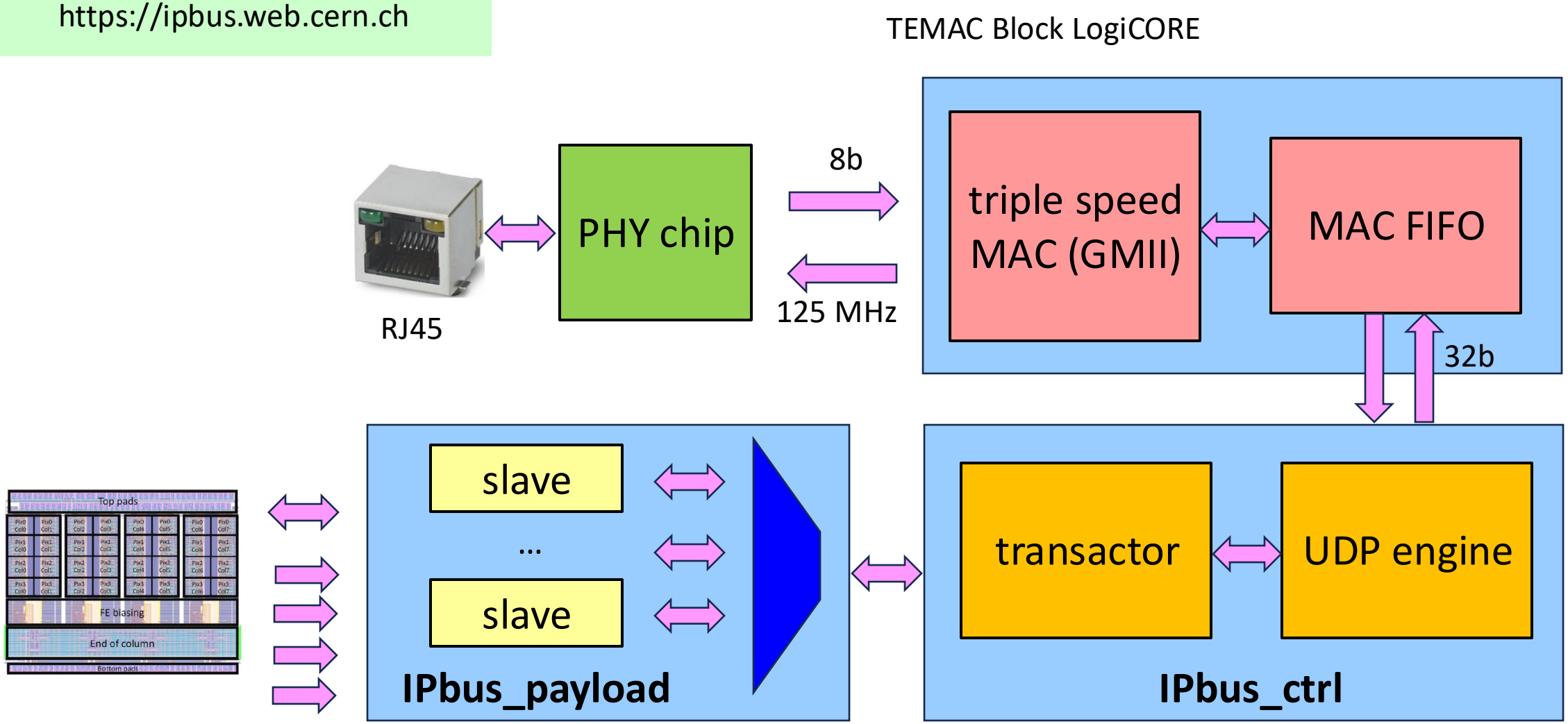
1 Gb ETH

CERN IPbus

FPGA board KC705

# initial RDO R&D: link protocol

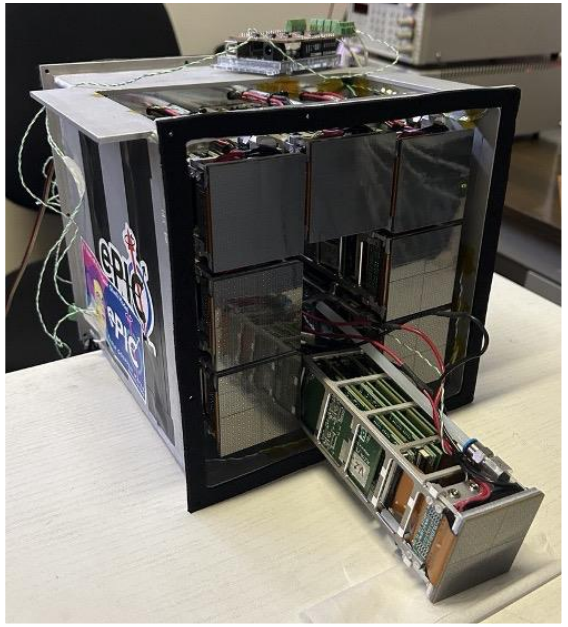
https://ipbus.web.cern.ch

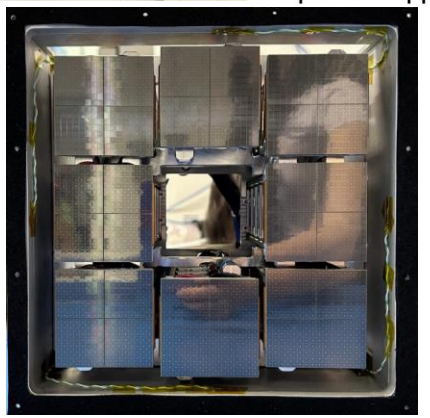


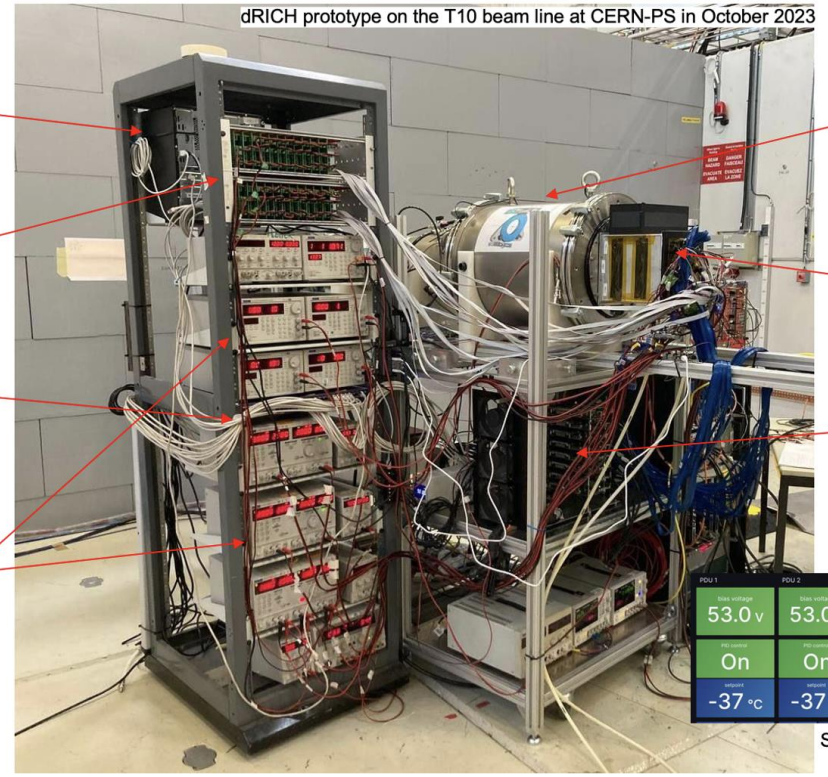

The firmware uses the CERN IPbus UDP-based core, which allows one to easily exploit the Ethernet port for receiving/transmitting data (and using easily cheap network infrastructure)

an easy ready-to-start protocol was key to start fast

# scale up to a test beam up to 2 kchannels








11 KC705 FPGA boards in parallel ➔ 64 AlCOR chips ➔2048 SiPMs

next step is bringing readout inside the PDU (RDO comes after)

# key point

we bypassed all ePIC discussions about protocols and we selected an “easy” one: IPBUS plus we distribute clock independently

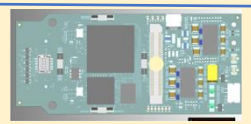
Phase 1 → operate RDO with IPBUS + external clock
Phase 2 → move to a streaming protocol/clock reconstruction FELIX supported (FULL? → see later)

# RDO project: the last 14 months

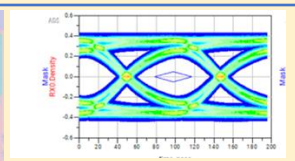
PDR — PDR

June 2024 — Dec — Mar — Jun — Sep 2025

design finalization

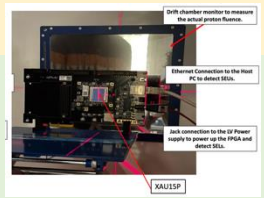


PCB layout / verification — July 24



PCB production

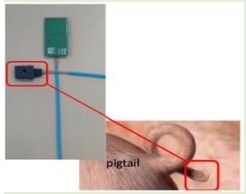
prototypes validation




irradiation tests
of RDO components

firmware porting using ALINX AUX15P
analysis of RDO power consumption

VTRX+ tests (light leakage)



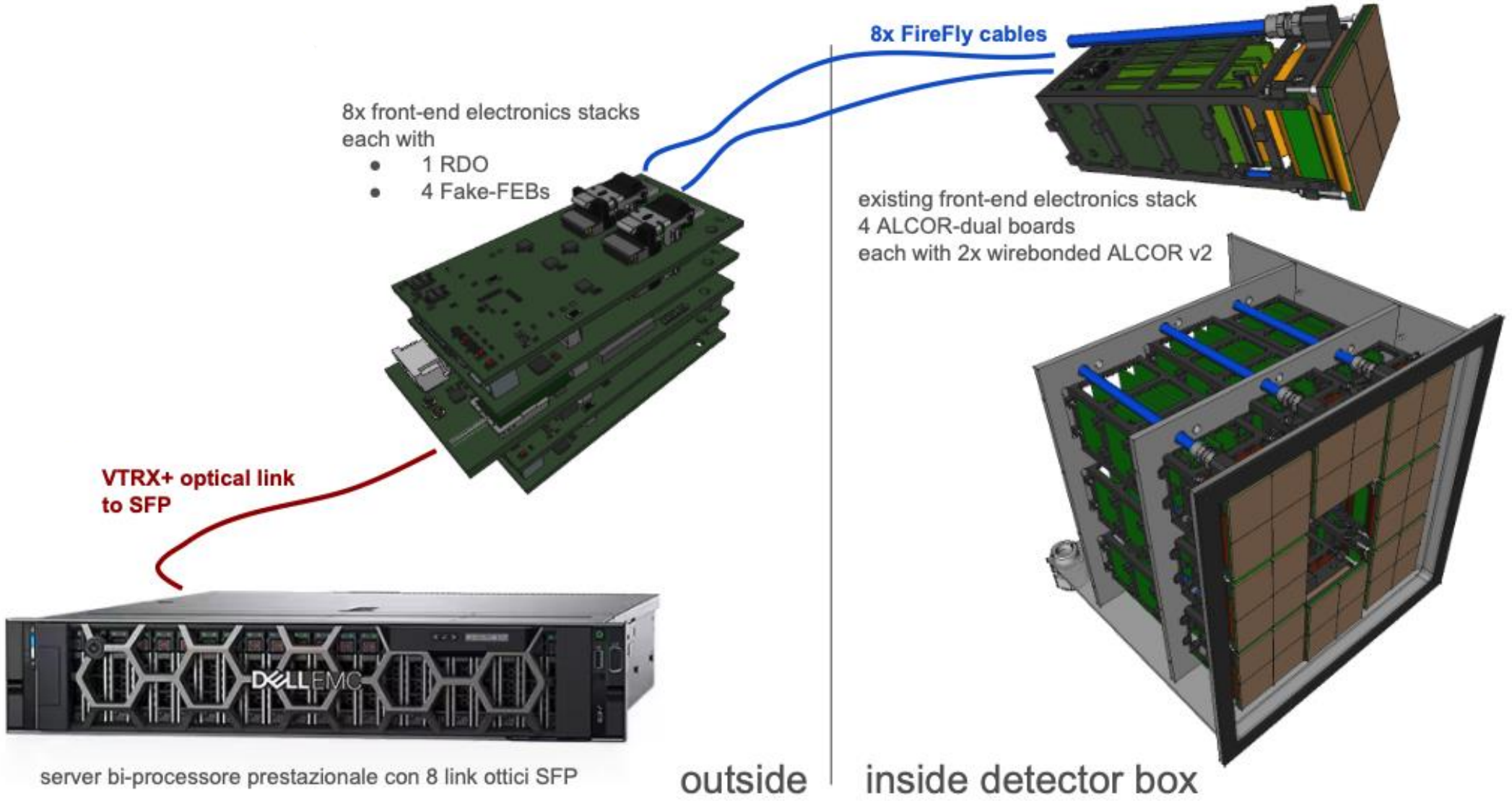

back-end DAQ redesign (DAM)

definition of VTRX+
pigtail length

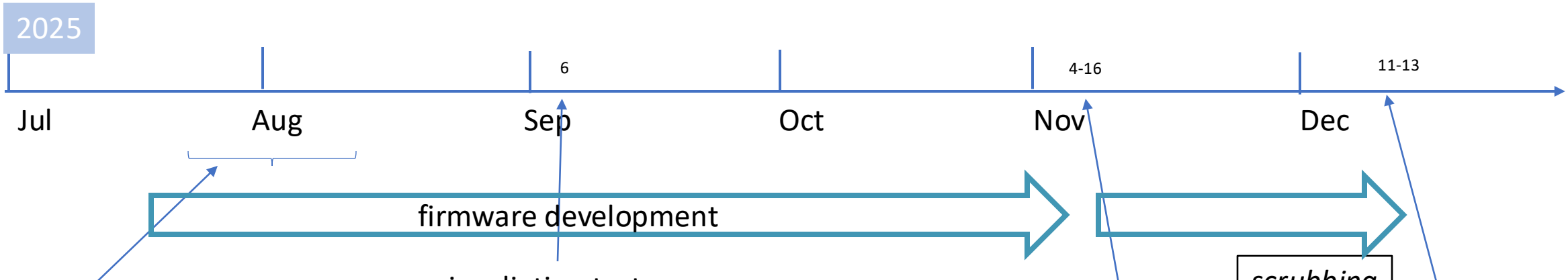
For details see yesterday presentation at PDR

# RDO setup for 2025 test beam (Nov. 2025)

- we use IPBUS protocol over VTRX+ with SFP NIC cards on receiving end
- ”fake-FEB” (ALCOR v2.1 adaptor) : two FireFly connectors to reach existing FEB (with 2 ALCOR v2.1)



# Plannning and validation tests (2025)




first "validation" to
give green light for other 8 RDOs
mounting:
- *mechanics*
- *power-up*
- *basic programming*
(details)

*ALCOR conf/readout with fake-FEB + IPBUS DAQ (possibly "streaming")*
(details)

We will be extremely busy until the end of the year

# Next steps/challenges for RDO

During 2026 we need:

- full validation of current prototypes
- fix any mistake found


- design adaptations due to integration challenges that may arise (cooling, space, FPGA resources, ...)

- prove communication with DAM (implementing a FELIX-supported comm. protocol)

# Plannning and validation tests (2026)

2026

Jan Feb Mar Apr May Jun Jul Aug Sep Oct Nov Dec

firmware / software development

remote programming
clock reconstruction – FELIX-supported comm. protocol (FULL with GBT on host)
details

second irradiation
test “full RDO”
@Trento

last test beam
readout full PDU
(RDO+ALCOR64)

irradiation tests:
full PDU @CHARM

[ details on 2026 irradiation tests ]

RDO communication tests with DAM

**Developing a RDO testbed to test RDO production (preparing for 2027 RDO production!)** [details]

requirements | specs | design | layout and production | validation

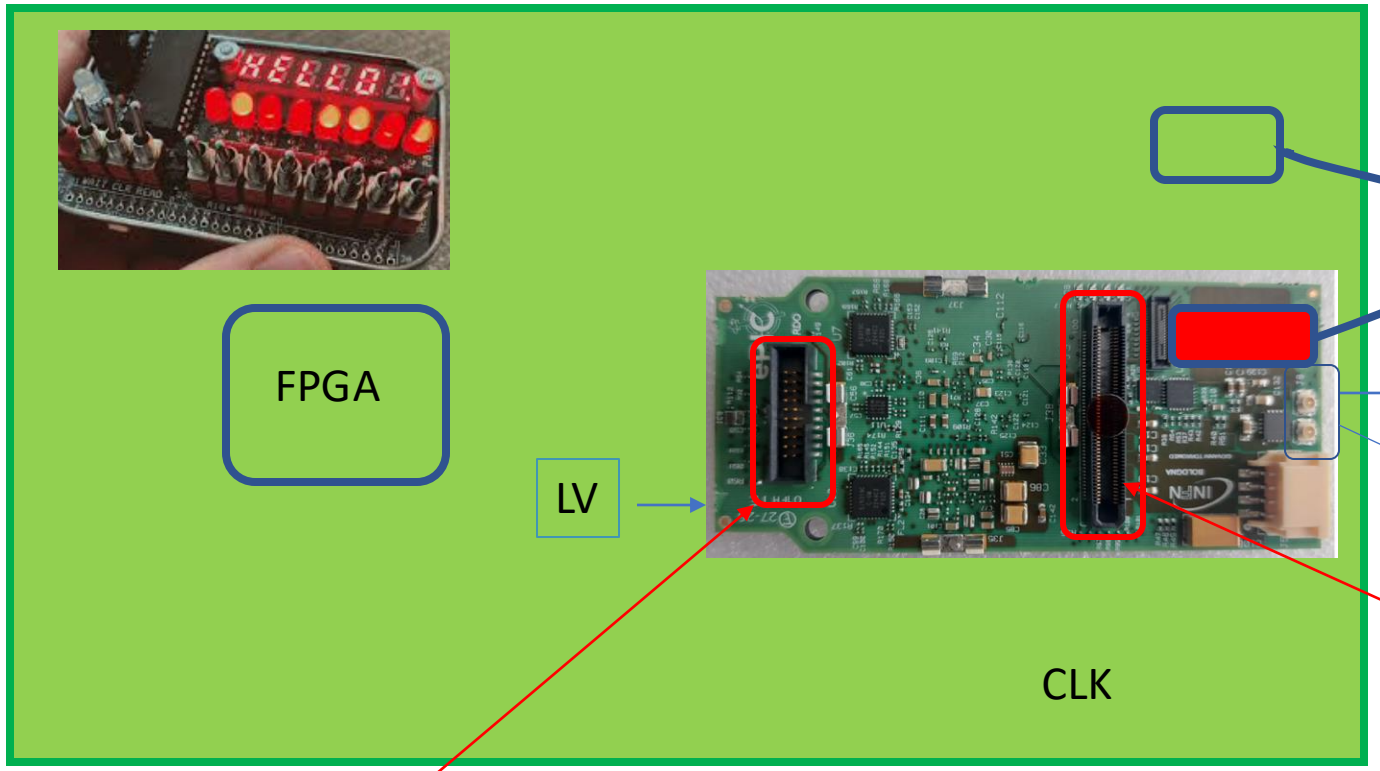
Details in backup

# RDO production: a RDO testbed for 1500 cards

preparing for RDO production in 2027 we will invest time preparing carefully budgeting (currently cost foreseen 680 k€ + VAT) and a **RDO testbed card** to test thoroughly, quickly and effectively the 1500 boards (and load the firmware)

display + switches to run specific tests

Request → **15 k€ (apparati)**




**Basic idea:**
the TB FPGA FW verifies all RDO I/Os are ok before moving to
a) VTRX+ installation – link check
b) testing with FEB
c) testing in a PDU

RDO is plugged on TB using ALCOR BUS botttom connector

EXT CLK (UFL to SMA)

a flat cable connected to (ALCOR BUS top connection)

a flat cable connected for FPGAs/atTiny programming

# The RDO-core team

**INFN BO dRICH RDO core team**:

- P. Antonioli, physicist
- D. Falchieri, electronic engineer
- S. Geminiani, PhD student (enrolled 1 Nov. 2024)
- L. Rignanese, electronic engineer
- G. Torromeo, electronic technician

- Pietro → coordination, backend software (currently using C++/Python IPBUS in future… through PCI → FELIX → RDO). GBT and radiation tolerance tests qualification from ALICE
- Davide → firmware coordinator (massive DAQ fw expertise … ALICE/ARCADIA/HYDRA/.. + all the things I don't know)
- Sandro → firmware (+ software) + he will write a PhD thesis about RDO
- Luigi → uController sw/fw + radiation tests (+ a lot of expertise on electronics.. if you need a component doing something… he knows)
- Giovanni → schematics, electrical design, link with ext. company for layout, layout designer

Obviously a lot of joint work with INFN-TO (ALCOR), other INFN-BO members (SiPM, PDU integration), INFN-FE

# A Work Breakdown Structure for RDO

This has to be done first under IPBUS, no inclusion of DAM link
We discuss the WBS of that crucial inclusion at the end of the meeting

| Software | Firmware | | Hardware |
|---|---|---|---|
| • ALCOR conf/readout<br>• Sensors monitoring<br>• Scrubbing mon.<br>• Remote programming | • ALCOR conf/readout<br>• Sensors monitoring<br>• PolarFire – Artix bus<br>• Scrubbing<br>• Remote programming<br>• Radmon | • Power Management<br>• uC sw/fw<br>• protection including<br>• power on/off safe sequences | • VTRX+ “cage”<br>• cooling<br>• fix mistakes → pre-prod<br>• RDO testbed<br>• integration with PDU |

# RDO next steps for go for production (8 RDOs)

1. Mechanical pairing with fake-FEB
2. Power-up : 2.5 / 1.4 jumper to avoid power to other sections
3. Prg uC via external connector
4. Power-up with uC (post-programming uC): check Vout LDO
5. Prg Artix via external connector
6. Prg Polarfire via external connector
7. Prg Artix → SkyWorks  (programming 125 MHz of Si5319)
8. Check consumptions
9. Check  UFL I/Os
10. Link IPBUS via VTRX+  [MT-MPO adapter + "polipo"]
11. Prg ALCOR via fake-FEB (via IPBUS → VTRX+)
12. ALCOR readout (via IPBUS → VTRX+)

Note: we can't test everything before give the "go" for next 8 RDOs...

# Backup

# RDO next steps for test beam

1. External clock processed by SI5326  (note: we need 16 SMA-UFL cables)
2. Readout of all I2C sensors
3. I2C programming of regulators on fake-FEB
4. Manage different IP (without jumpers)
5. Cooling ?!
6. A mini rack: 8 RDO + fake-feb on both sides etc...

Optional (bonus):

1. IPBUS + UDP streaming

# RDO next steps for test @TIFPA

1. Writing QSPI Flash via SPI (writing via JTAG)
2. Scrubbing
3. Comunication between PolarFire and Artix
4. Current monitor via uC
5. Communication between uC and ARTIX

Optional (bonus):

1. Polarfire program ARTIX at boot
2. QSPI Flash writing via IPBUS (Remote Programming!)
3. During the test: one fake-feb connected and we read 2 ALCOR32? (note: ALCOR not exposed to radiation)

# RDO next steps towards full ePIC DAQ

- Check noise from charged pump
- Check noise (light) from VTRX+ / engineer “shield”
- Link EIC → clock reconstruction (need project input)
- Clock at 394 MHz/ ALCOR@394 MHz
- Polarfire program Artix at boot
- Remote programming (writing PolarFire via VTRX+)
- Remote programming (writing Flash memory via VTRX+)
- IPBUS —> EIC link over VC709/707
- Data format // buffering // “frame”
- Test with ALCOR64 + FEB
- Test  with FELIX
- test in magnetic field (PDU)
- PDU in detector box etc…

TB2026: dismount leds!!

- **pre-production** during 2026 (if we don't need it before) “RDO26”
- test card for testing RDO