

SLBP – WP1



Comments to WP1

- *Come valutare lo stato del progresso? E il successo o insuccesso?*
→ Need milestones (**MI**), key performance indicator (**KPIs**), internal and external (CSN5) **checkpoints**

- *Analisi dei rischi debole. Dovremmo stabilire un paio di parametri precisi (da test su fascio) per determinare se una soluzione è valida oppure no.*

→ a detailed **Gantt** needed. Work in progress on a **risk table**.
Restarting activities after summer just now...

Objectives

WP1: Finalize the design of the Gamma Beam Profiler detector.

Quarter	Task
Q1/2026	Study the performance of the old LUXE prototype in a low charge test-beam, unexplored in previous tests
Q2/2026	Measure the cross-talk of flat flexible cable (FFC) with new interleaved signal-GND topology
Q3/2026	Measure and compare the performance of the FFC (low cost) and micro coaxial (high cost)
Q4/2026	Redesign the sensor PCB and the patch panel to accommodate for the new solution
Q1/2027	Procure and manufacture the microstrip sensor
Q2/2027	Test FERS electronics based on Werooc PsiRoc ASIC
Q3/2027	Assemble the detector setup (sapphire bonding, connections, front-end)
Q3/2027	Characterize the performance of the optimal system at a beam facility in terms of radiation resistance and detector resolution. As a function of: <ul style="list-style-type: none">• Instantaneous beam charge• High voltage bias• Environmental conditions
Q4/2027	GBP detector mechanical and software integration







Risks and mitigations

This WP has two possible risks: unavailability of the test beam line and a sub-optimal performance of the signal cables and electronics.

Since in the test-beams conducted at the CLEAR facility there were limitations to the precision of the provided beam when going to beam charges below 10 pA, the preferred beam line would be the Frascati BTF facility. If that is unavailable, we will ask DESY to provide us with the necessary low-charge beam time. If that is not possible, the CLEAR facility has some solutions they will try to provide a stable beam under 10 pC.






The work plan already contains possible options in case the FFC solution does not yield the necessary results, by using micro-coaxial cables. In addition to the FERS A5202, the future CAEN psiroc-based charge integration board will be tested.

WP1 – milestones and deliverables

-  **1** Characterized sapphire response w.r.t beam's characteristics
 -  **a** Paper on sapphire's application as HEP detector
 -  Application note for interconnection/read-out design (KPIs)
-  **2** Optimal **sensor**-readout interconnection solution
 -  Technical report with FFC/micro-coax. comparison
 -  PCBs and measurement reports

❏ checkpoint ❏

Assessment of the optimal detector design + workshop

-  **3** Final-**sensor** manufacturing and **detector** assembly
 -  Detector ready
-  **4** Performance characterization of the GBP **detector**
 -  Paper on sapphire strip detector performance in a e-beam monitoring application
 -  Technology readiness level report for CSN5-checkpoint (state of the art, present project status and outlook)

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WP1 – Key performance indicators (KPIs)

Sapp. response w.r.t beam's characteristics **KPIs** (define **target**)

- [tech.] Charge collection efficiency (CCE) measured with precision $< \pm X\%$ over beam intensity range.
- [tech.] Linearity of detector response up to X pC beam charge.
- [tech.] Signal-to-noise ratio (S/N) $\geq X$ for MIP-equivalent signals.
- [proj.] Beam test completed (CLEAR/BTF/DESY).
- [proj.] Talk/conference proceeding > 1 on sapphire for HEP by Q2/26.
- [proj.] Peer-review publication 🚚_a by Q3/26.

Detector readout (interconnection + readout) **KPIs**

- [tech.] Crosstalk (%) for any interconnection solution considered
- [tech.] Performance/degradation for each solution
- [proj.] Decision documented with technical report delivered to 4th CSN5 meeting 2026 (Sept.)

WP1 risk assessment

■ Sapphire-sensor risks

- Wafer procurement delays
- Manufacturing defects
- Wire bonding / wafer handling

■ Rischi tecnici sui materiali (difetti nella metallizzazione, fragilità dei wafer sottili).

■ Rischi di integrazione software/meccanica (compatibilità con sistemi di acquisizi

■ CAEN does not deliver Werooc PsiRoc asic

■ Rischi di personale/organizzativi (dipendenza forte da CAEN o da beamtime esterno).

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