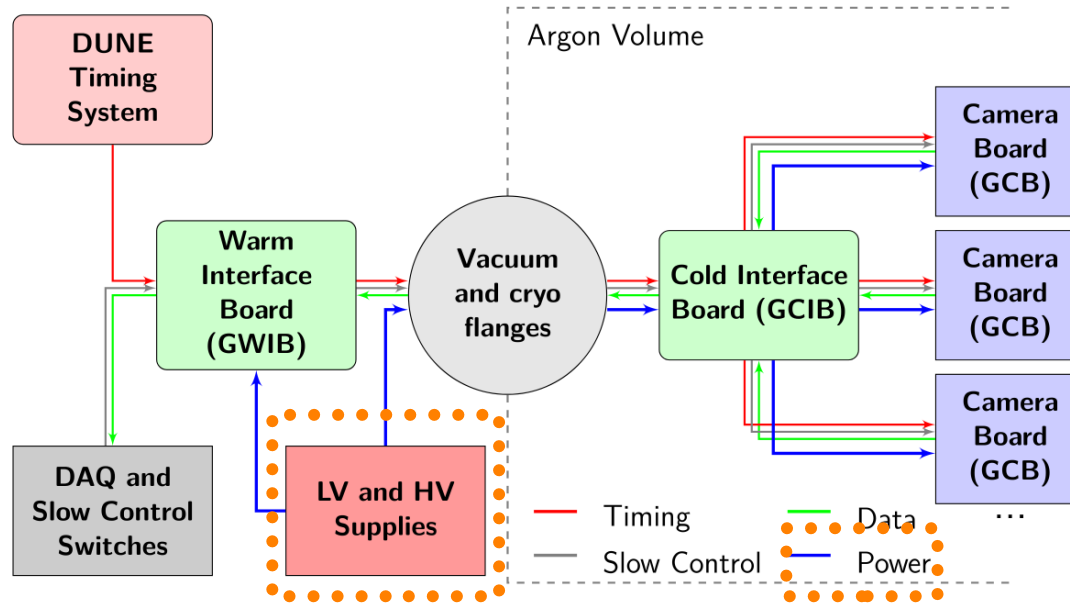


GRAIN Feedthroughs and power mockup

Nicolò Tosi – INFN Bologna

DUNE Italia 11/11/2025

Part 1: Powering challenges

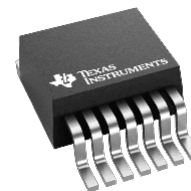


Powering DENEb in GRAIN

- DENEb uses a reasonable amount of power, but requires this power at a low voltage and high current:
 - Analog Vdd @1.2V: ~1 A when off, ~8 A working
 - Digital Vdd @1.2V: ~4 A when off, ~8 A working
- Supplying this power would be trivial without
 - Cryogenic Immersion and cryostat penetration
 - Magnetic Field
 - Rapid cycling to reduce heat load (settling < 1 ms)

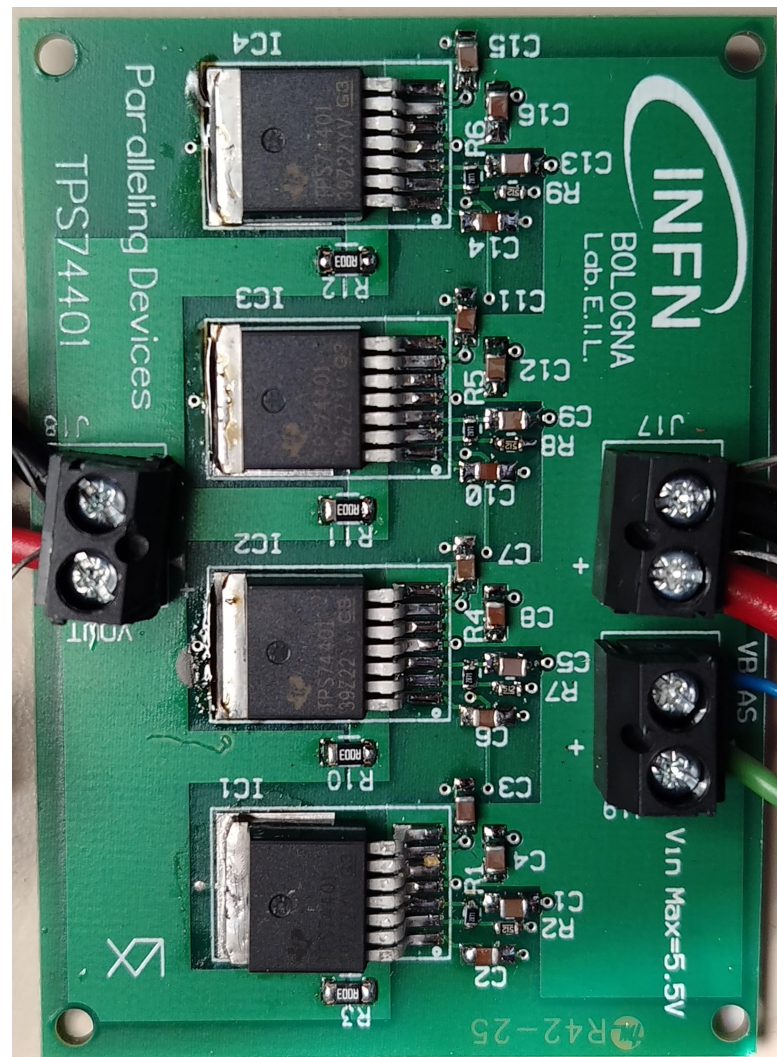
Cryo regulator on camera board

- We have not found any cryogenic Switching regulator
 - would allow conversion of reasonable currents at higher voltages
 - would also need to work in B field – not trivial
- Very few models of cryogenic linear regulators known to exist
 - None of these supply even close to 8A
 - Best candidate is Texas TPS74401 supplying 3A
 - Paralleling works but has downsides (worse load regulation)
- Designed a test board to exercise parallelization
 - Board is ready, will require systematic testing



LDO test board

- Four regulators in parallel
 - Up to 12A
- Very first cryo bath OK
 - Tested only up to 7A
 - Some limits from test setup
- Ballast resistors cause mediocre load regulation
 - Improves a bit by itself in cryo
 - Can use smaller R

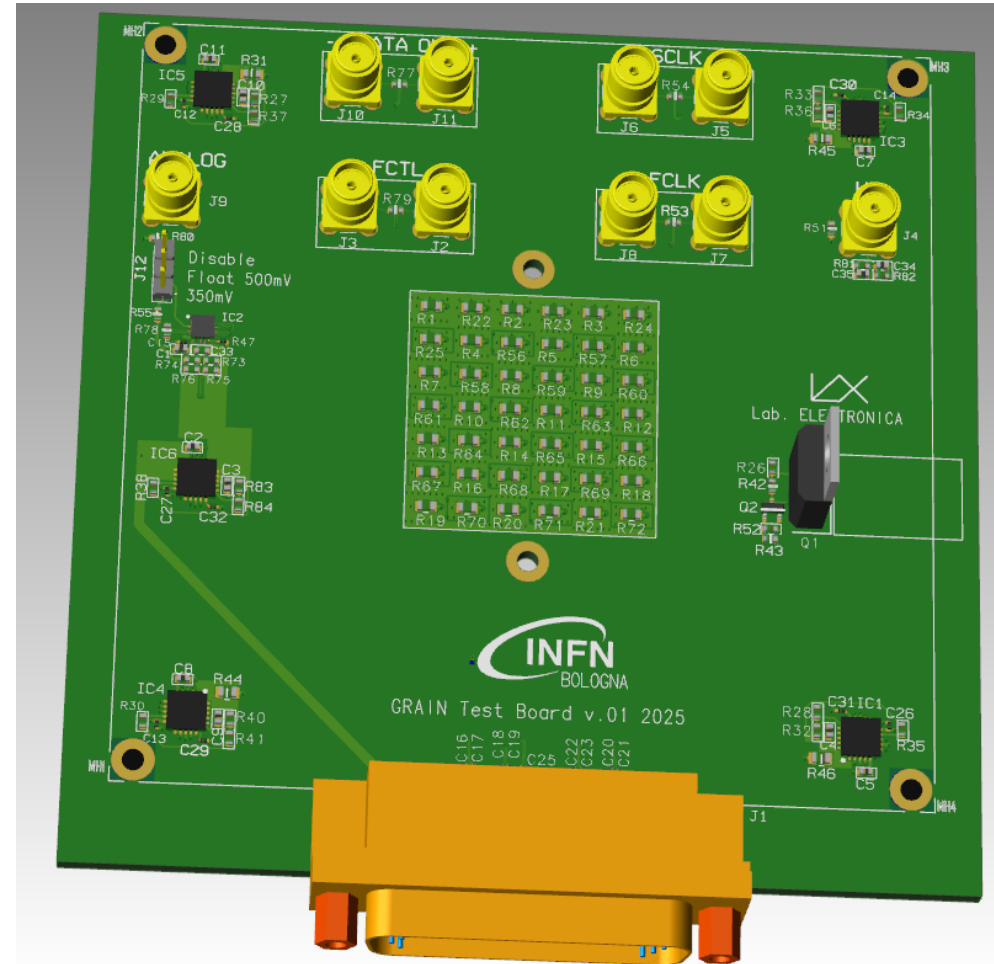


End goal: full power mockup

- Mockup boards were planned for end of this year
 - The increase in power caused us to redesign the power system
 - Search for more powerful LDOs took a few months
- Todo by 2025: intermediate test with 4-LDO board
 - Measure performance up to max current, stress test few weeks
 - Measure settling time for power gating, high cycle count
 - Work on improving load regulation
- Q1 2026: complete redesign of mockup boards
 - Incorporate also changes in connectors (see part 2)

The mock-up

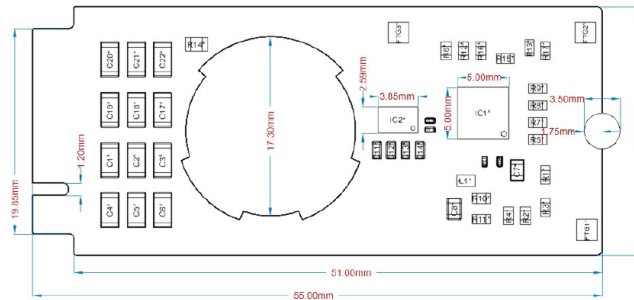
- Old design lower power
- The mock-up is sized like a real GCB
- Excessive number of layers (18), to spread heat from the central region (would be needed for routing in the actual GCB)
- Mock connection via the D-Sub, test via SMA



The rest of the power chain

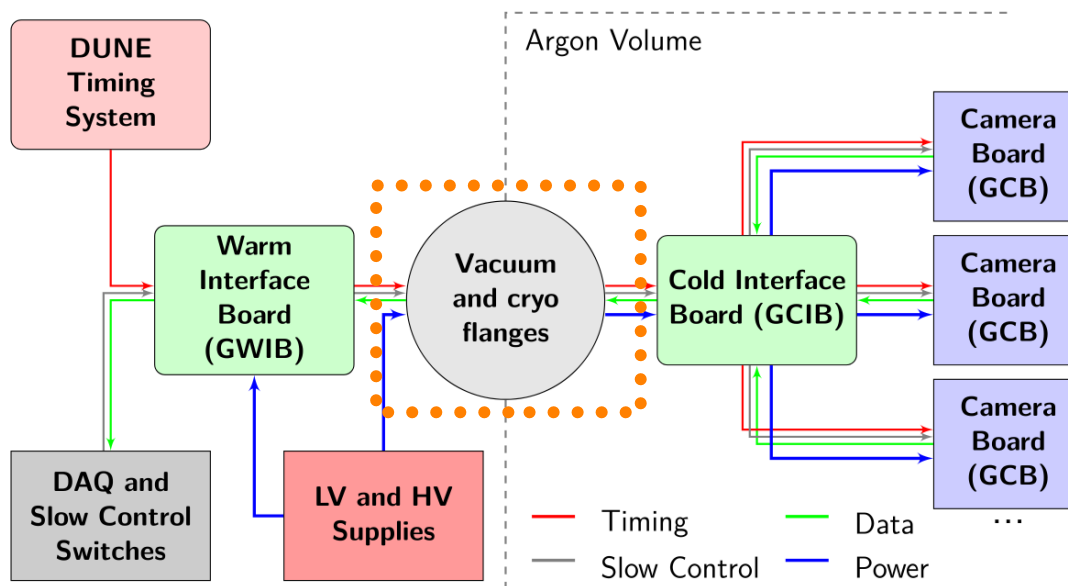
- Option: use a warm, B-field tolerant switching regulator on the GWIB?

CERN bPOL-48V
Air Core Inductor



- With regulator:
 - More efficient, possibly less expensive (fewer CAEN boards)
 - Needs testing, design effort
- Without regulator
 - Simpler, possibly more robust
 - Thicker cables, more wasted power

Part 2: Feedthroughs



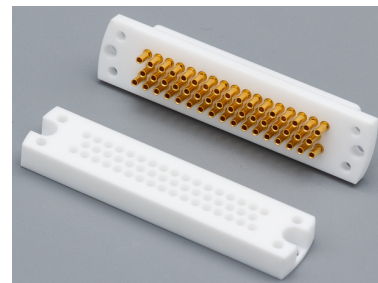
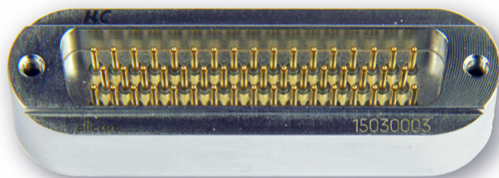
Cryo-vacuum feedthrough

- Some issues with completely custom solutions
 - Lack of expertise on our side
 - Few if any actually submerged (mostly in gas, warmer...)
 - Unclear if we could formally meet certification standards
 - Relatively limited quantity to absorb R&D costs
- Limited to catalog of available suppliers
 - Not the best match for our data lines requirements
 - Not space efficient on our small flanges



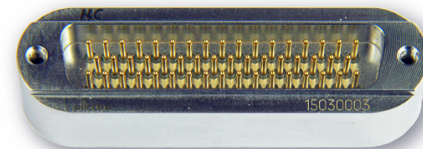
Power connections

- Power for DENEb requires high current connections
 - Standard solution available: Sub-D High Current Pins, 6 A each
 - 2 x 50-pin connectors cover the eight boards per flange
 - Includes SiPM bias around 40V, auxiliary voltage(s).
- This is based on Allectra catalog parts:
 - Feedthrough, Kapton insulated wire, Ceramic cryo Connector



Data connections

- Commercial parts typically include:
 - Sub-D or similar multipin connector, no controlled impedance, mates with unshielded ribbon cables
 - Common coaxial types, of which the smallest is SMP, with 50 Ohm connectors and cables
- Critically: there is no ready-made 100 Ohm differential high-speed connectors
 - Either use 2 x coax => very costly
 - Develop our own based on available parts

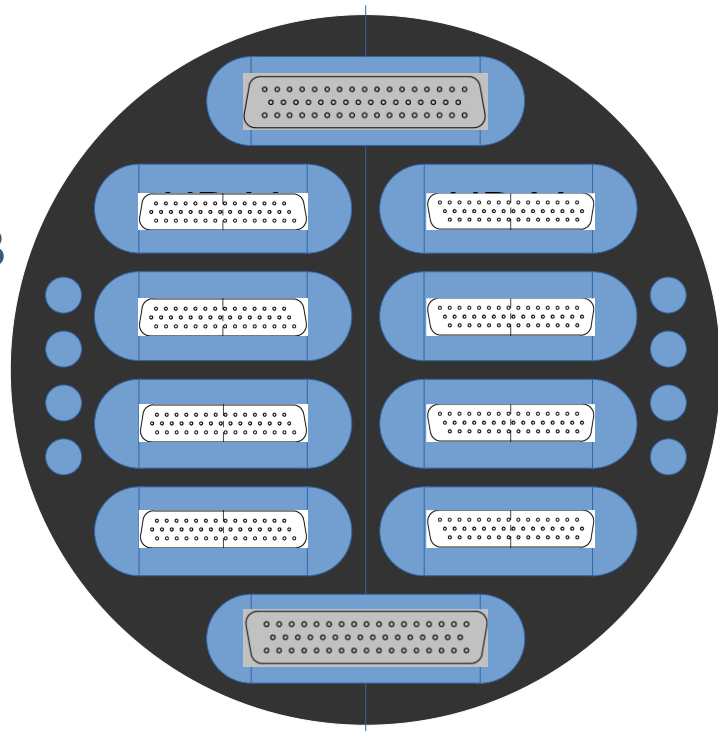


Data connections: requirements

- Most critical lines (>300 MHz B/W):
 - Analog port (our main test/calibration feature), 50 Ohm single
 - Clock port, 100 Ohm differential SLVS
- Other high speed lines (~300 MHz B/W):
 - Data port, Multifunction port, 100 Ohm differential SLVS
- Other lines:
 - Configuration, 3x, 100 Ohm differential SLVS
 - Reset, 100 Ohm differential SLVS

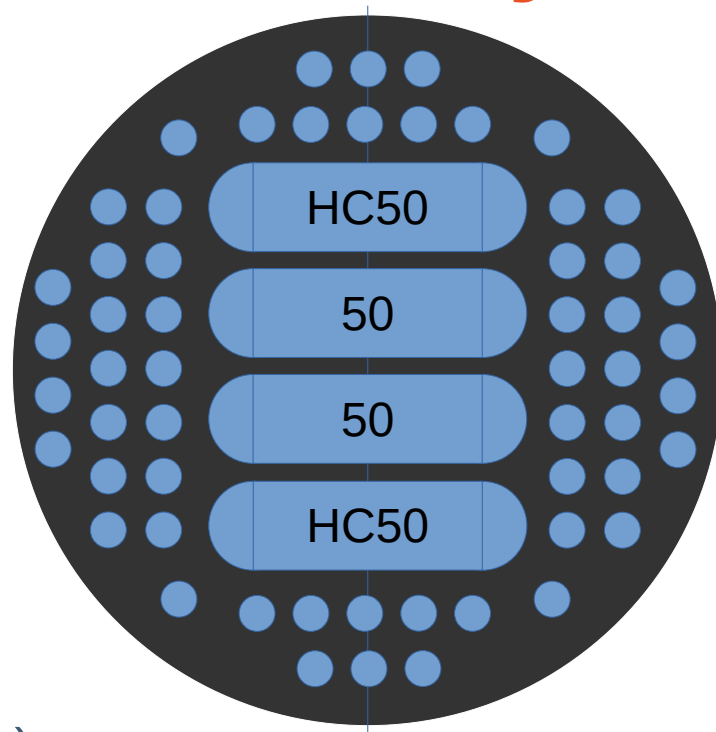
Data connections: semi custom

- Design:
 - High density Sub-D connector
 - Custom controlled impedance flex PCB
- Pros:
 - Least expensive (300-350k)
 - Allows independent connections
- Cons:
 - No catalog ceramic option for connectors
 - R&D risk. We have most components for test, delay with flex PCB



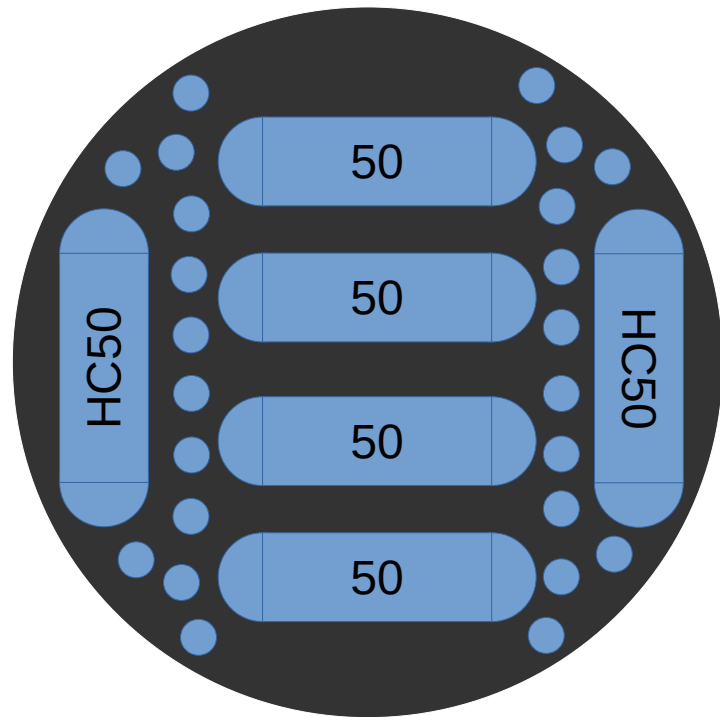
Data connections: coaxial only

- Design:
 - Sub-D connector for non critical lines
 - Coaxial for everything else
- Pros:
 - No R&D effort
 - No (very low) risk
- Cons:
 - Installation challenge (more than others)
 - Cost. Likely approaching 500k with cables and connectors



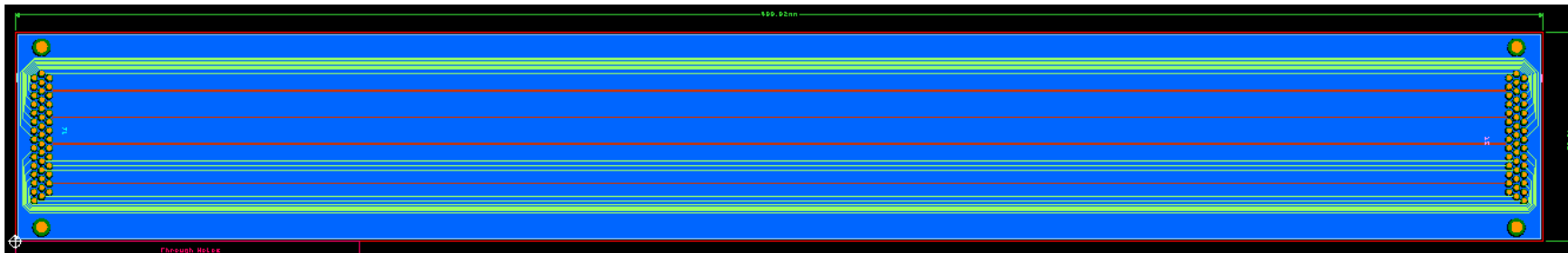
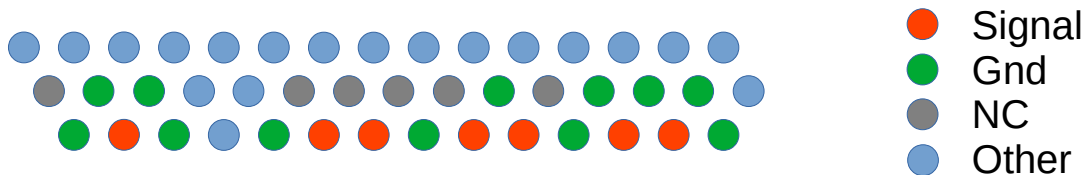
Data connections: Intermediate

- Design:
 - Sub-D connector for most lines
 - Coaxial only for clock and analog
 - Flex PCB for less critical lines?
- Features:
 - Ceramic option available for Sub-D
 - Intermediate R&D effort
 - Intermediate risk
 - Intermediate cost (400k-ish??)



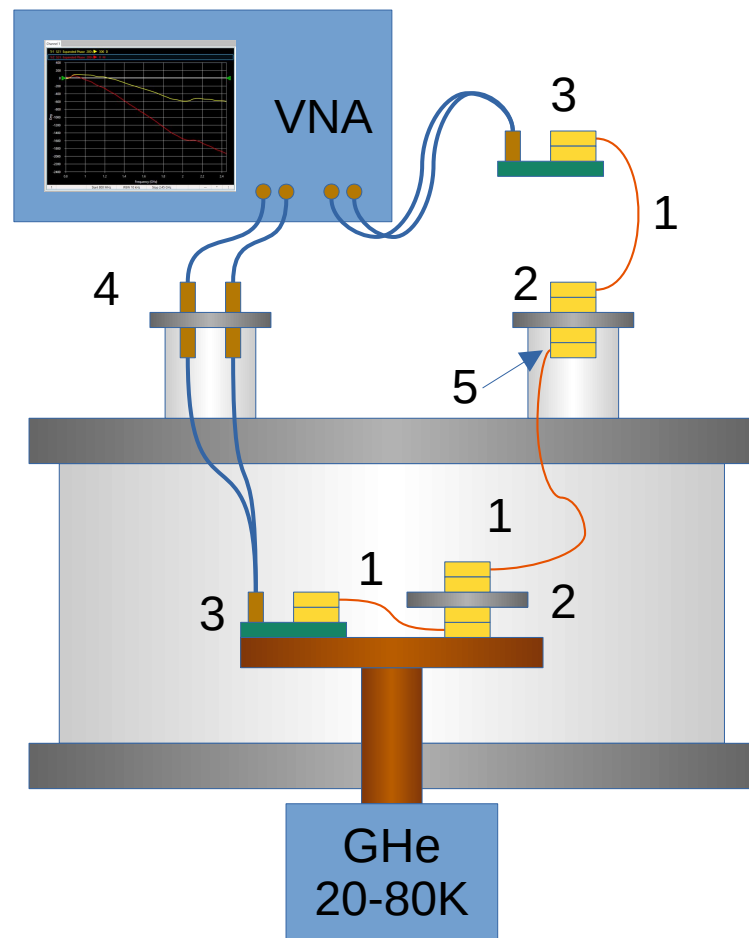
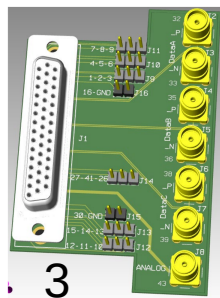
Kapton flex “cables”

- On order (now at >6 wks admin delay on the order...)
- Can test single ended 50 Ohm, Differential 100 Ohm in various configurations



Basic test setup

- Cryo and vacuum combined
- Dry, but can go down to 20K
- Test Cable (1)
- D-Sub 44 HD feedthrough (2)
- Adapter PCB (3)
- SMA feedthrough (4)
- Most critical bend (5)

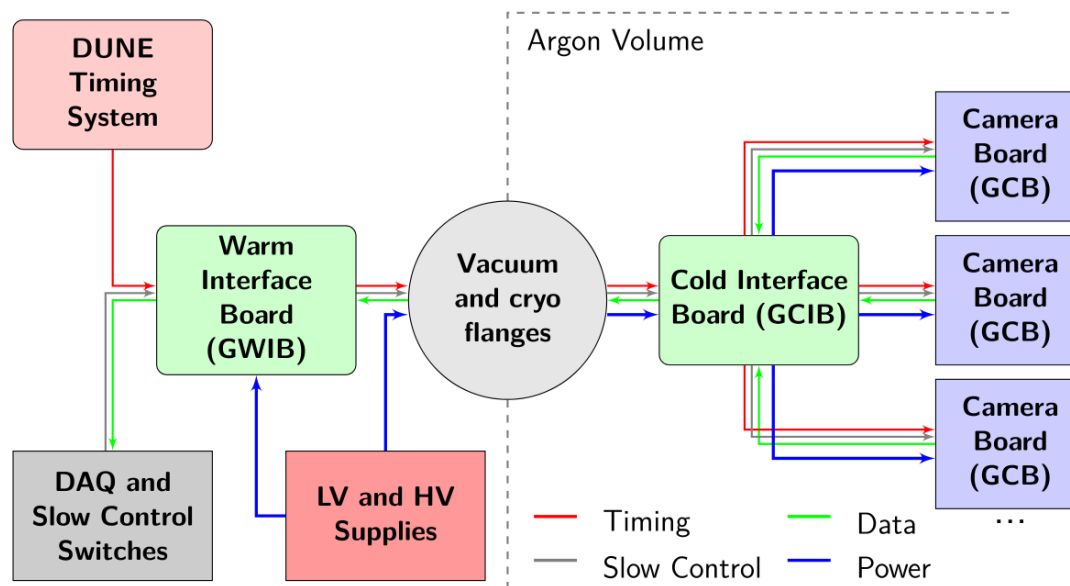


Tentative test plan

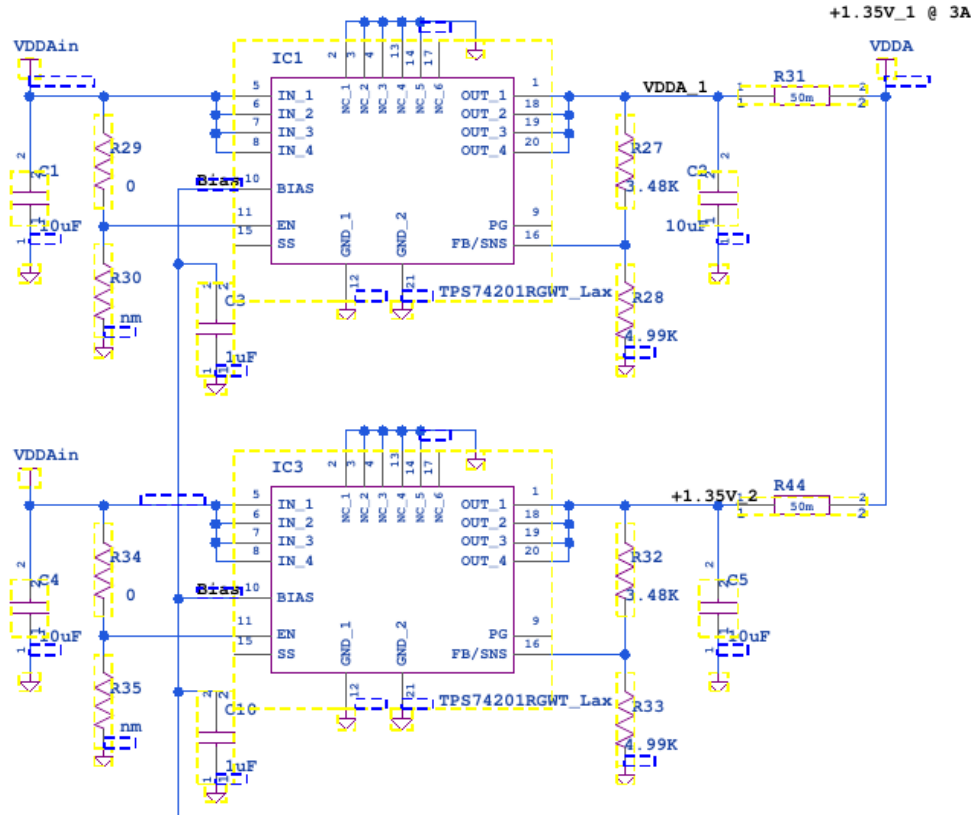
- Tests an individual connection chain in Bologna using LN₂ and the cold finger setup
- More extensively test the power scheme (including outer power supply, relevant for transients)
- All the missing components will be ordered before end of 2025 (assuming no further admin delays)
- Complete test setups should be available end of Q1 2026
- Full test protocols to be established



Backup



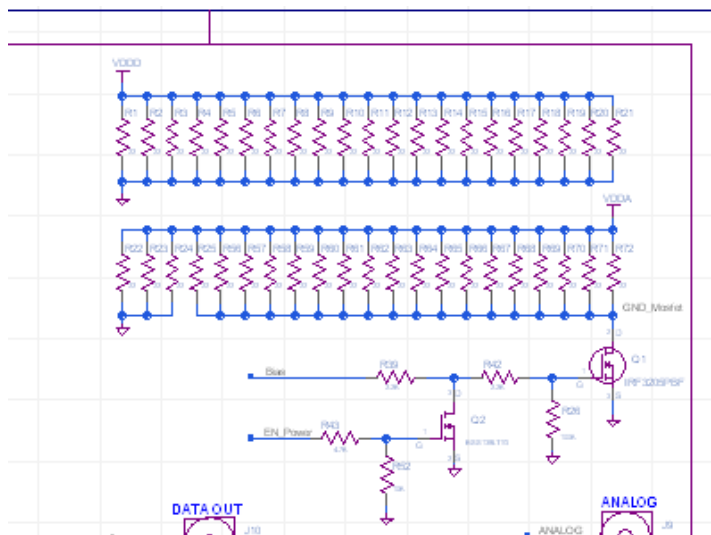
LDOs



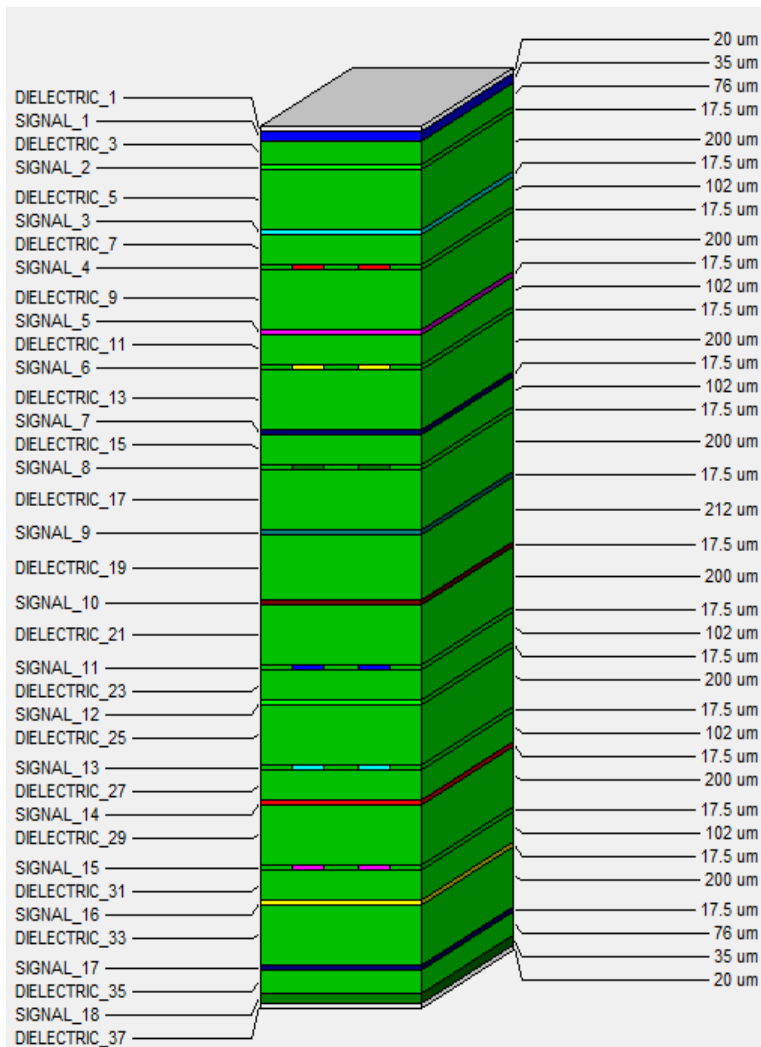
TPS74201

- Known to work in cryo
 - Iout max 1.5A
 - Vout 0.8 to 3.6V
 - Dropout < 100mV
- VddA: 2x LDOs @ 1.2V
- VddD: 2x LDOs @ 1.2V
- VddIO: 1x LDO @ 1.8V
 - Only used by LVDS/SLVS buffer

“DENEb”



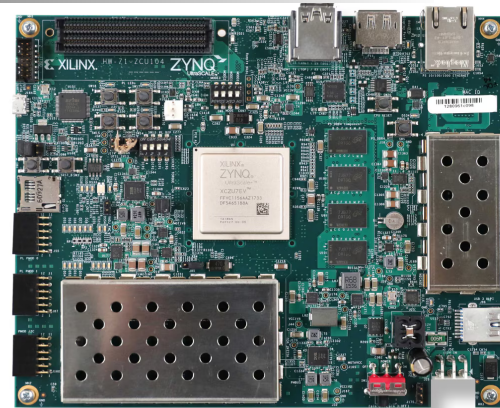
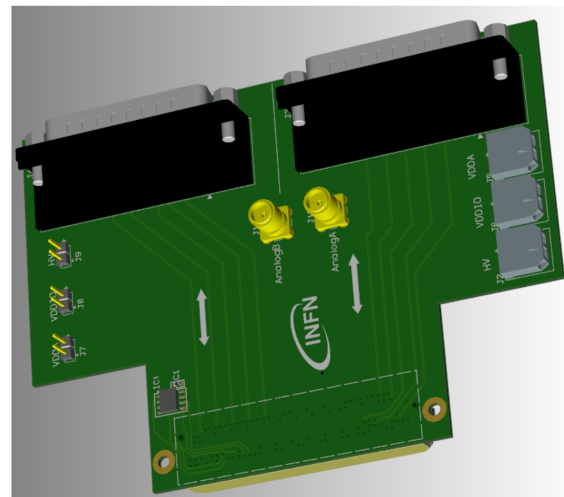
- Two sets of resistors in parallel
 - Default is ~ 1 Ohm per set
 - Set powered by VddD is always on, draws ~ 2 W
 - Set powered by VddA is enabled by mosfet, draws ~ 2 W when on, ~ 0.2 W when off
 - Set resistance will be adjusted to match real power draw
 - Layout and size matches ASIC size very roughly



Layer/Net		Layer Usage	Plane Type	Plane Class	Plane Data State
Layer 1	...	Plane	Positive	(Default)	Dynamic
GND	○			(Inherited)	Dynamic
GND_Mosfet	○			(Inherited)	Dynamic
VDDA_1	○			(Inherited)	Dynamic
VDDA_2	○			(Inherited)	Dynamic
VDDD_1	○			(Inherited)	Dynamic
VDDD_2	○			(Inherited)	Dynamic
VDDIO	○			(Inherited)	Dynamic
VDDIOin	○			(Inherited)	Dynamic
Layer 2	...	Plane	Positive	(Default)	Dynamic
VDDAin	○			(Inherited)	Dynamic
Layer 3	...	Plane	Positive	(Default)	Dynamic
GND	⊙			(Inherited)	Dynamic
Layer 4		Signal	Positive	(Default)	Dynamic
Layer 5	...	Plane	Positive	(Default)	Dynamic
GND	⊙			(Inherited)	Dynamic
Layer 6		Signal	Positive	(Default)	Dynamic
Layer 7	...	Plane	Positive	(Default)	Dynamic
VDDD	○			(Inherited)	Dynamic
Layer 8		Signal	Positive	(Default)	Dynamic
Layer 9	...	Plane	Positive	(Default)	Dynamic
GND	⊙			(Inherited)	Dynamic
Layer 10	...	Plane	Positive	(Default)	Dynamic
GND_Mosfet	⊙			(Inherited)	Dynamic
Layer 11		Signal	Positive	(Default)	Dynamic
Layer 12	...	Plane	Positive	(Default)	Dynamic
VDDA	⊙			(Inherited)	Dynamic
Layer 13		Signal	Positive	(Default)	Dynamic
Layer 14	...	Plane	Positive	(Default)	Dynamic
GND	⊙			(Inherited)	Dynamic
Layer 15		Signal	Positive	(Default)	Dynamic
Layer 16	...	Plane	Positive	(Default)	Dynamic
GND	⊙			(Inherited)	Dynamic
Layer 17	...	Plane	Positive	(Default)	Dynamic
HV_gnd	⊙			(Inherited)	Dynamic
Layer 18	...	Plane	Positive	(Default)	Dynamic
HV	⊙			(Inherited)	Dynamic

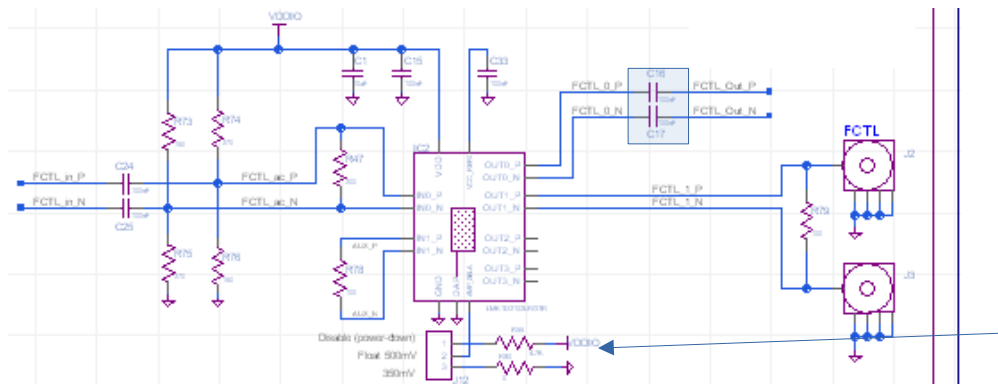
The FMC adapter

- Interfaces the ZCU104 development board with our cables on DB44
- Provides an SLVS compatible driver (the Zynq has a builtin compatible receiver)
- Separate input connectors for Power, HV
- Separate output for analog signal
- Usable on its own for thermal-only tests.
How many do we want?
 - We can make it with 4 connectors too



“SLVS” Driver

LMK1D210xL



Schematic shown here is for mockup

Can be used AC or DC coupled, if AC coupled we will test a “pulldown” termination that may be useful for fast control line

- I/O Buffer to have something to attach differential lines to...
- Not quite SLVS (not available)
- Input CM range 300-2300 mV, swing 300-2400 mV
- Output CM 700 mV typ. (+-100)
- Output swing adjust 350-500
- Used in FMC to drive outputs
- Used in Mockup for “active” loopback

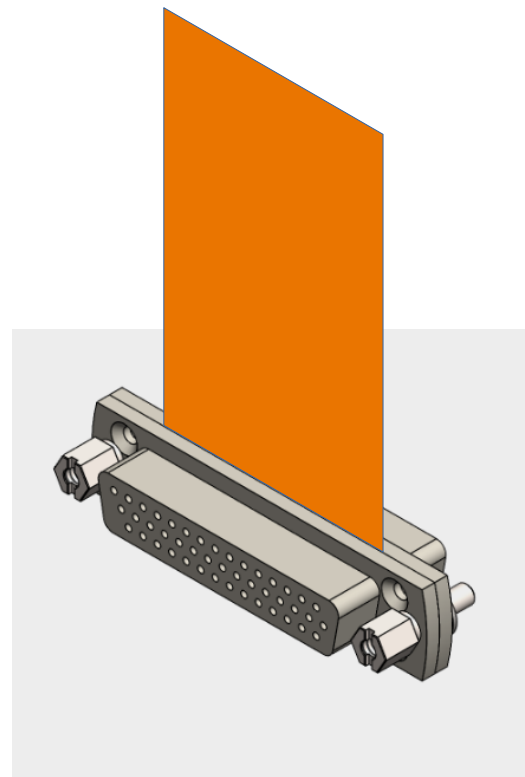
DB44 and cables

- ~12-20 lines for DENEb I/O
- Others GND for impedance control, “shield”



Allectra commercial:

- no impedance control
- no shielding
- likely differential skew



Our idea:

- use Allectra connector, maybe modify top half
- insert multilayer kapton cable in the middle
- solder Allectra pins to the cable
- 50/100 Ohm traces, shield, power planes, ...