A Cryogenic 1024-Channel Mixed-Signal ASIC for SiPM Readout in 110 nm CMOS for the GRAIN Detector at DUNE

DUNE ITALIA Collaboration Meeting
11/11/2025

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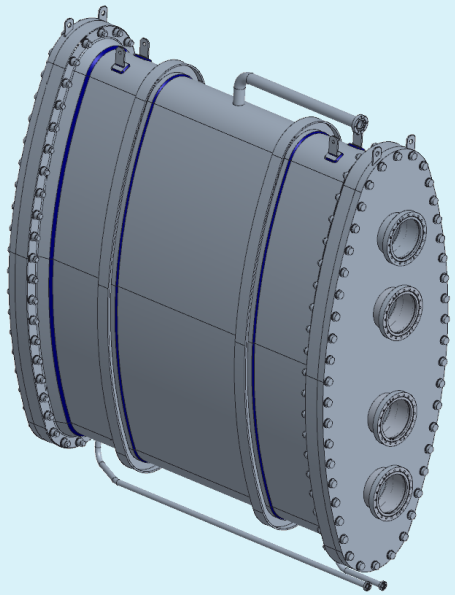
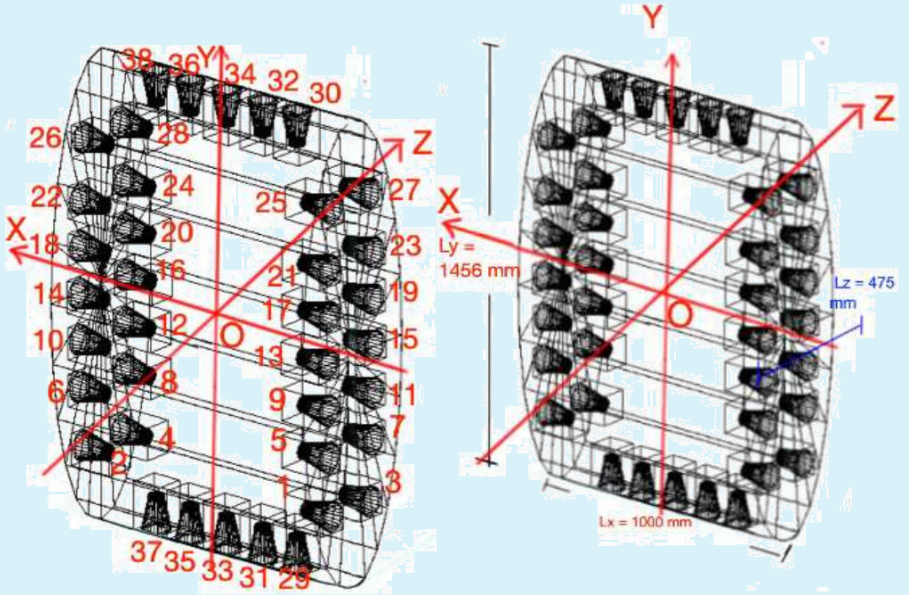
DENEBx1024 for GRAIN at DUNE

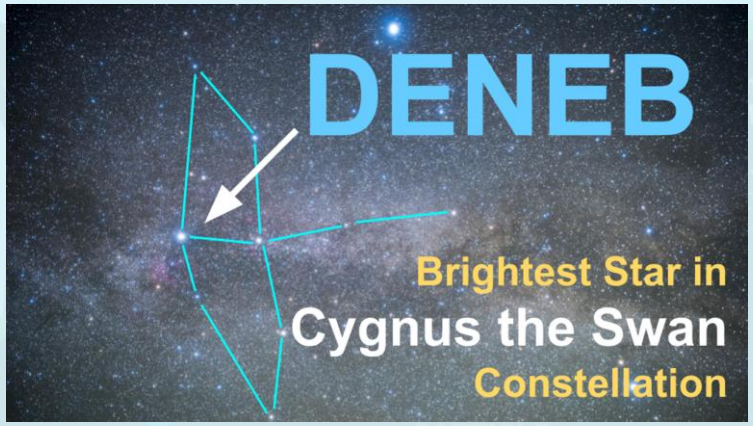
60 Cameras operating in lAr (87K):

- **Optical lenses / Coded Aperture Masks** for focusing the light
- **Sensor: 32 x 32 SiPMs Matrix** mounted on a board with a
- **<u>Readout ASIC 1024-channel</u>**

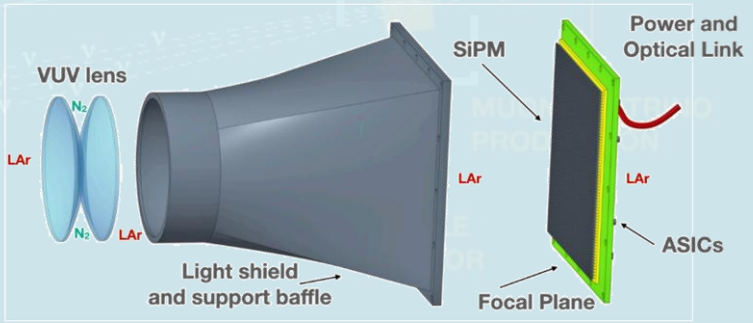




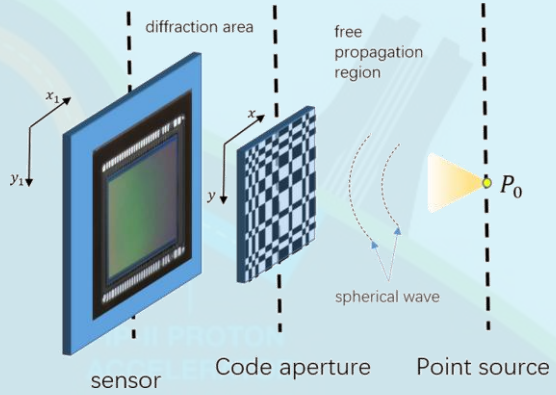
Dune integrated **E**lectronics for **NE**utrino **B**eams



Optical Lenses

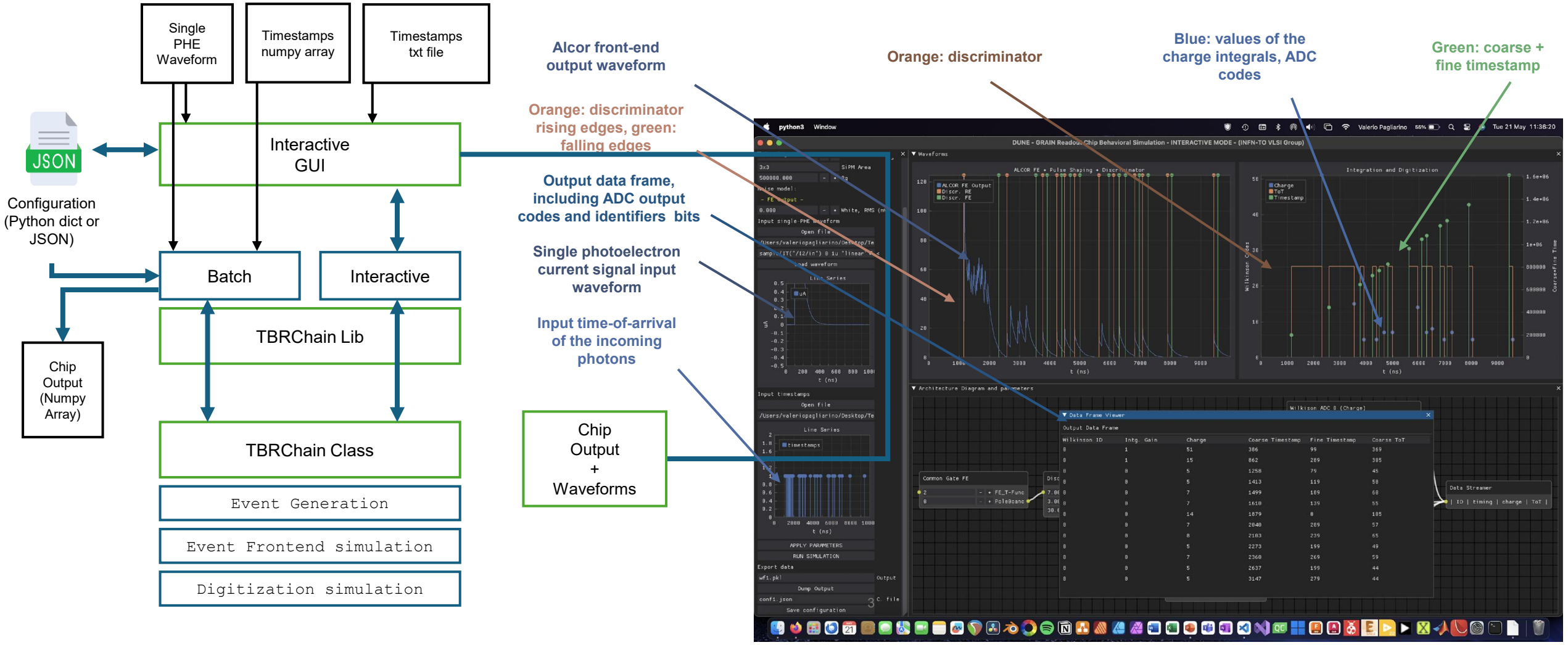


Coded Aperture Masks



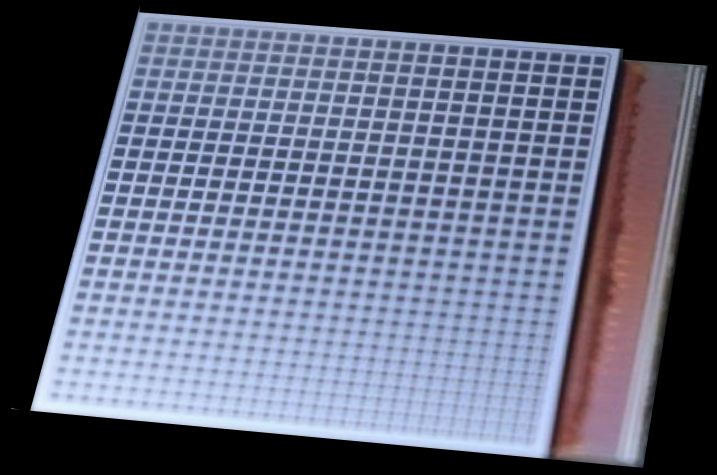
DENEB Software Model

In the DUNE-GRAIN project, Python software implementing a full chip behavioral model has been developed, in order to validate the design requirements against simulated data (time-of-arrival of single photons) produced by physics simulation codes.

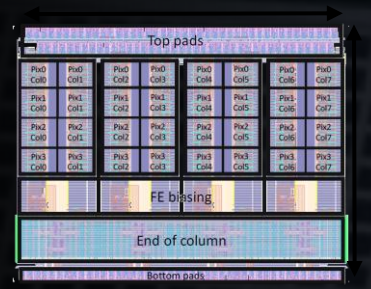


Features	DENEBx1024
Technology	**UMC 110 nm**
Operating Temperature	**77 K – 300 K**
Channel Modularity	**1024**
Measurements	**ToA, ToT, Slew Rate, Charge Integral**
SPTR / Slew Rate Resolution	**50-100 ps**
Time over Threshold Resolution	3 ns
On-Pixel TDC Derandomization	4x
Photon Counting Resolution	**3-4 codes/PE**, 1 PE between 1 and 5 (Slew Rate)
Charge Dynamic Range	**[0.5 – 100 PE]**
AVG Power Density	**5-15 mW/ channel**
Silicon Die Size	20 x 23 mm^2 (Reticle Size)
Event word	**128 bit , 64 bit (no charge integration)**
Number of Tranceivers	**32 = 1 x 32 Column (with TDM)**
Single Transceiver Speed	**SLVS/LVDS : 320 Mbps SDR or 640 Mbps DDR**
Event rate / pixel	312.5 kHz (uniform), 2 MHz (max on a single channel)
Clock Frequency	310-325 MHz
Specific Features	**Power gating, Asynchronous Events Gate VETO (ALICE 3 RICH)**

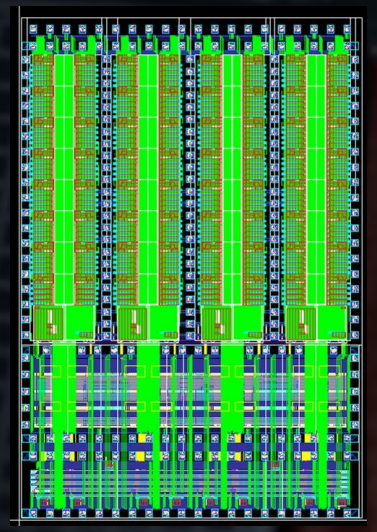
Technology Choice



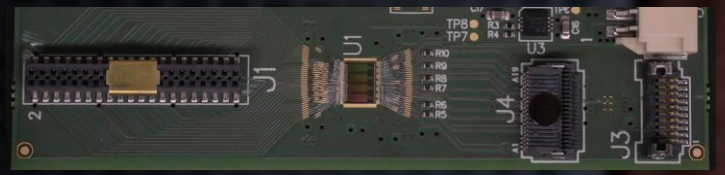
ALCOR's Parent: 1024 pixel channels were bump-bonded to the silicon pixels. The ASIC was wire-bonded on the board



From 32-ch to 64-ch



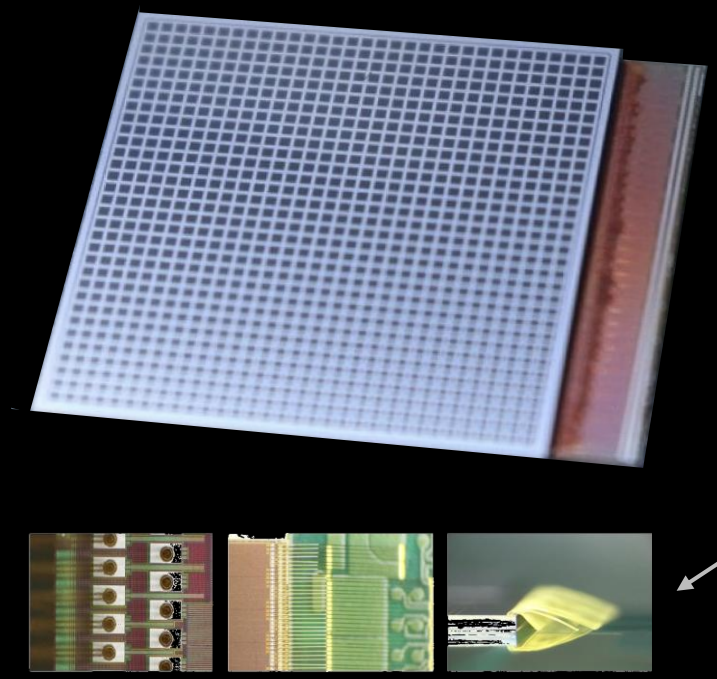
ALCOR v2 wire-bonded on the PCB



- **WHIN: 1024 Channels**
  TT Development at INFN Torino
  - **UMC 110 nm**
  - 1024 Channels, reading out silicon pixels
  - The ASIC is bump-bonded to the pixels
  - Key IP blocks like the **TAC based TDC (30 ps)** **CFD**
  - **Output BW 20 Gbps,** data rate limited by the EoC
  - **It laid the basis for different following prototypes**

- **ALCOR v1-2-3 : 32 – 64 Channels**
  A **L**ow power **C**hip for **O**ptical sensors **R**eadout
  - **Single photon sensitivity**
  - **Time measurement: ToA** + **ToT** or **Slew-Rate** information for **time walk correction**
  - **Triggerless** readout scheme with **fully digital output**: 32-bit event word, 4 LVDS 320 MHz DDR Tx links
  - Power consumption **~10-12 mW/channel**

Technology Choice



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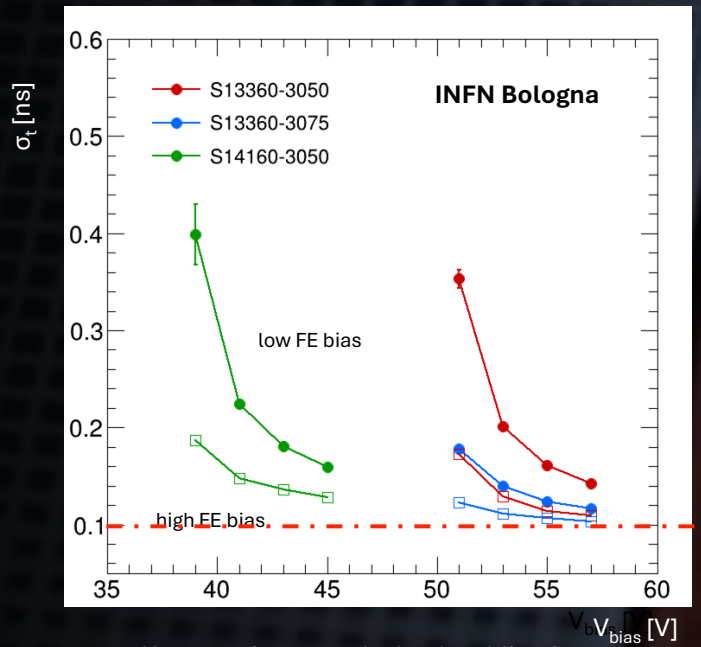
Single Photon Time resolution



If you are interested, check publication:
https://www.sciencedirect.com/science/article/pii/S0168900224007435

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DENEBx1024 Floorplan

ASIC Size & Layout

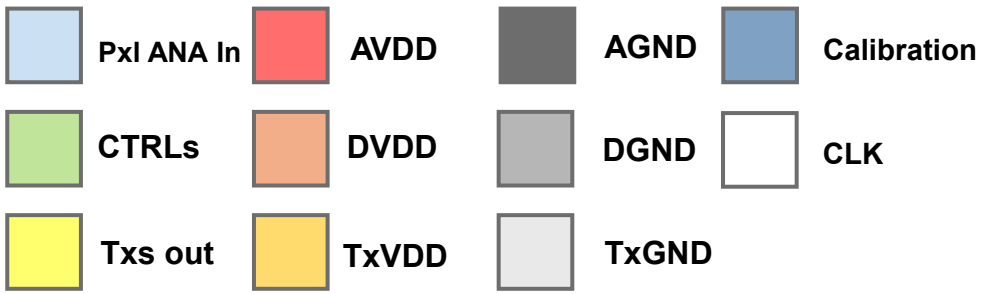
- **Reticle-size chip**: from **2 × 2 cm²** up to **2 × 3 cm²**
- Uniform array of **I/O pads on a 500 µm pitch grid**

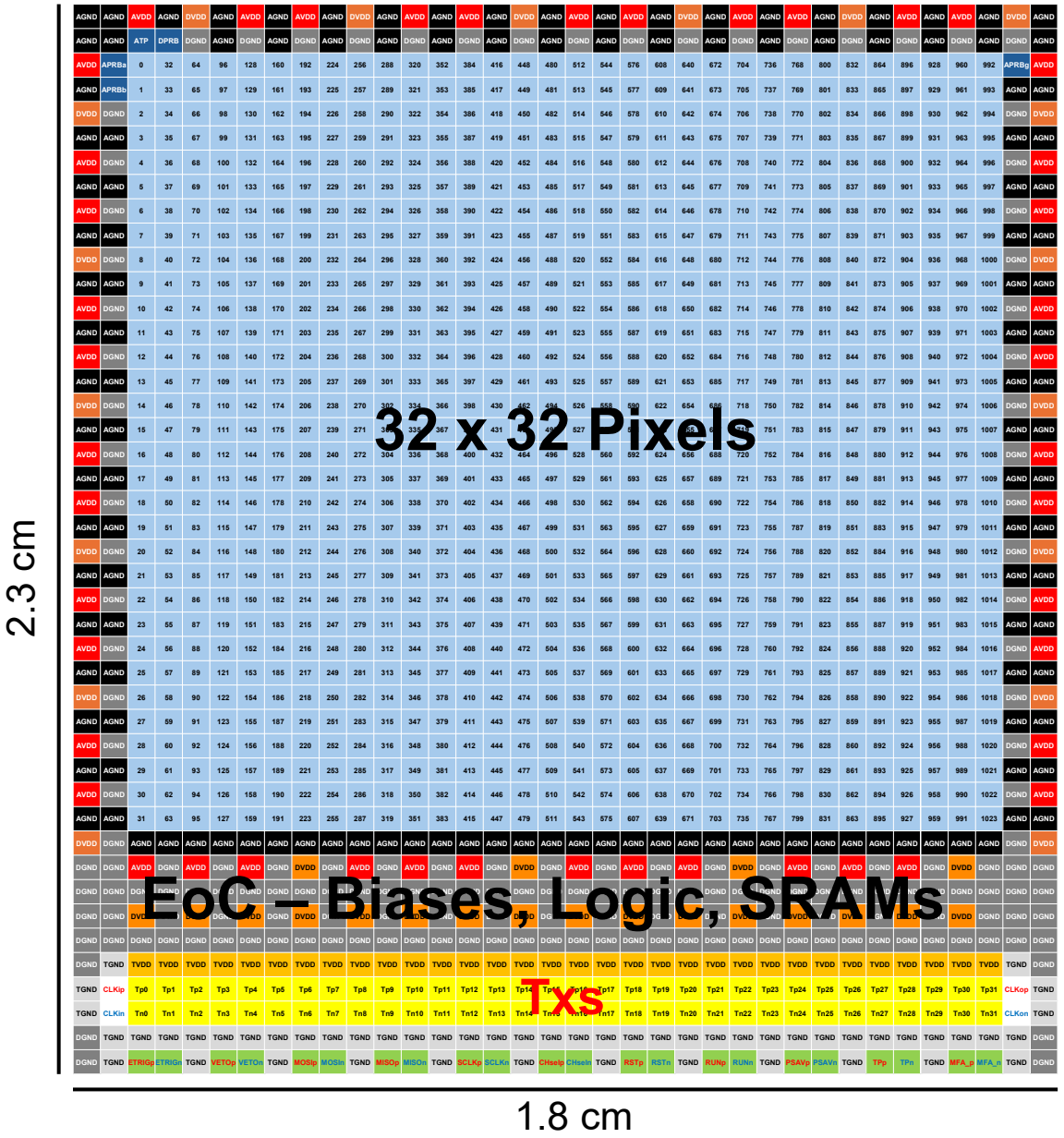
Input Analog Interface

- Mixed-signal ASIC with **high-density analog input pads**
- **32 × 32 channels**, each with a dedicated analog input pad
- Pad pitch driven by channel layout (**500 µm square pixels**)

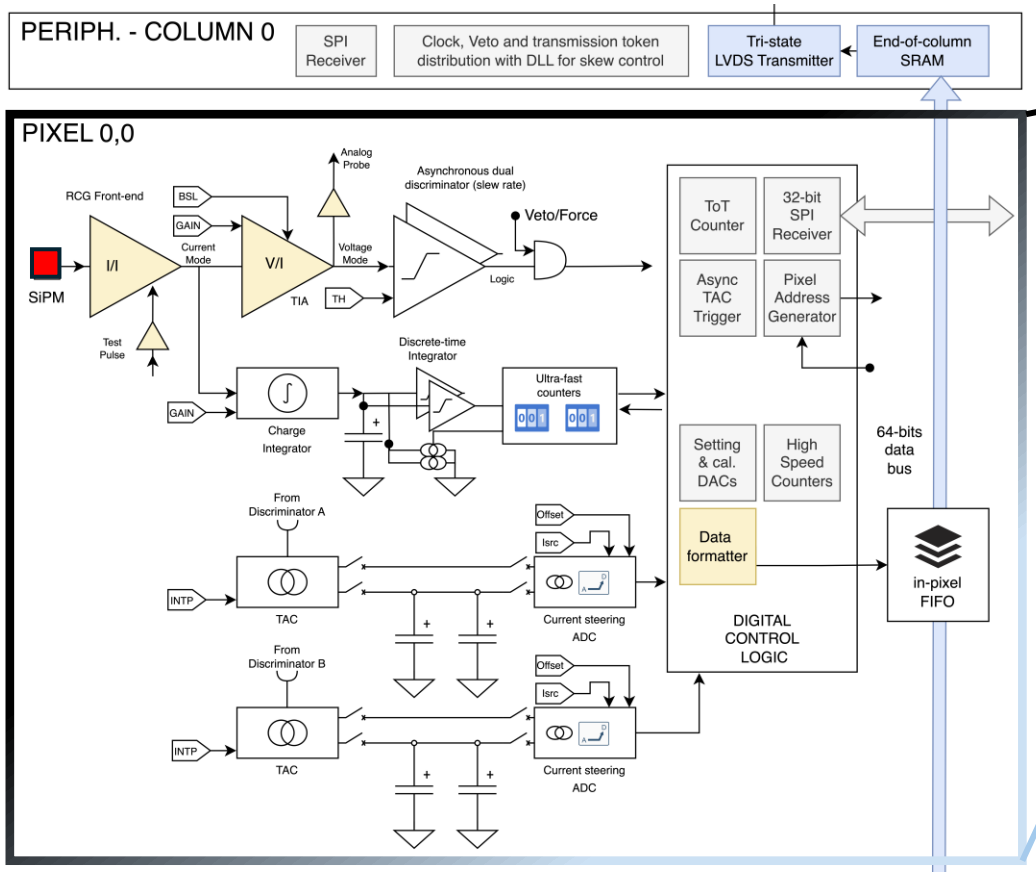
Digital Ouputs:

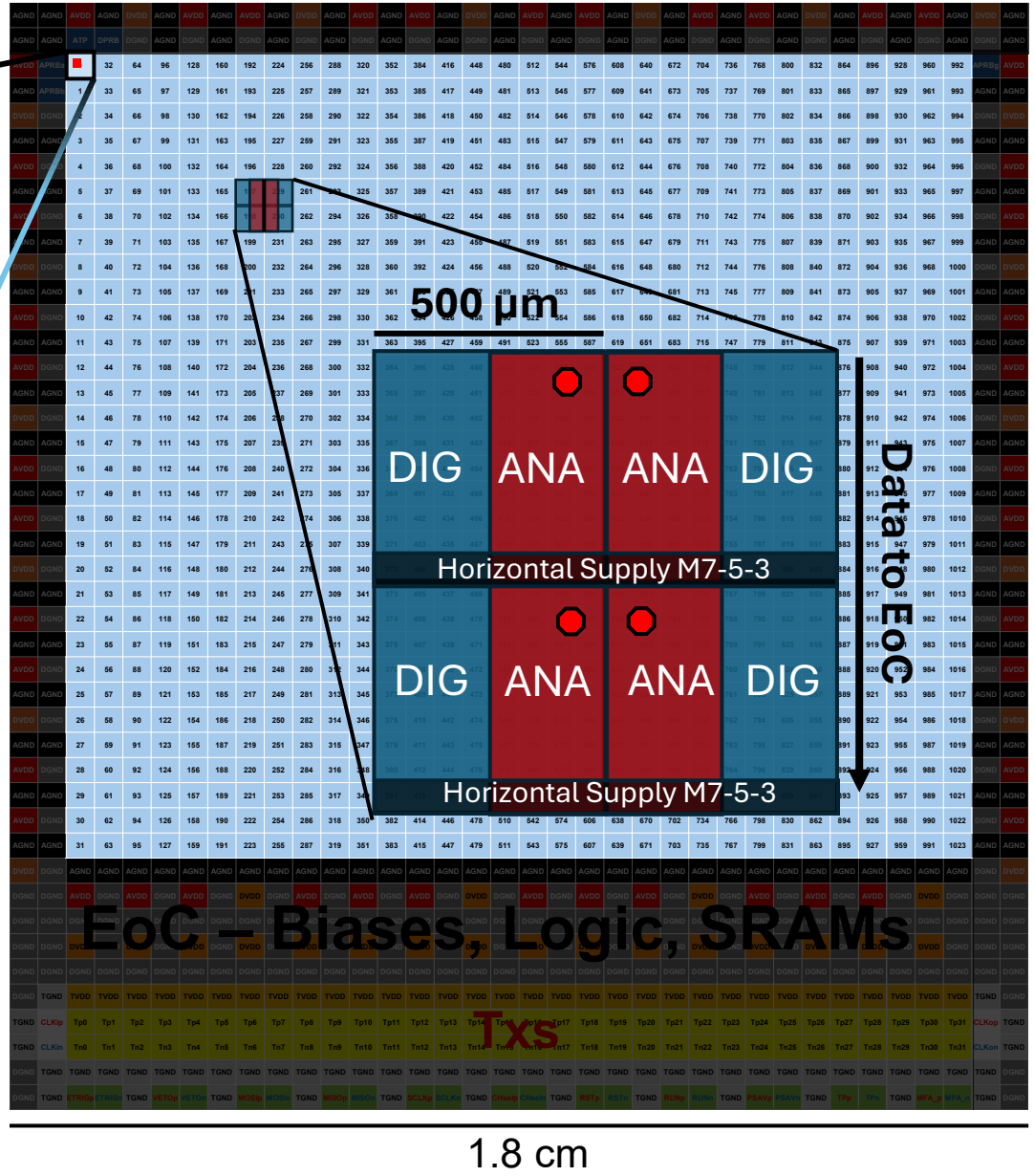
- **Located at the EoC: 32 x SLVS-LVDS TXs, 640 DDR (TDM)**
- EoC SRAMs can store up to 1 spill acquisition





DENEBx1024 Pixel Architecture

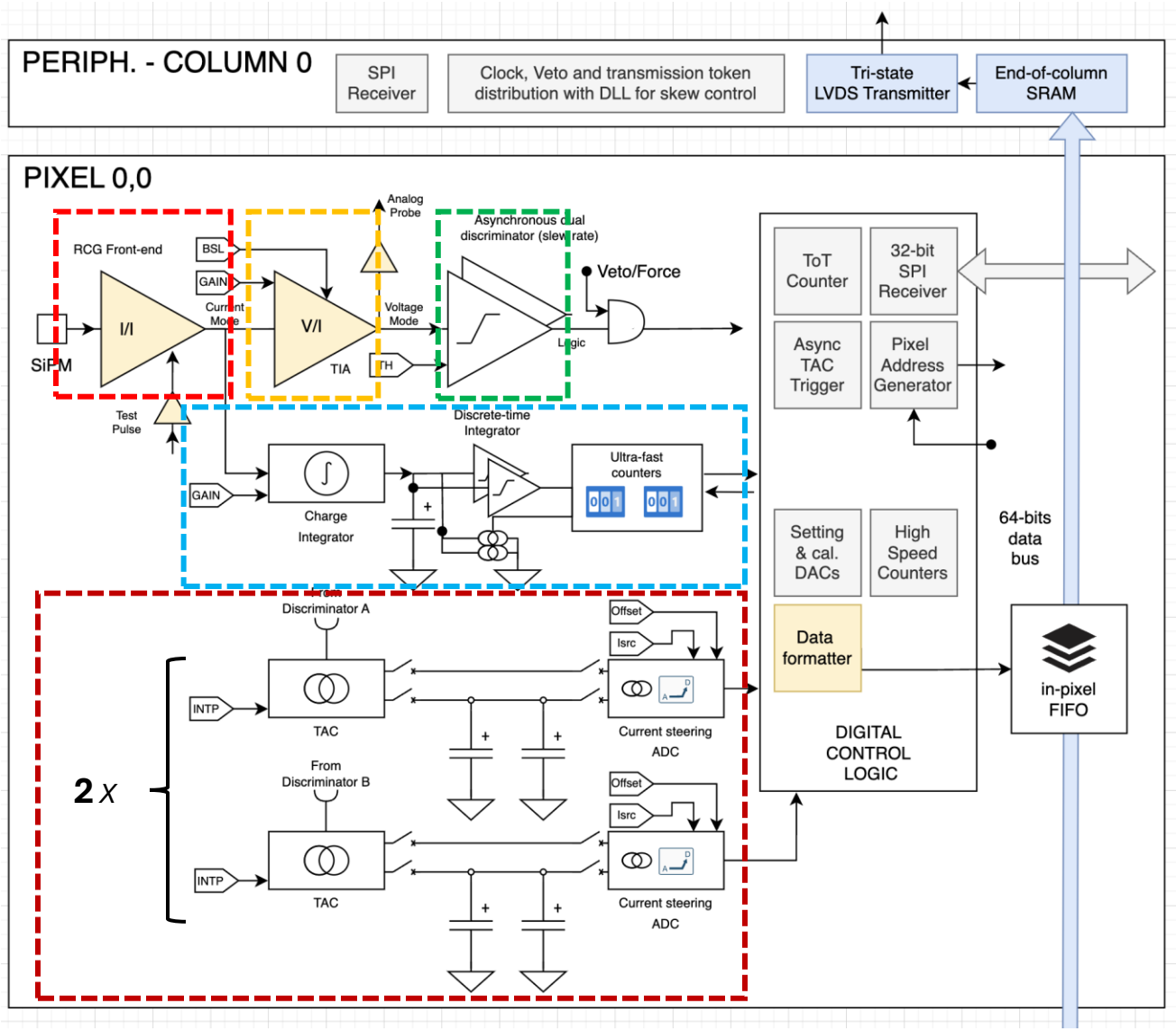




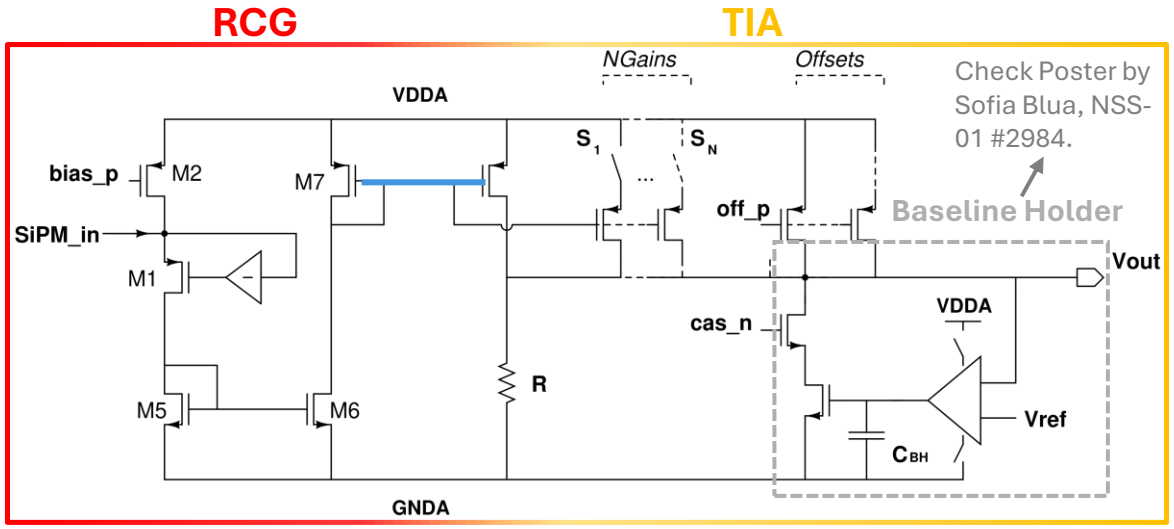
Pxl ANA In
AVDD
AGND
Calibration
CTRLs
DVDD
DGND
CLK
Txs out
TxVDD
TxGND

DENEBx1024 Pixel Architecture

- **Regulated Common-Gate (RCG)** very front-end
- **Fast transimpedance amplifier** for the timing branch
- **2x Fast asynchronous discriminators** (for slew rate measurements) with VETO and Force Trigger features for trigger and time pick-off
- **1x Charge Integrator** with data converter to the digital domain
- **4x Time to Analog Converter** with Hybrid SAR ADCs for fast time digitization
- **In-pixel trigger window for dark count suppression**
- Digital Test Pulse
- Analog Probe Buffered Output



Very Front-End: Time Branch



TWELL MOSFET for mitigating mixed-signal substrate noise

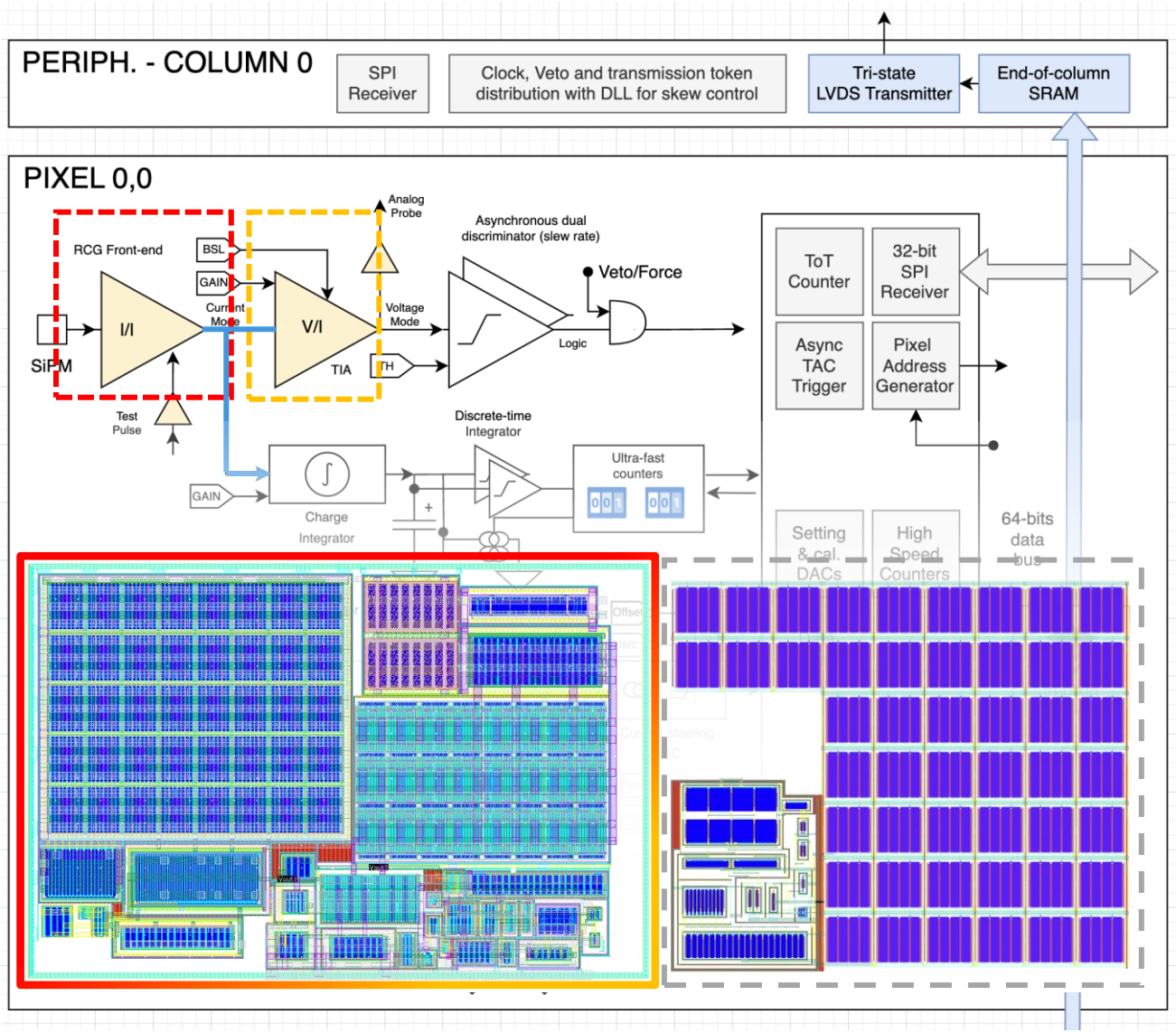
Input stage

- Dual-polarity RCG current conveyor
- Programmable bias currents: CG (30-100 µA) and BOOST (1-4 mA)
- Z_{in} ~ 10-20 Ω

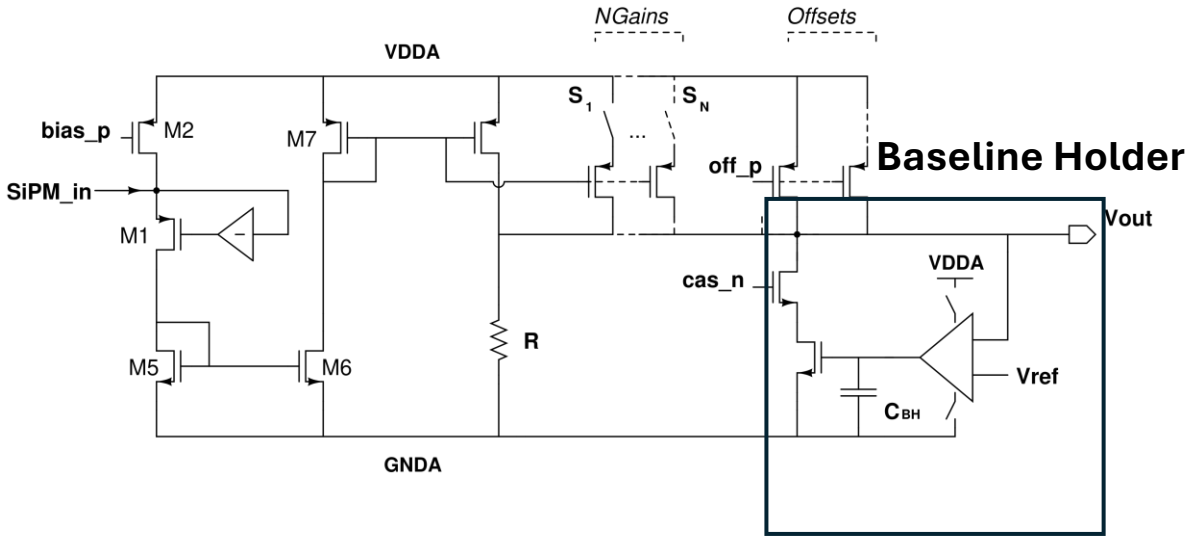
Output stage

- **TIA Res: 2.7 kΩ - 5.4 kΩ**
- **+ Gain settings:** 1/3, 4/3, 7/3 , 10/3 (12PE), 20/3 (6PE)
- **DC coupled**, baseline compensation based on:
  - Gain and CG bias current settings + fine offset adjust(3-bit)
  - Continuous and discrete-time Baseline holder ← Compensates for temperature excursions with low mismatch

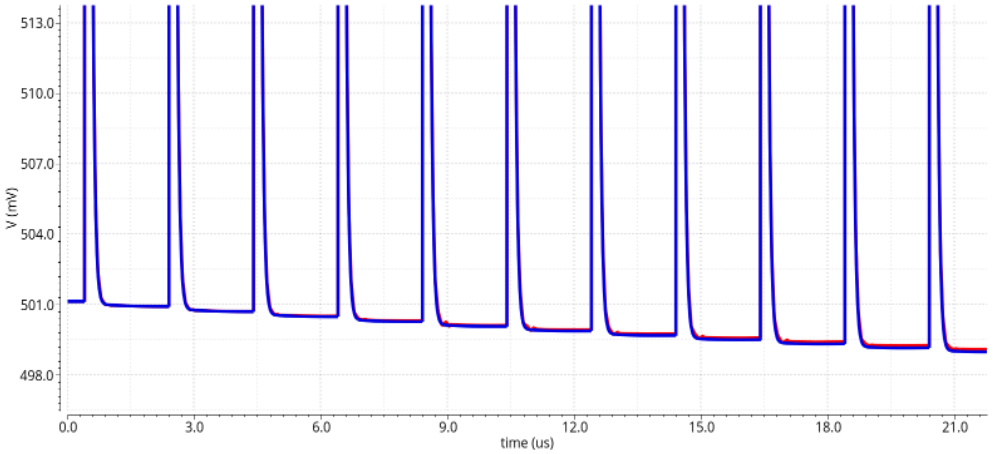
Best timing performance
SPTR < 100 ps



Very Front-End: Baseline Holder

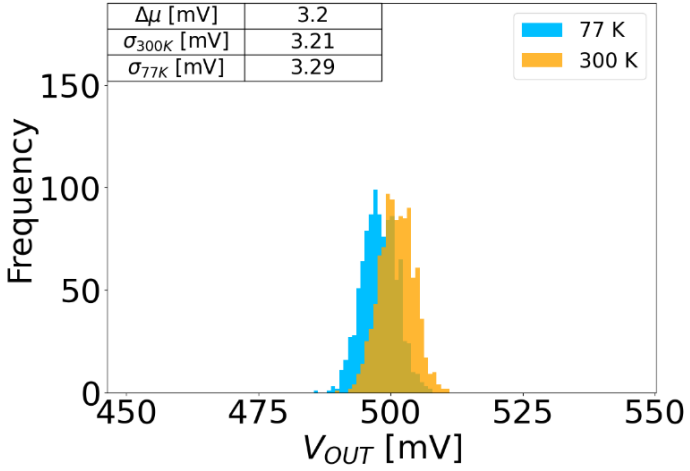


500 KHz Highly piled-up signals

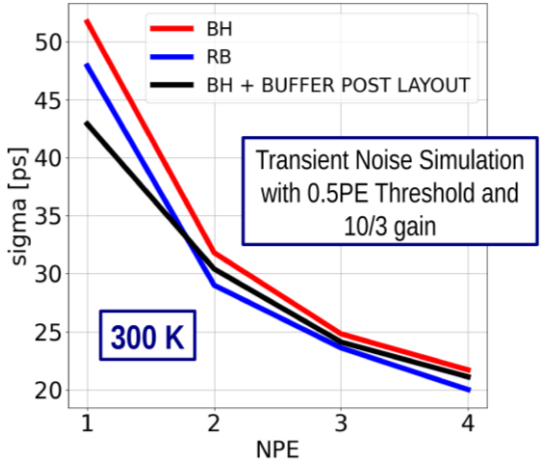


Baseline drift

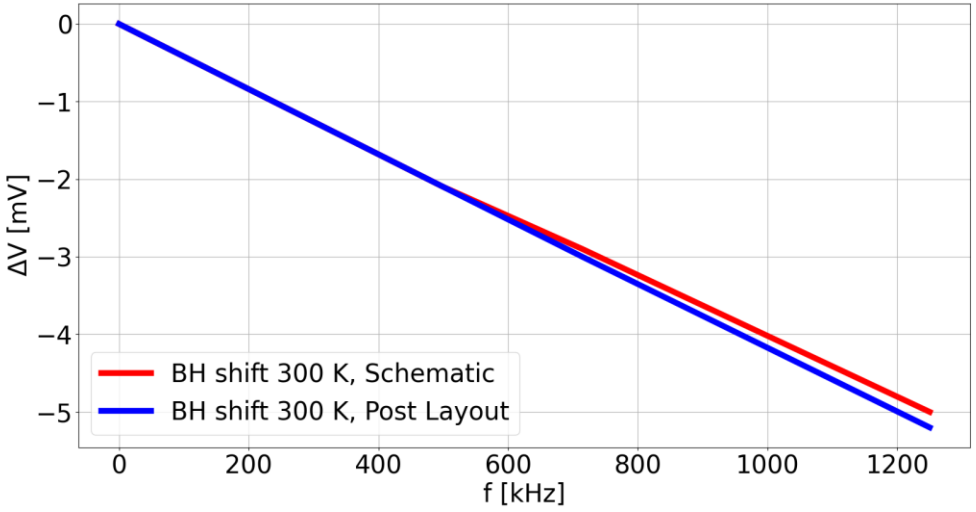
MC Mismatch Postlayout



Jitter Post-Layout



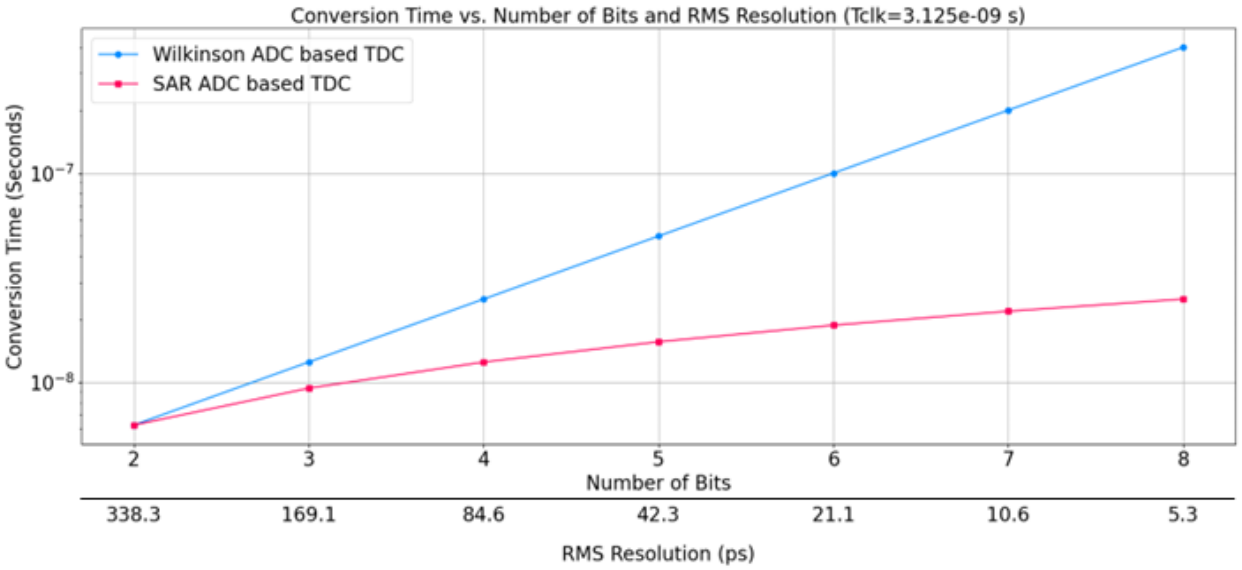
Post-Layout vs Schematic Simulations

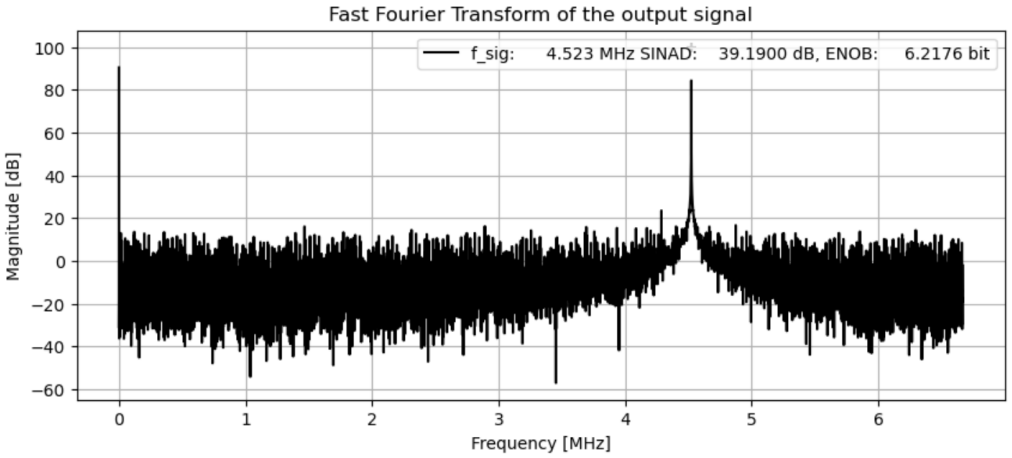


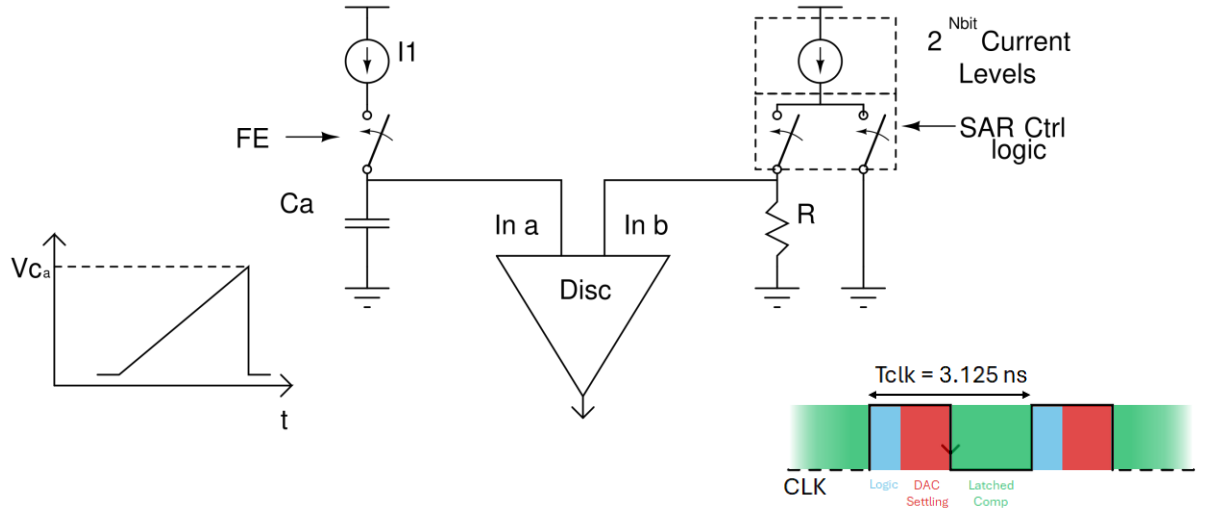
Baseline drift has been minimized

DENEB's Time-of-Arrival Digitization

- **The time-of-arrival measurement** is performed using **4 time-to-digital converters** consisting of an analog interpolator of the main clock signal.
- **The asyncronous edge is used to trigger** a high-precision current source that charges an integrating capacitor.
- The voltage across the capacitor is digitized using two selectable analog-to-digital converters: a **high-linearity Wilkinson converter and a much faster SAR ADC**
- **The 4 units ensures high de-randomization capabilities,** they can be used independently for handling very high event rates or coupled **(2+2) for slew-rate measurement**, for photon couting and time-walk correction

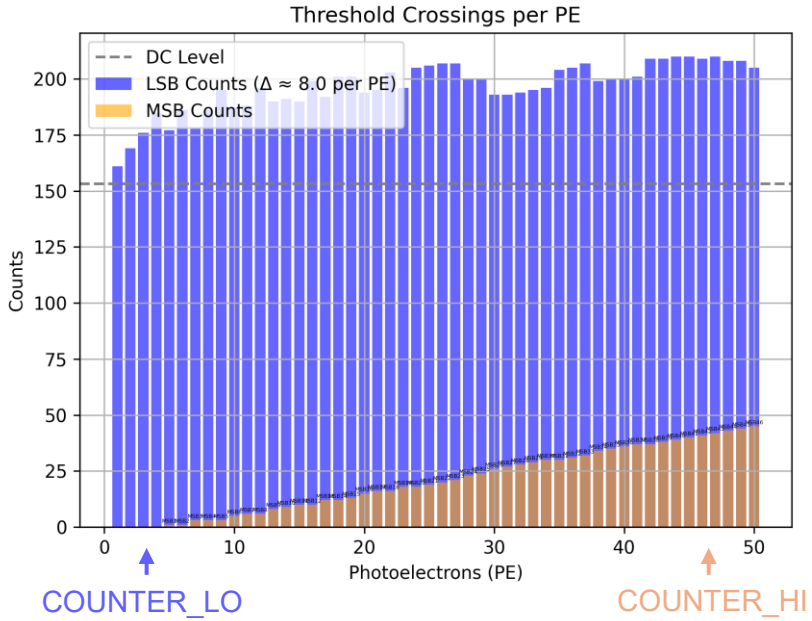






Discrete-Time Charge Integrator

Every channel provides a charge integrator for **photon couting** consisting of a **discrete-time current-to-frequency converter**.
Dynamic Range: 50 piled-up photons and up to 500-1000 integrated photons, 3-4 codes/PE
Residuals: < 0.5 PE
Conversion time ≈ tsig

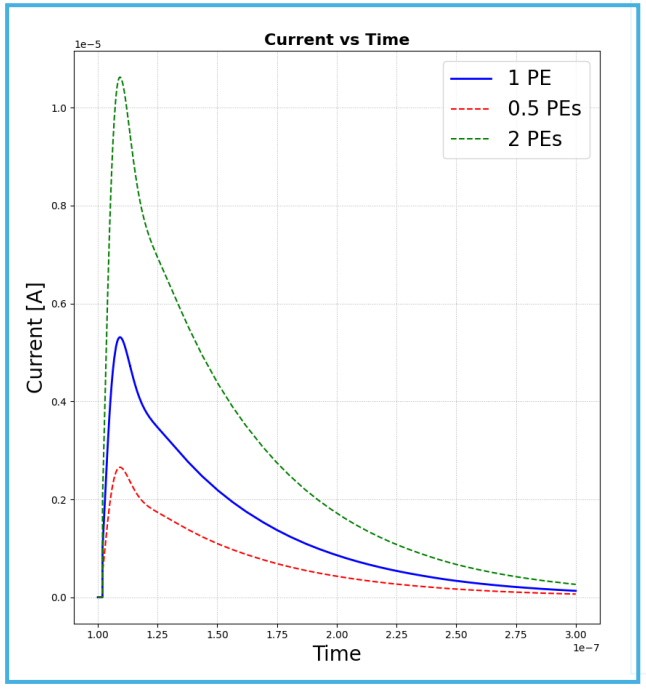


$$N_{PE} = K_{LO}(\#_{LO} - \#_{Baseline}) + K_{HI}(\#_{HI})$$

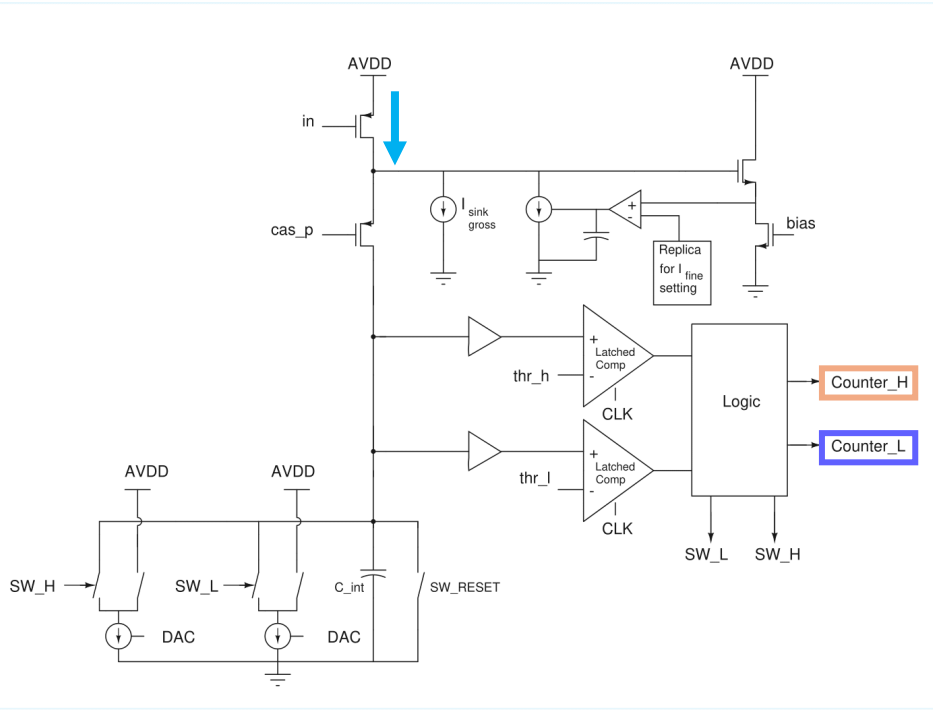
Counts when there is no signal, only due to the DC current

$$\#_{Baseline} = m(\#_{LO-nosignal}) + b$$

I_{in}



By simulating synchronous piled-up photon events a calibration is performed

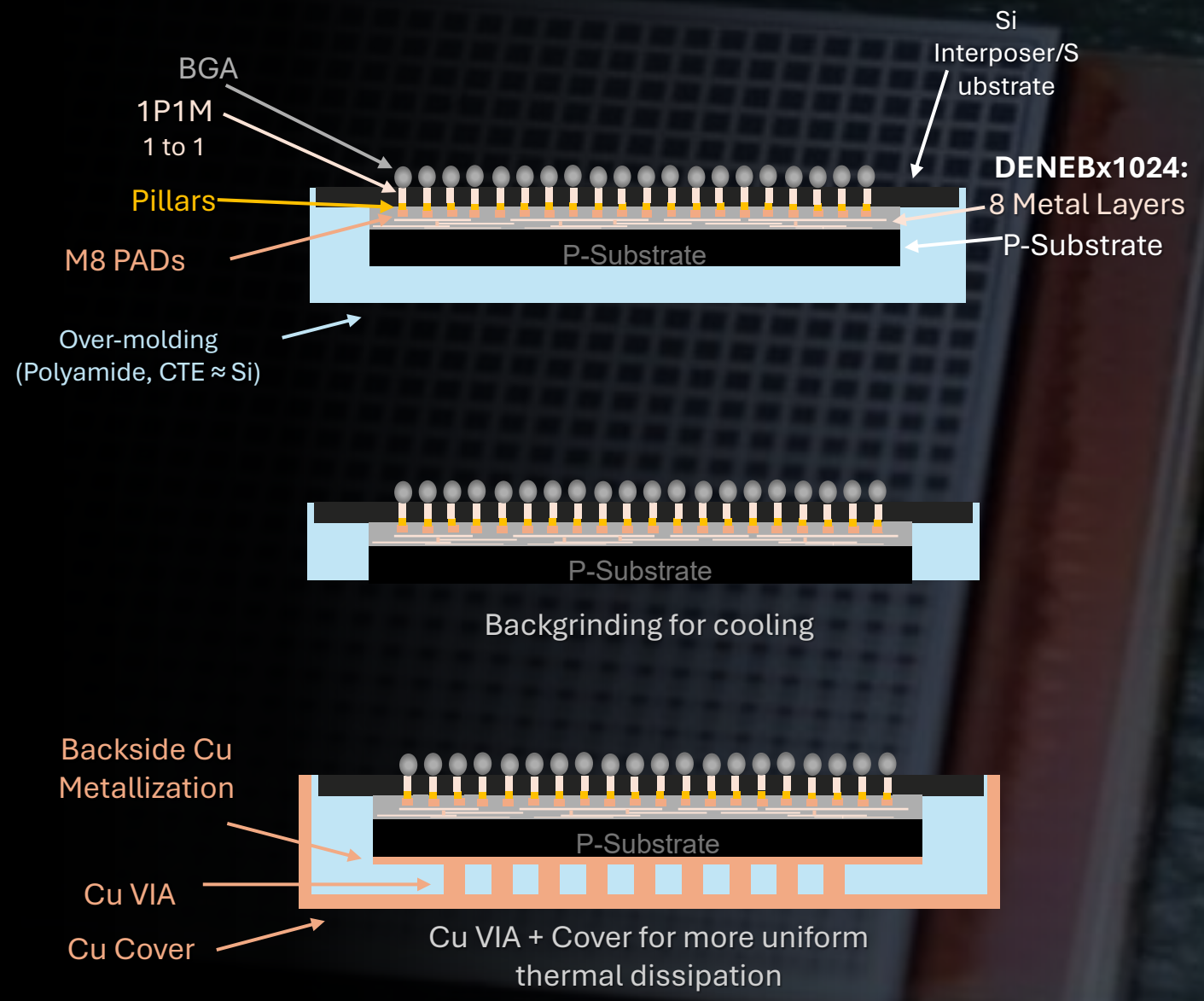


Scheme of the Discrete-Time Delta-Sigma Integrator

DENEBx1024 FOWLP

FOWLP (Fan-Out Wafer-Level-Package):

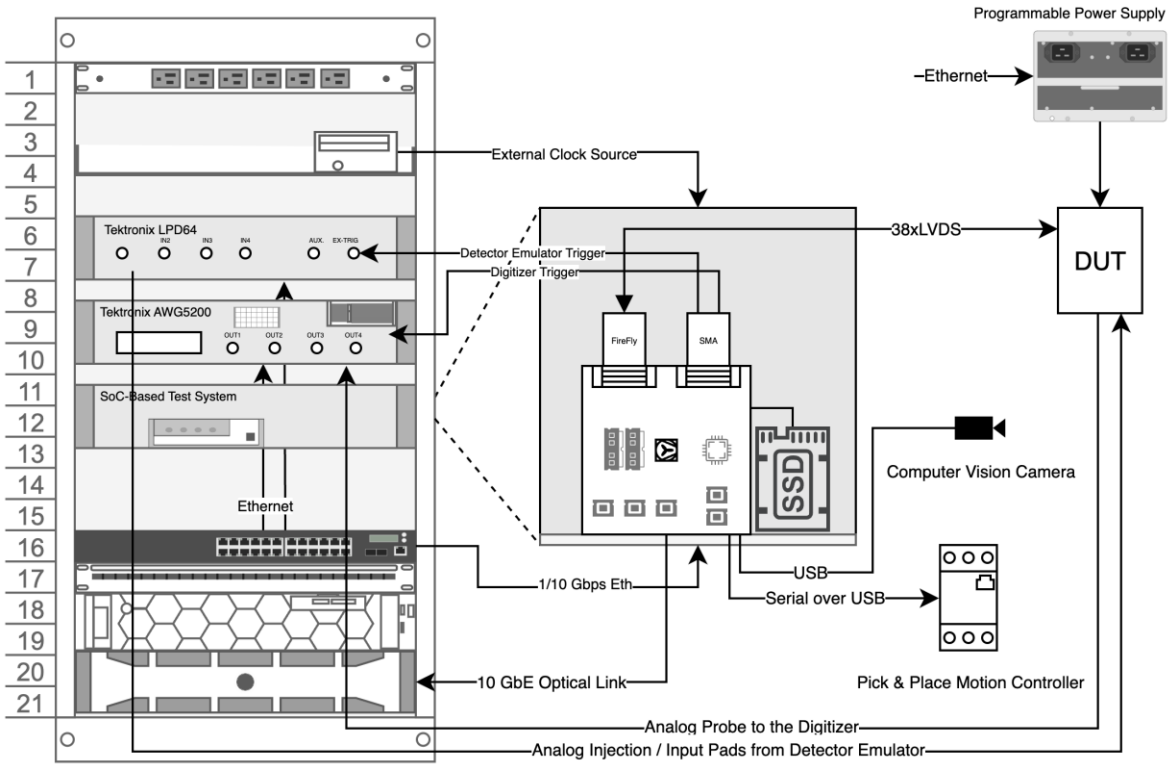
- Advanced semiconductor packaging technology that extends the interconnects beyond the original die size,
- Allowing more space for redistribution layers (RDL) and larger ball pitches.
    - **ASIC: 47 x 36 PADs with 100-500 µm pitch**
    - **Cu pillars**
    - **Si interposer**
        - CTE match, good for cryogenic application
        - RDL: 1P1M
          1 to 1 from top to bottom
    - **47 x 36 BGA with 500 µm pitch**
        - Ready for assembly Chip
- **Signal integrity and thermal simulation** outsourced by the company:
- **Test socket**
- **Probe card**

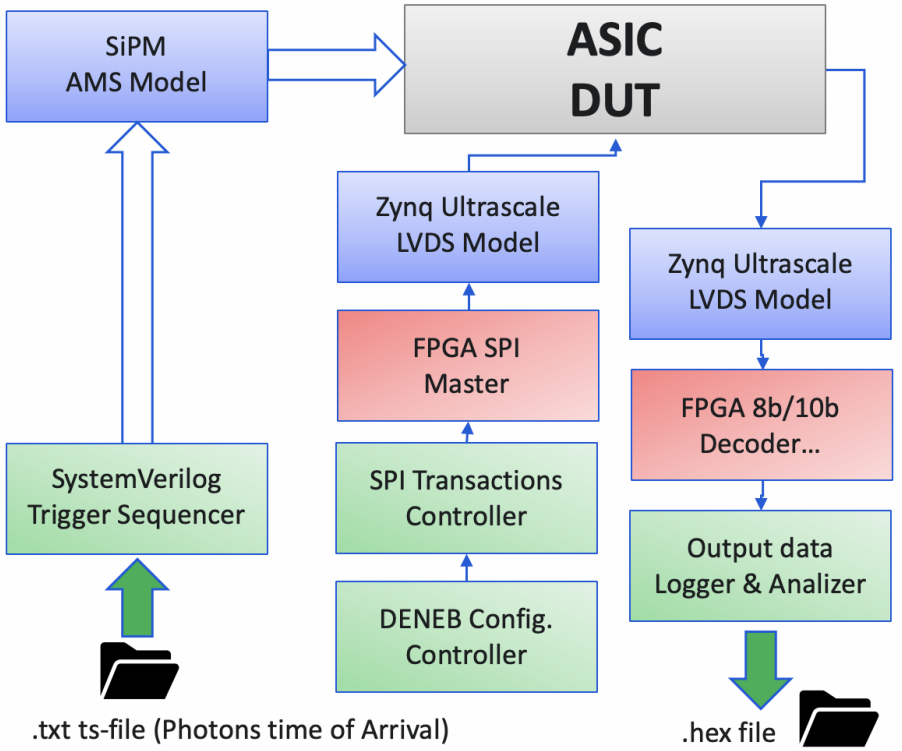


DENEBx1024 Verification and Test Set-up Environments

- In order to reduce the time-to-test of the ASIC upon arrival from the foundry and to verify the design in more realistic conditions, the verification IP (VIP) packaging flow has been used to integrate **synthesizable IPs of the test system into the SystemVerilog object-oriented verification environment.**

- **The test system will be used for the mixed-signal debugging and testing of the ASIC after production**. The arbitrary signal generator will be used as a detector emulator, while the LPD64 digitizer will be connected to the multi-channel analog probe. The ASIC has a SPI-like configuration interface and 32 LVDS/SLVS data links with 640 Mbps data bandwidth.





Conclusions and Timeline

- A **1024-channel SiPM Readout ASIC** for the GRAIN **lAr GRAIN detector at DUNE ND (FNAL)** is under development. The chip will also serve the ALICE3 RICH detector (2035)
- **Key ASIC features:**
  - **1024 channels**, with on-chip time stamp and photon count digitization
  - **300 to 77 K operation**
  - **UMC 110 nm CMOS node**, leveraging key IP blocks developed and tested in the same technology
  - **Time**: 50-100 ps SPTR, TIA, two fast discriminators, and 4 (2+2) TDCs
  - **Charge**: Integrator based on a current-to-frequency converter, can be disabled for doubling the data BW
  - Power gating for low power, and In-pixel programmable delay lines for veto signal generation
  - lpGBT-compatible data transceivers
  - **The chip will come with cryo-compatible 2x3 cm2 package (FOWLP) with** low CTE mismatch
- **Development Status**
  - The chip integration (Digital-on-Top) is ongoing in parallel with new blocks layout design and post-layout validation
  - In the team the verification environment is under development, first verification will follow in 2026
- **A first engineering run is scheduled for Q3-4 2026** to ensure the availability of the DENEB chip for testing in the course of 2026.
- **In 2026/2027, once the cryogenic package is received, the ASIC characterization will proceed** at room temperature and in liquid nitrogen (77K), including optical tests with the SiPM matrix and electrical and functional characterization without it.
- **A second run will follow in Q4 2027**, providing the final version of the ASIC. A second possible package production with modifications is considered to meet the variation in the final version of the ASIC submitted to the foundry in 2027

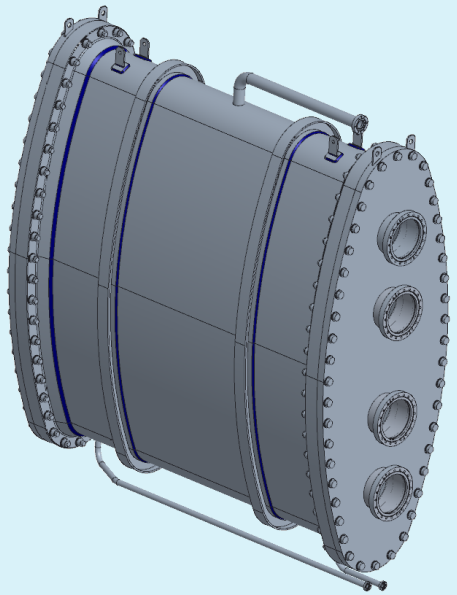
Back Up

GRAIN at DUNE

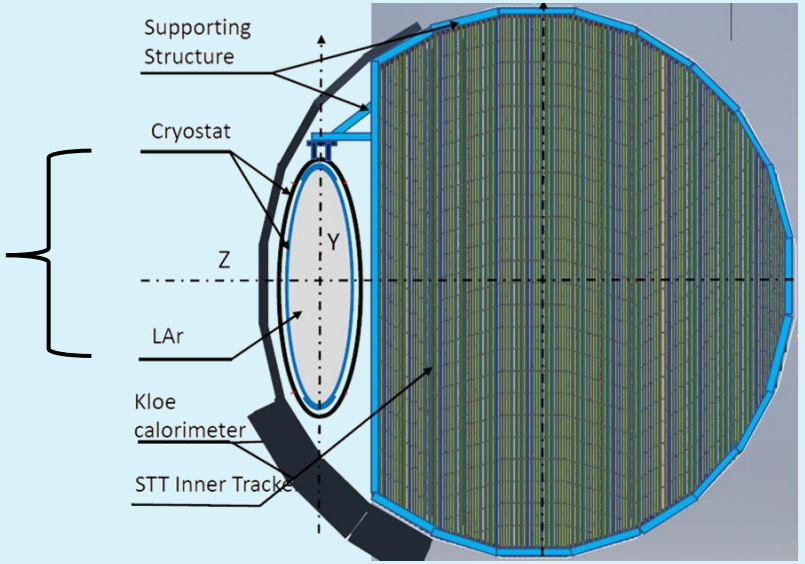
DENEBx1024 is designed for GRAIN

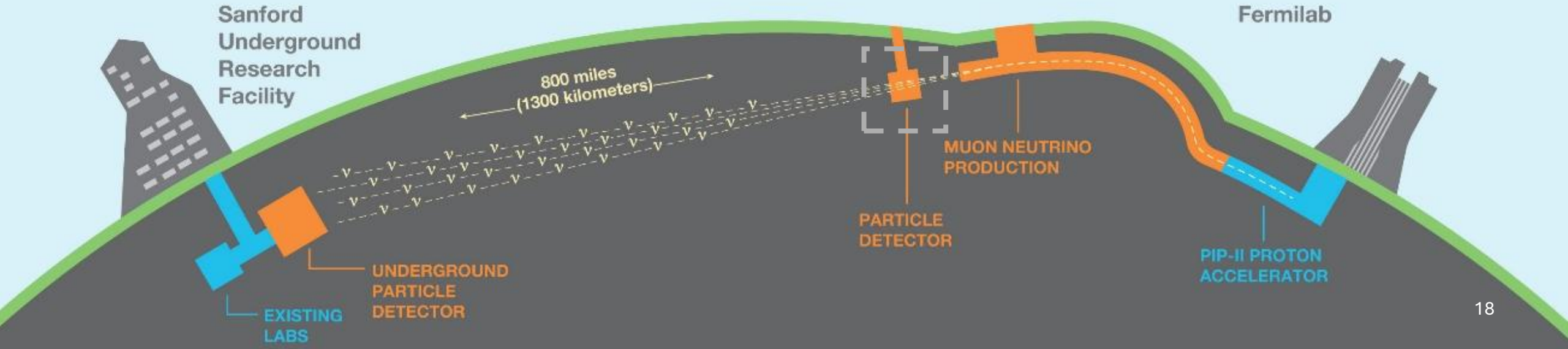
GRAIN:

- **Part of the System for on-Axis Neutrino Detection (SAND) at the DUNE ND facility.**
- **1 ton active cryogenic lAr target.**
- **Novel approach:**
  Neutrino tracks reconstruction through lAr scintillation light detection



SAND at the Near Detector Facility





DENEBx1024 for GRAIN at DUNE

SiPM signals to be readout have a complex structure:

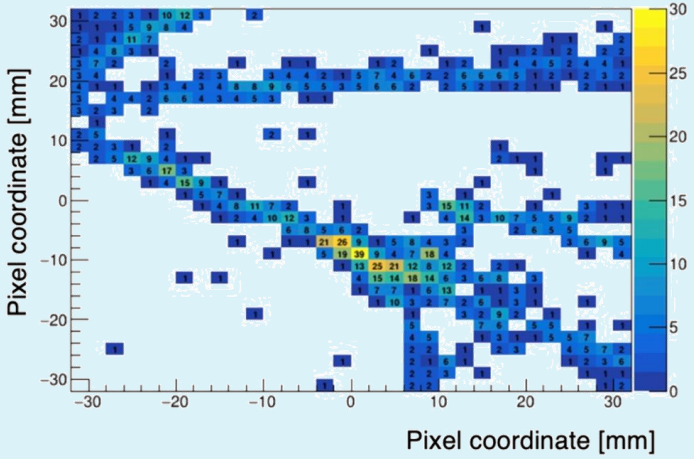
- Single photon and large number of piled-up photons.
- 10-20μs time window, with 1.2 s duty cycle

The ASIC must:

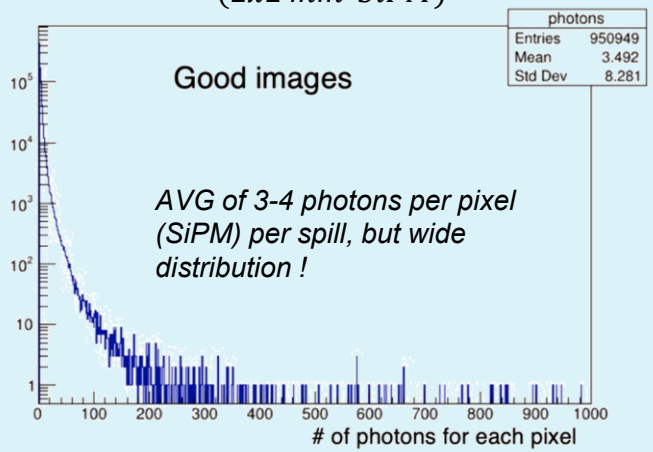
- **Detect single photons** (threshold = 0.5 p.e.)
- **Timestamp** the Maximum Number of Events
- **Count the photons** while minimizing the unintegrated and undigitized charge
- **Work at 77 K and 300 K**
- **< 1 W/cm²** For avoiding bubble generation in the cryostat

Timeline: System-grade ASIC in 2029

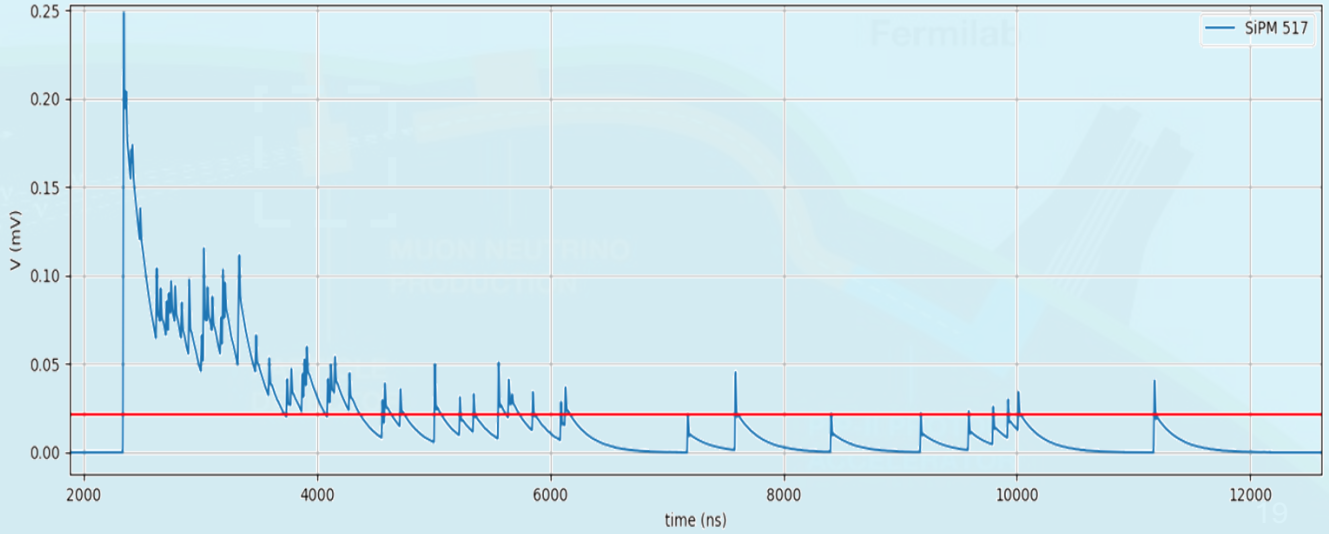
1024 SiPM Matrix simulated light detection during a spill



Single Pixel # Photons Statistics per Spll $(2x2\ mm^2 SiPM)$



Data are distributed into 10/20 us time windows every 1.2 seconds



Design and Verification Strategies

Design Strategies

- **Analog block design:** Cadence Virtuoso with multi-corner simulations using Spectre and AMS
- **Digital design (coding):** Visual Studio Code with SIGASI code linter plugin, Synopsis Design Compiler and Library Compiler
- **Digital integration:** Cadence Innovus **(Hierarchical Digital-on-Top)**
- **Logic radiation tolerance:** Hamming-encoding for FSM states and TMR for configuration registers and crucial blocks such as the reset logic. Redundancy on the full-chip-level reset signal.
- **Sign-off:** Cadence Virtuoso
- **Source Control:** Source control managed by INFN private Gitlab istance with pull-request system and CI/CD for code linting on commit.

Verification Strategies

- **System-Level simulations:** Python behavioral simulation model with GUI and interfaces for Monte Carlo physics simulation software
- **Analog Verification:** Cadence Spectre and AMS simulator
- **Digital Verification:** Cadence Xcelium with AMS,
  object-oriented System-Verilog testbench with coverage optimization.
- **Top-level verification:** digital verification environment integrated with FPGA IPs used as Verification IPs (VIPs) and Verilog-A models for the SiPM matrix. Radiation effects simulated injecting bit-flips in the SystemVerilog testbench.

Verification Strategy and Coverage Assessment

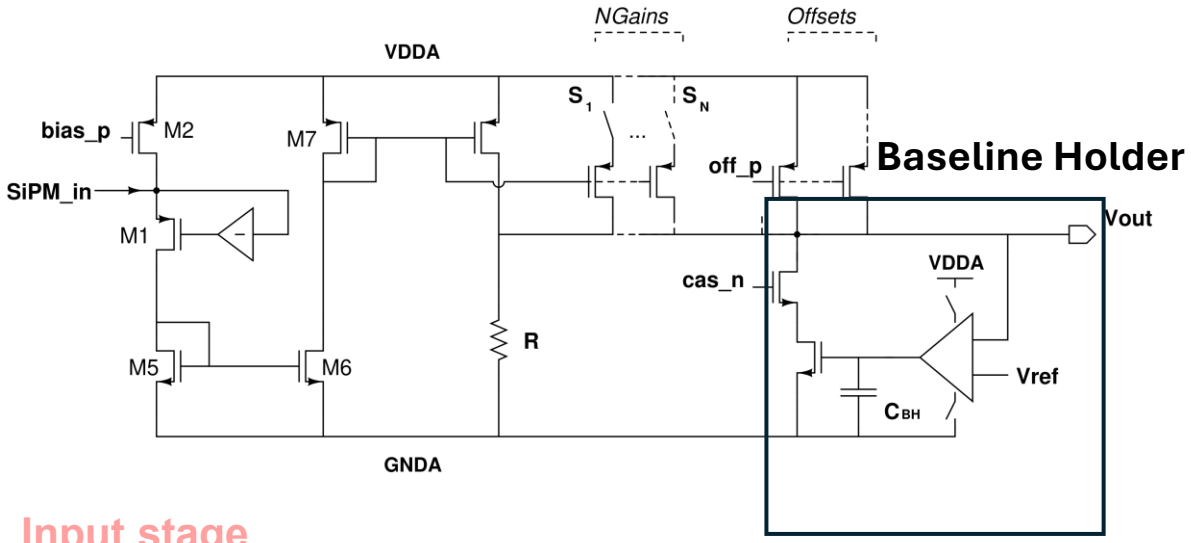
On the mixed-signal post-synthesis top-level:

- **Xcelium (event driven) + Spectre / Fast SPICE** Configuration testing, test of the digital logic and test of TMR and radiation tolerance systems using random (SEU + async signals) + sequential (configuration values) sampling of the space of parameters. Coverage supported by sequential testing of all the allowed configurations.

- **Xcelium (event driven) + Spectre / Fast SPICE** Injection of SiPM discharge signals using a Verilog-A model of the sensor driven by a Time-of-Arrival time series generator. Coverage supported by generating a very large amount of photon hit patterns in different configurations of the ASIC.

- **Subset of runs on the post-layout design of the pixel**
- **Reduced subset of runs on the post-layout design of the top-level**
- **Computing power ensured by a > 512 core, 8-16 GB/core virtual machines on HPC cluster**

Very Front-End: Baseline Holder



Input stage

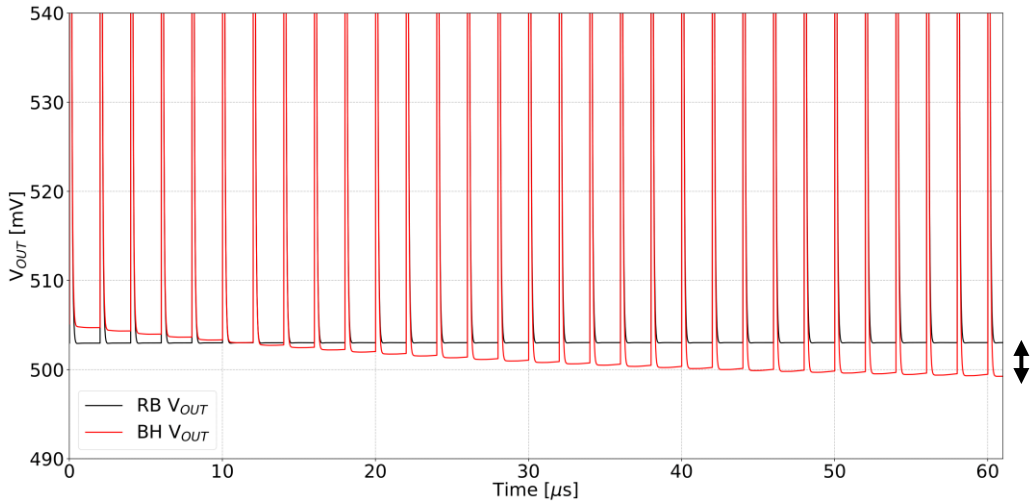
- Dual-polarity RCG current conveyor
- Programmable bias currents: CG (30-100 µA) and BOOST (1-4 mA)
- Z_{in} ~ 10-20 Ω

Larger signals will reduce the impact

Output stage

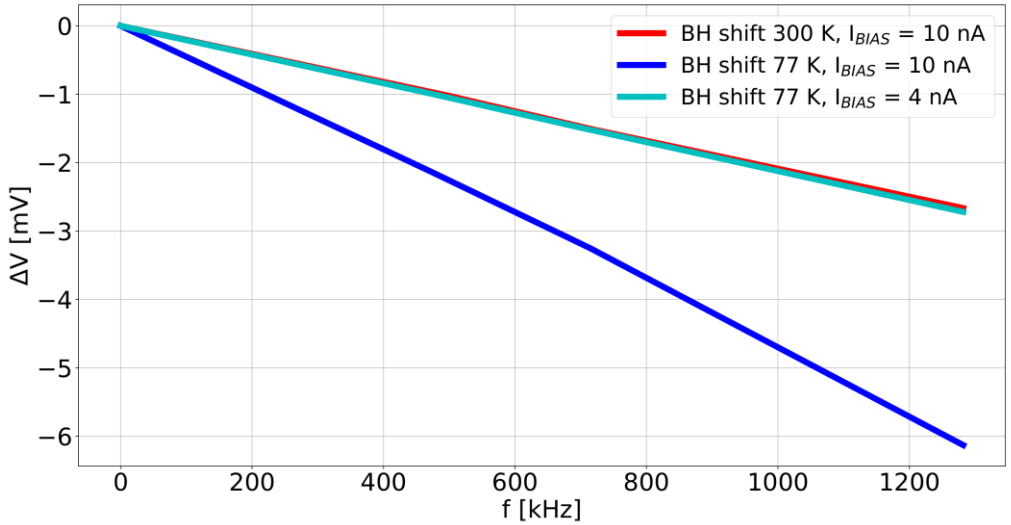
- **TIA Res: 2.7 kΩ - 5.4 kΩ**
- **+ Gain settings:** 1/3, 4/3, 7/3 , 10/3 (12PE), 20/3 (6PE)
- **DC coupled**, baseline compensation based on:
  - Gain and CG bias current settings + fine offset adjust(3-bit)
  - **Continuous and discrete-time Baseline holder** ← Compensates for temperature excursions with low mismatch

500 KHz Highly piled-up signals



Baseline drift

Drift in a 20 µs window at different pulse frequencies



Baseline drift has been minimized

ALCOR SPTR Results Highlights

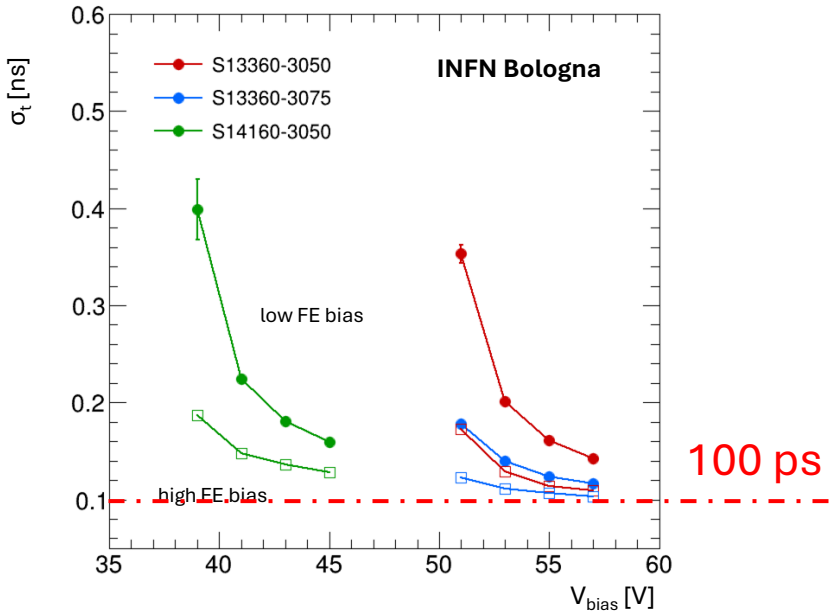
First FE version (no BH, lower gain, i.e. worse jitter) has been tested at room temperature

dRICH Collaboration effort for testing the prototypes

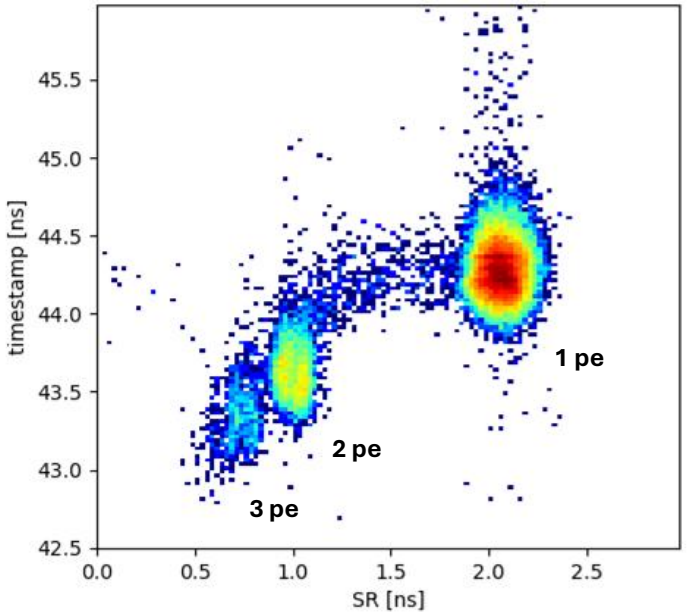
- ALCOR v2 and ALCOR v2.1 characterized in Torino and Bologna laboratories
- Validation with laser set-up and test-beam at PS (2023-2024)

Single Photon Time resolution

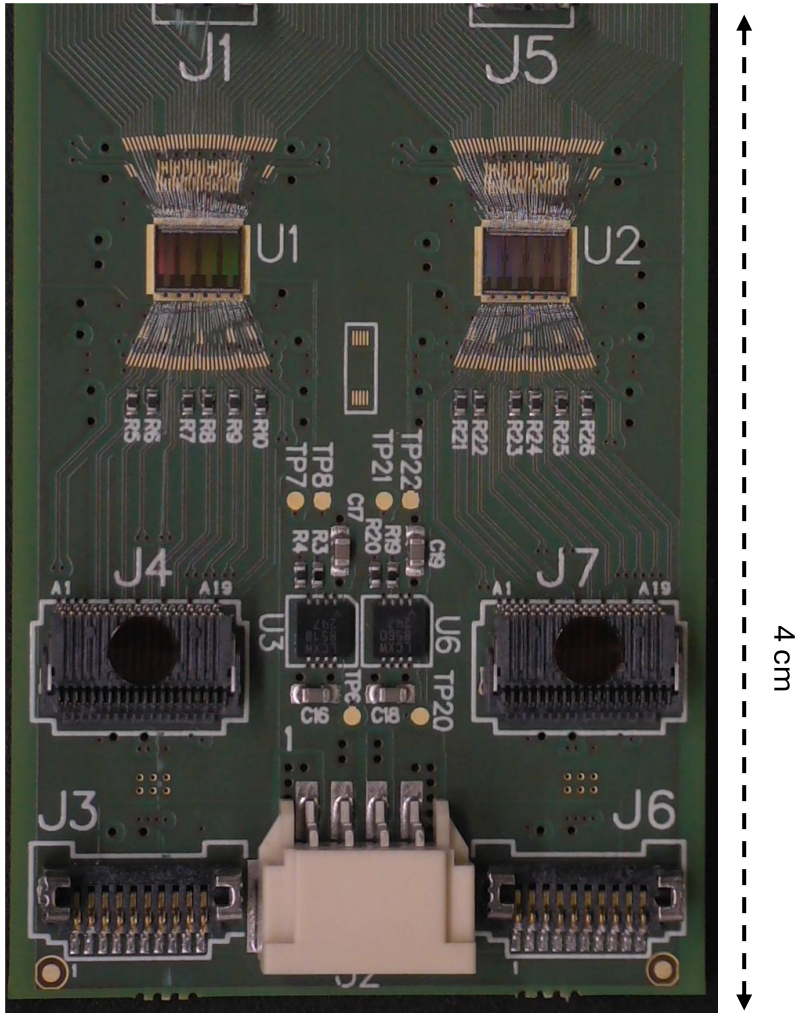
300 K!



Time walk correction (SlewRate mode)



Designed using specifications close to final FEB: very similar space constraints and same number of channels (64)



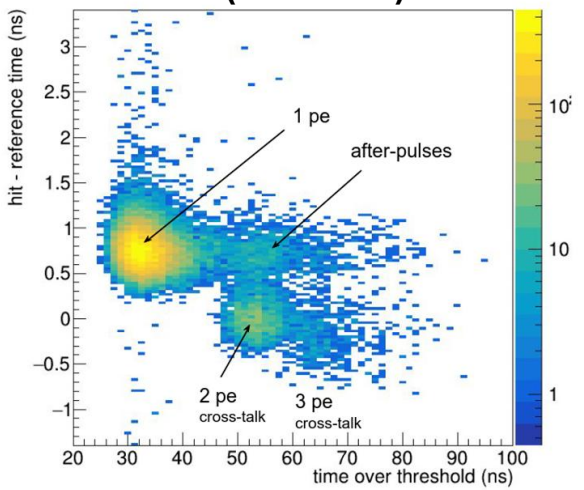
If you are interested, check this presentation:
R. Preghenella «The ePIC_dRICH SiPM photodetector unit»

ALCOR SPTR Results Highlights

- **SPTR is strongly dependent on**
  - **The SiPM type/size**
  - **Overvoltage**
- *If hp*: $\sigma_{V-Noise} = 1\ mV$, *Jitter < 100 ps*
  SP Slew-rate > 10 $\frac{mV}{ns}$ i.e. $\boldsymbol{V_{peak-SP} > 100\ mV}$ ⟷
- **SPTR Temperature dependence**

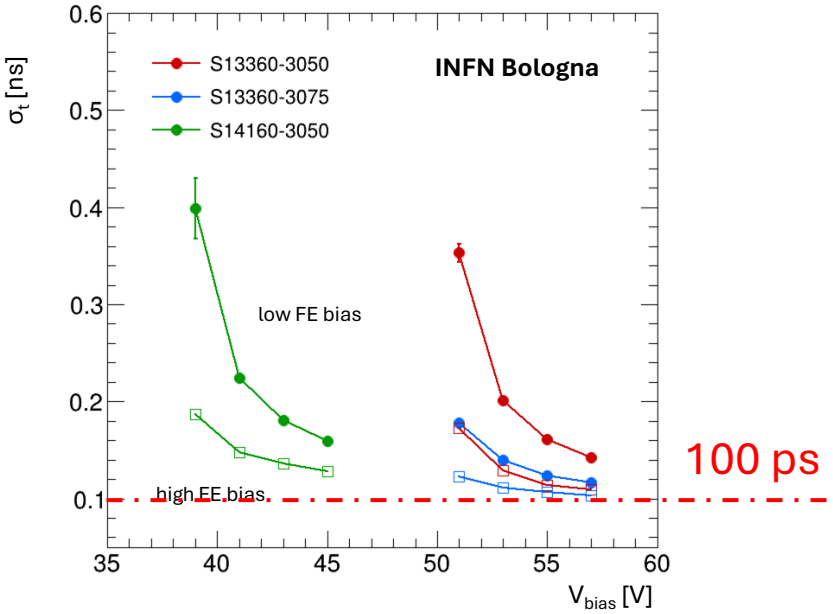
Lower dynamic range (< 50), but only in the TIA!
No impact on the time-walk correction, which is critical only for low PEs
Charge measurement is not affected!

Time walk (ToT mode)

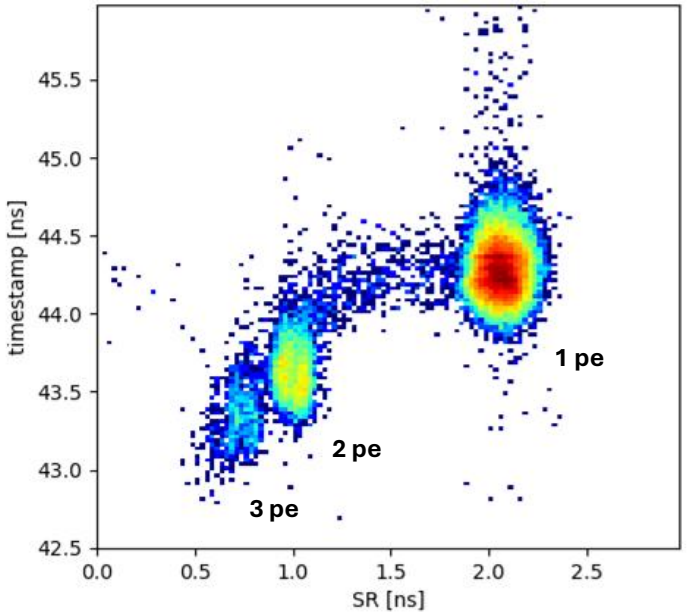


Single Photon Time resolution

300 K!



Time walk (SlewRate mode)

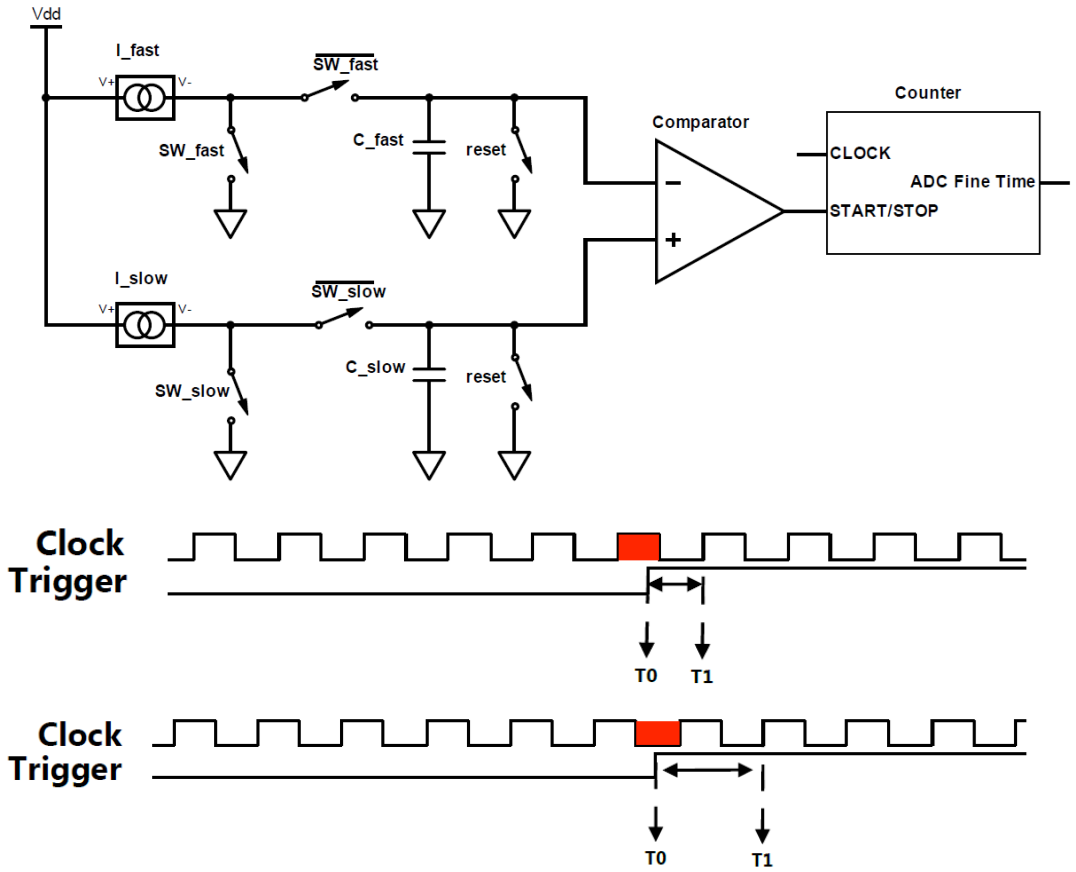


Slew rate mode provides

- **Better separation than ToT** and consequent **better Time-Walk correction**
- Cons: Slew rate mode requires **2 edges fine time stamp**, i.e., **2 TDCs busy per event**, i.e. it doubles the dead time of the pixel

ALCOR Time-to-Digital-Converter

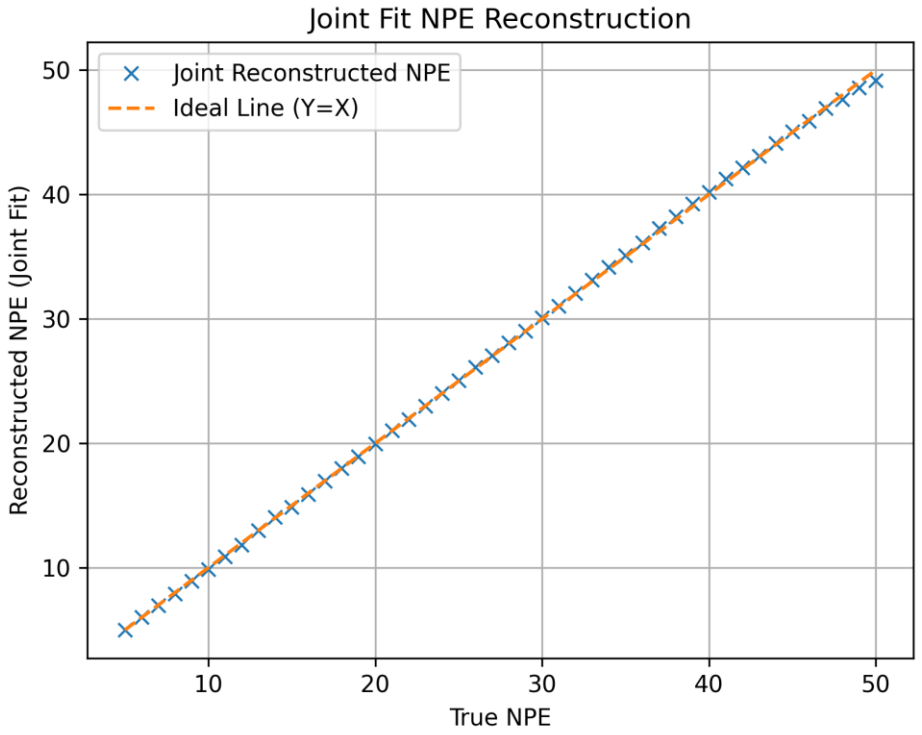
- **Coarse time: 15-bit clock counter**
  - Timestamp saved at the rising /falling edge of the Trigger signal
  - Coarse time resolution is limited by the system clock frequency
- Time conversion performed by **TDC** based on **analogue interpolation** (9-bit fine time):
  - **Fast ramp:**
    Constant current to charge C_{fast} → measure phase between event trigger and clock
  - **Slow ramp:**
    Smaller constant current to charge C_{slow} → counts clock cycles until V_{Cslow} and V_{Cfast} are equal
- I.F. 64 or 128 → LSB = 25-50 ps @320 MHz
- Measured time interval: 0.5 - 1.5 clk period
- TDC conversion time: [200, 600] ns
- 4 TDCs per pixel for **event derandomization**

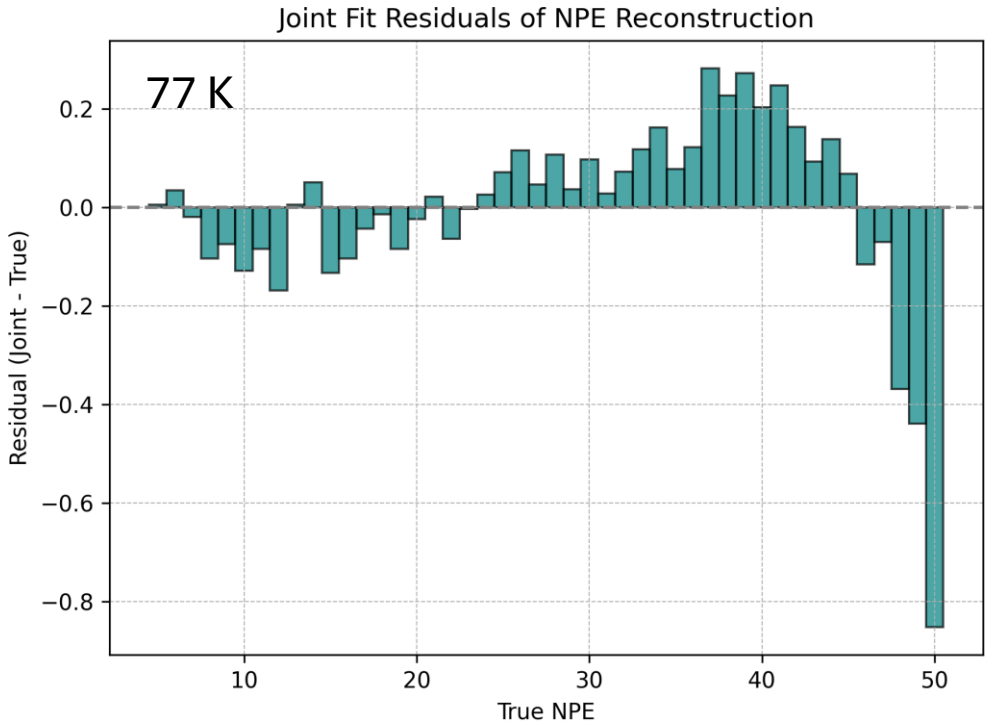


T_0 Before Clock Falling Edge:
If the trigger (T_0) occurs before the clock's falling edge, the fine time is measured between T_0 and the next clock rising edge (t_1).

T_0 After Clock Falling Edge:
If the trigger (T_0) occurs after the clock's falling edge, the fine time is measured up to the *second* rising edge. In this case, the full timestamp is obtained by adding one clock period to the fine time.

Discrete-Time Charge Integrator





$$N_{PE} = K_{LO}(\#_{LO} - \#_{Baseline}) + K_{HI}(\#_{HI})$$

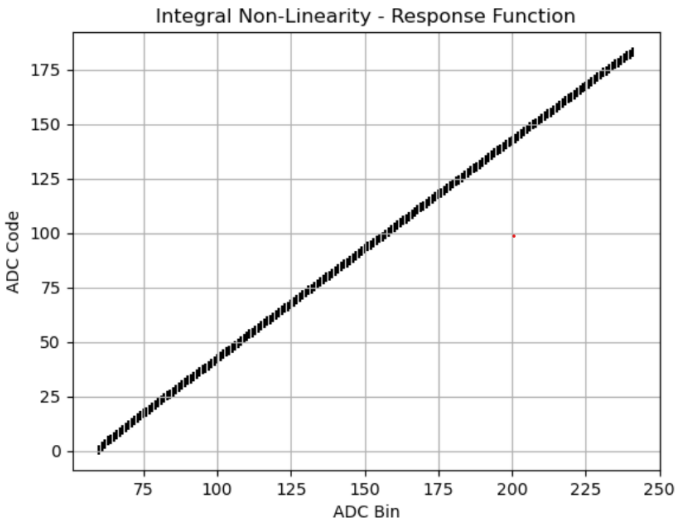
$$\#_{Baseline} = m(\#_{LO-nosignal}) + b$$

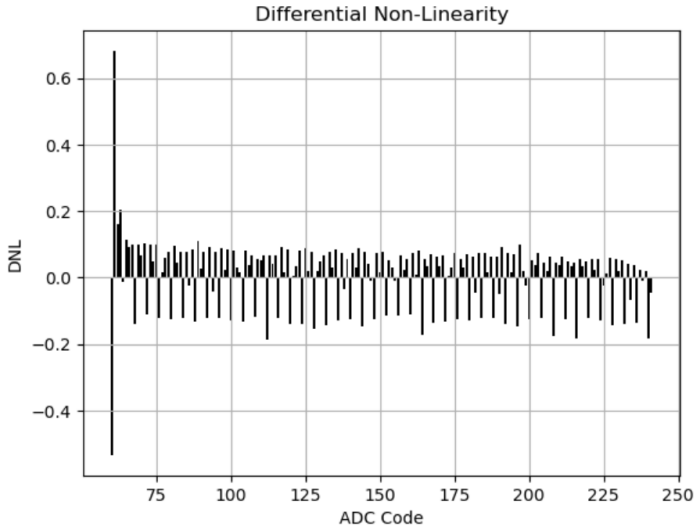
Counts when there is no signal, only due to the DC current

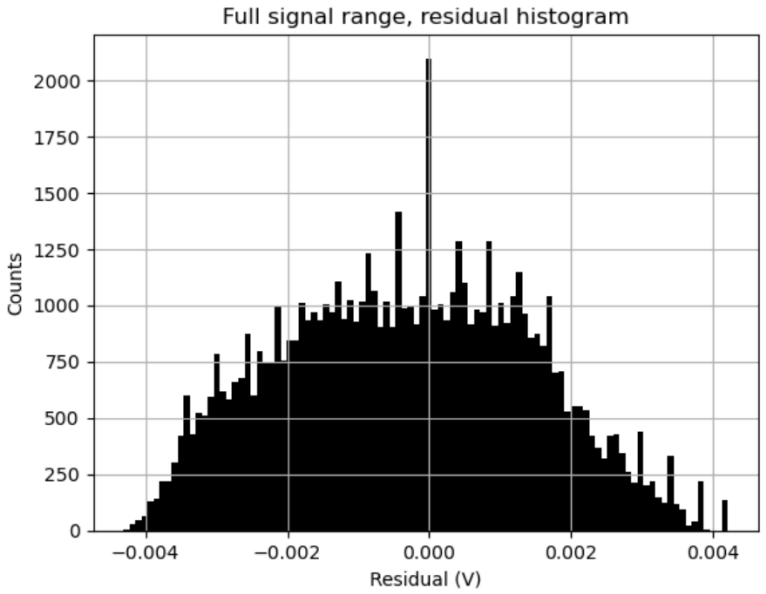
Residuals show the error in units of PE on the reconstruction when different piled-up photons are presented to the integrator

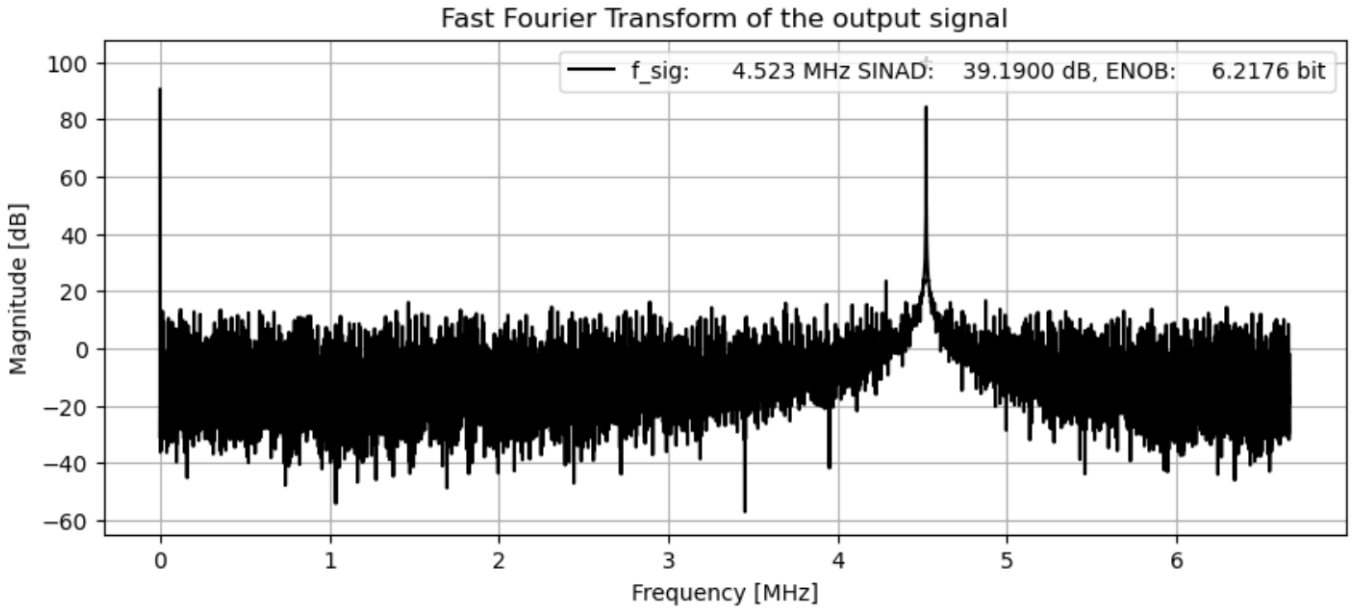
Time-of-Arrival Digitization

- The SAR ADC embedded in the DENEB TDC is a novel block that is being characterized for linearity, SINAD, ENOB etc.
- The time resolution is limited by the jitter of the front-end, so the conversion speed is maximized, at the cost of a resolution limited to 5-8 bit. (8 bit ⇒ 17 ps RMS).

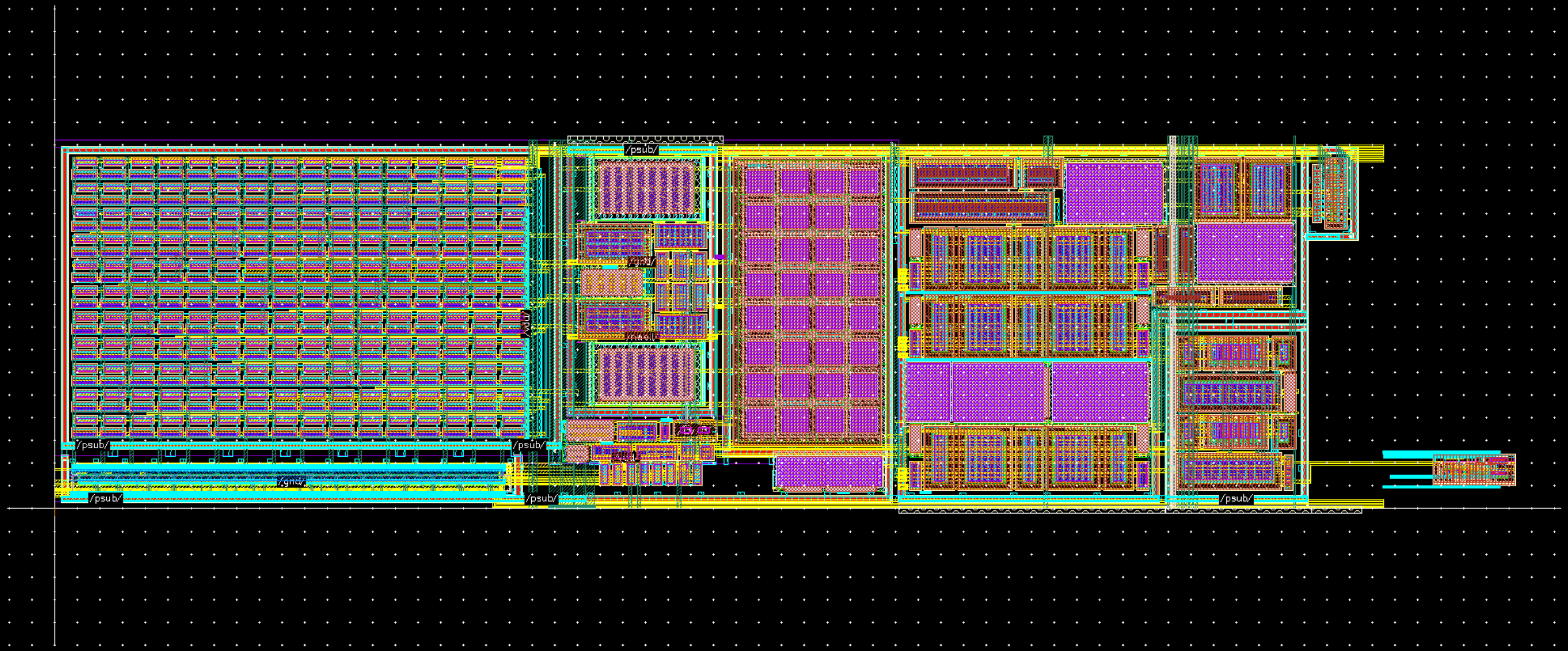








Improvements from ALCOR TDC



Improvements from ALCOR TDC

≈ 100 µm

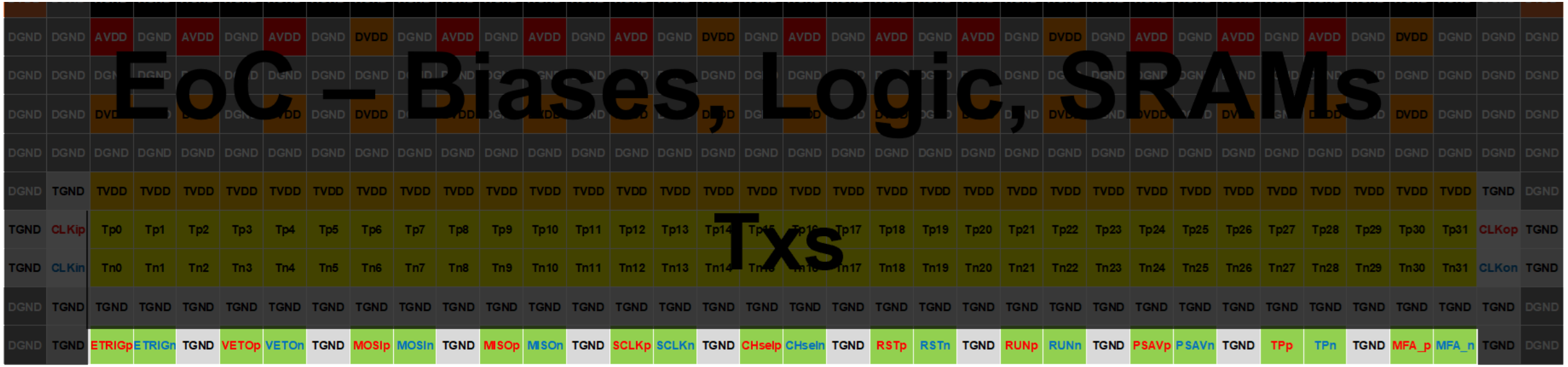
In the ALCOR TDC, the Time-to-Amplitude Converter (TAC) and Wilkinson current sources occupy approximately **one-third** of the total TDC area.
The design includes **128 current sources**, enabling an interpolation factor of **64 or 128.**

The **new TDC architecture**:

- **Maintains** the area footprint for both **SAR** and **Wilkinson** operation modes.
- **Enhance flexibility and functionality** of the system.
- **Accept faster conversion times**

≈ 300 µm

DENEB's Control IOs



External Trigger

External VETO

SPI

Clock

Channel select

Full Reset
- TDCs
- Logic
- SPI

The Global Run State signal is used to trigger the acquisition state

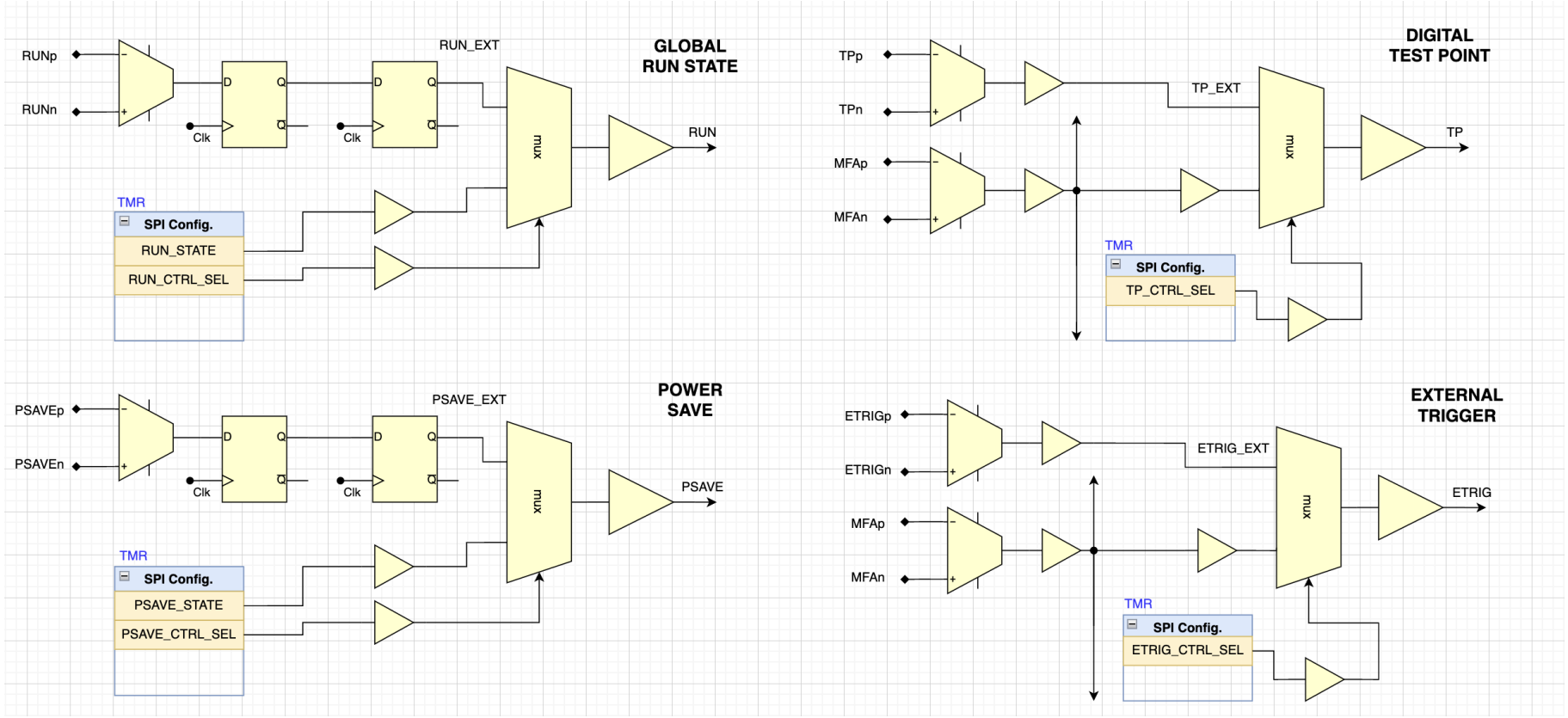
The save solution is used for triggering the power save mode

Asynchronous signals

The VETO signal can also be injected through the MFA input, or it can be produced internally using a multi-tap delay line starting from the clock signal. This mode is suitable for the use with the lpGBT and the LHC-derived clock.

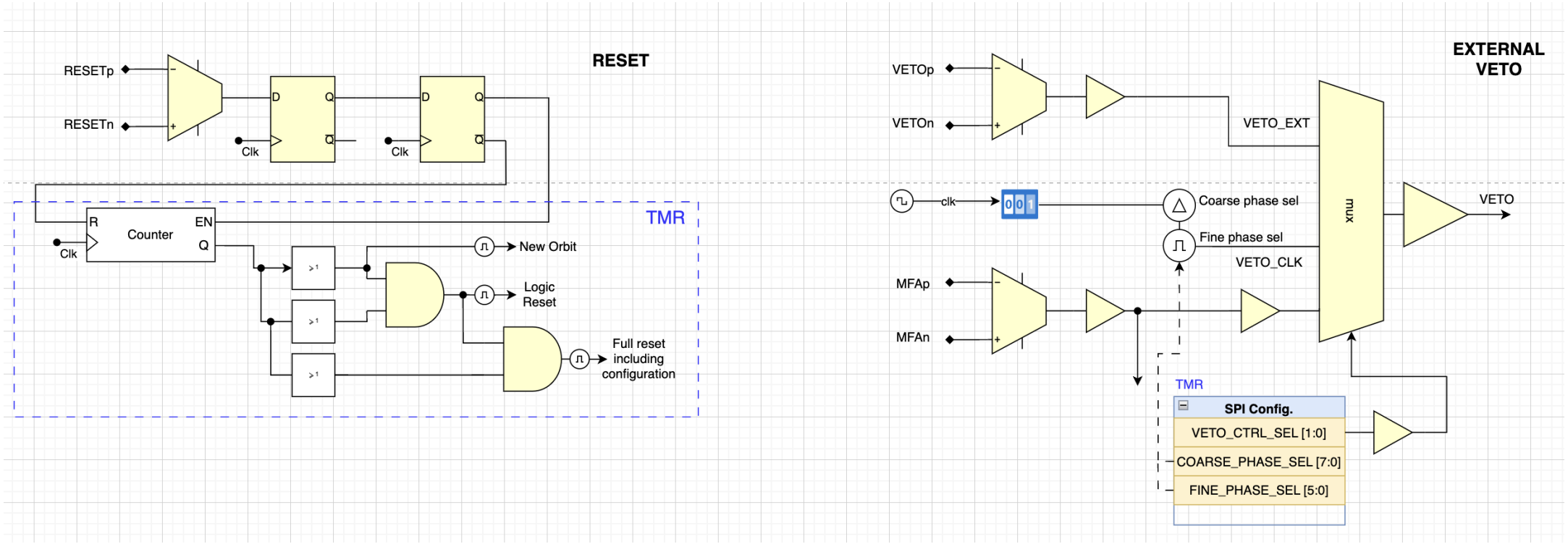
Auxiliary IOs

- The Global Run State signal is used to trigger the acquisition state of the ASIC and it is controlled by a SPI register (non timing critical) or a dedicated differential pair (timing critical, synchronous).
- The SPI is based on a robust timeout-based protocol that doesn't require the CS dedicated line.
- The digital test pulse and the external trigger are asynchronous signals that can be injected using a dedicated input pair, or the "multi function asynchronous (MFA)" input during the testing phase.



Veto and Reset

- The reset signal is synchronous and handled by a dedicated state machine. The duration of the trigger signal (in a similar fashion with the ALCOR chip) triggers the “new orbit” function (reset the coarse counters of the TDCs), the “logic reset” or the “full reset” that includes the SPI configuration. The logic is triplicated with TMR for SEU protection.
- The external VETO can be injected using a dedicated pair, the MFA input or it can be produced internally using a multi-tap delay line starting from the clock signal. This mode is suitable for the use with the lpGBT and the LHC-derived clock.



Pixel Logic

- The pixel logic is based on 4 independent event buffers that collect the timing, charge, ToT and ancillary data, formatting them to a couple of 57b event words.
- These words are appended to an output buffer and transmitted to the end-of-column logic using a daisy-chain data bus that is re-synced and arbitrated in every pixel of the column
- The charge word can be disabled for performing slew-rate only photon counting with more efficient exploitation of the bandwidth of the 320 Mbps / 640 Mbps transceivers.