Updates on Timing and DAQ

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11/11/2025 DUNE Italia

Highlights of the ICD

Key differences from other subdetectors:

- SAND timing requirements are ***more stringent*** and touch the limit of what the Dune Timing System can deliver

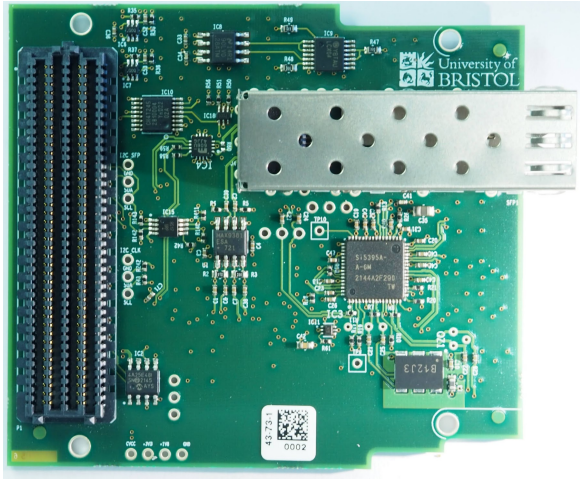
- SAND is requiring precision time information on the beam and advance beam spill information ***beyond*** what the accelerator had originally *planned to deliver*

Open questions for integration

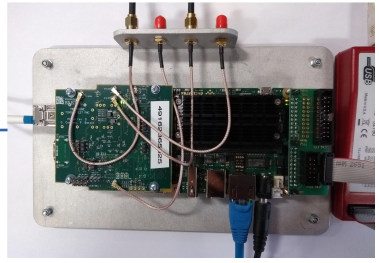
- The GRAIN electronics requires an early-warning signal to control the power gating feature of DENEB
- There is a requirement from the accelerator side to know how early this warning needs to come
- Exact knowledge requires having both the full power chain and the ASIC available, which will take too long
- A value of 4 ms was indicated as a (conservative) estimate

Test at scale

- The DAQ WG procured and distributed the timing reference mezzanine last CM
  - Also got two that are compatible with AMD Ultrascale+ FPGAs
- As far as we know, DTS plans to procure most of their hardware **before end of FY26**
- Any incompatibilities or issues discovered afterwards would be difficult to solve
- We encourage subsystem to start testing these boards with their back-end solution!



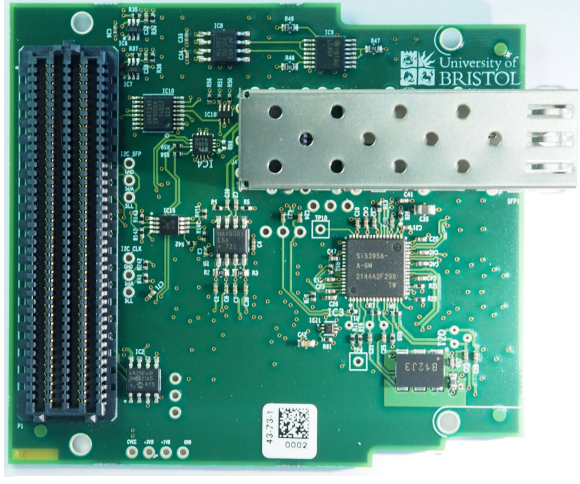
ECAL FERS Backend integration

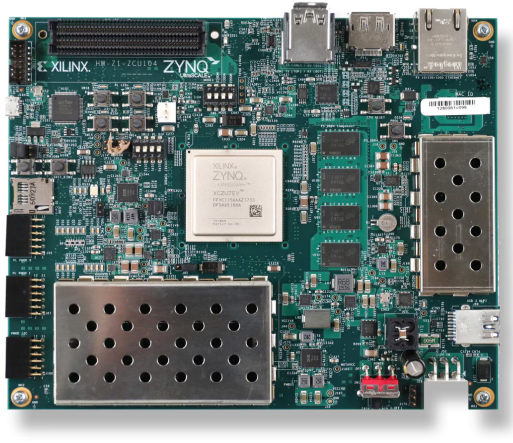


- CAEN tentatively agreed to integrate DTS/DAQ endpoint in their FERS concentrator, which is the candidate back-end for ECAL
- Need to make progress on the integration

Endpoint test

- One student in Bologna will start an integration test
- Uses ZCU104 carrier, we have two
- We will configure one as master and the other as endpoint.
- A third device is needed to test difference between endpoints. One is available in GE





DAQ Endpoints

- New estimates for the number of DAQ endpoints:
- GRAIN: 8 endpoints (on the GWIB)
- ECAL: 4 endpoints (on the FERS concentrator)
- Tracker: not known yet, backend not mature enough: O(10-100)

- Both ECAL and GRAIN are few enough to be on one fiber splitter (1:8), allowing somewhat lower jitter within the detector.

Progress made this year

- Progress writing the Interface Control Document for DAQ
- Progress on writing the TDR Chapter
- Better understanding of accelerator timing issue, though some details of the issue remains open