Tech-FPA National PhD Program

2^{nd} Year Admission Presentation

Candidate: Marco Toffano (XL cycle - Electronics)
Supervisors: M. Bellato, J. P. Zendri

Tuesday, September 16^{th}, 2025

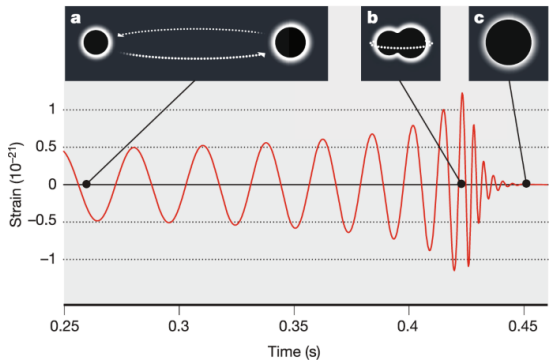
Università degli Studi di Padova

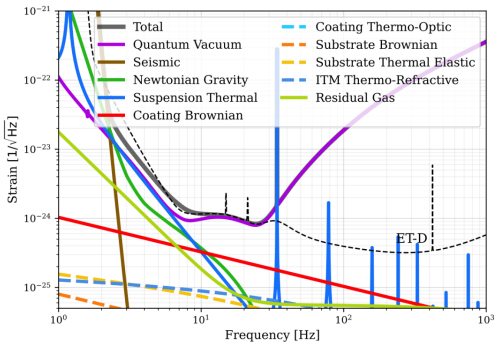
INFN PADOVA
Istituto Nazionale di Fisica Nucleare
Sezione di Padova

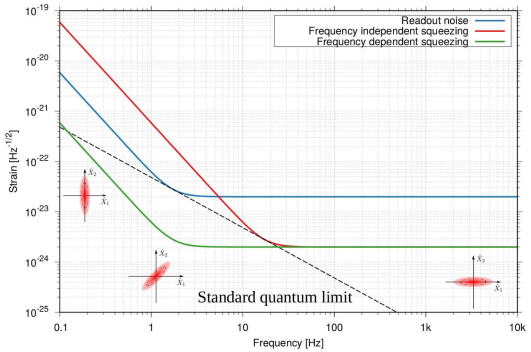
Research topic

Interactions of massive celestial objects cause ripples in spacetime, travelling at c.

VIRGO, as well as LIGO and future ET, all rely on precise timing of the various actuators across detector for *active noise compensation*, allowing accurate measurement of the resulting spatial displacement here on Earth's surface.







Detection of low-frequency events is challenging due to several disturbing factors: seismic, newtonian, thermal and *quantum vacuum* (shot & radiation pressure).

↪ Ultimate sensitivity is enhanced by injecting *squeezed light* in the interferometer dark port... However, **strict requirements** apply:

Angular jitter of the squeezing ellipse $< 10\ m\text{rad}_{RMS}$ (1Hz ÷ 100 kHz)

- Met by locking in frequency & phase the various lasers employed for SQZ light generation. Practically, this is done with highly-pure DDS-based RF sources operating @ different frequencies (4 MHz, 80 MHz, 1.26 GHz, etc.)

Objectives

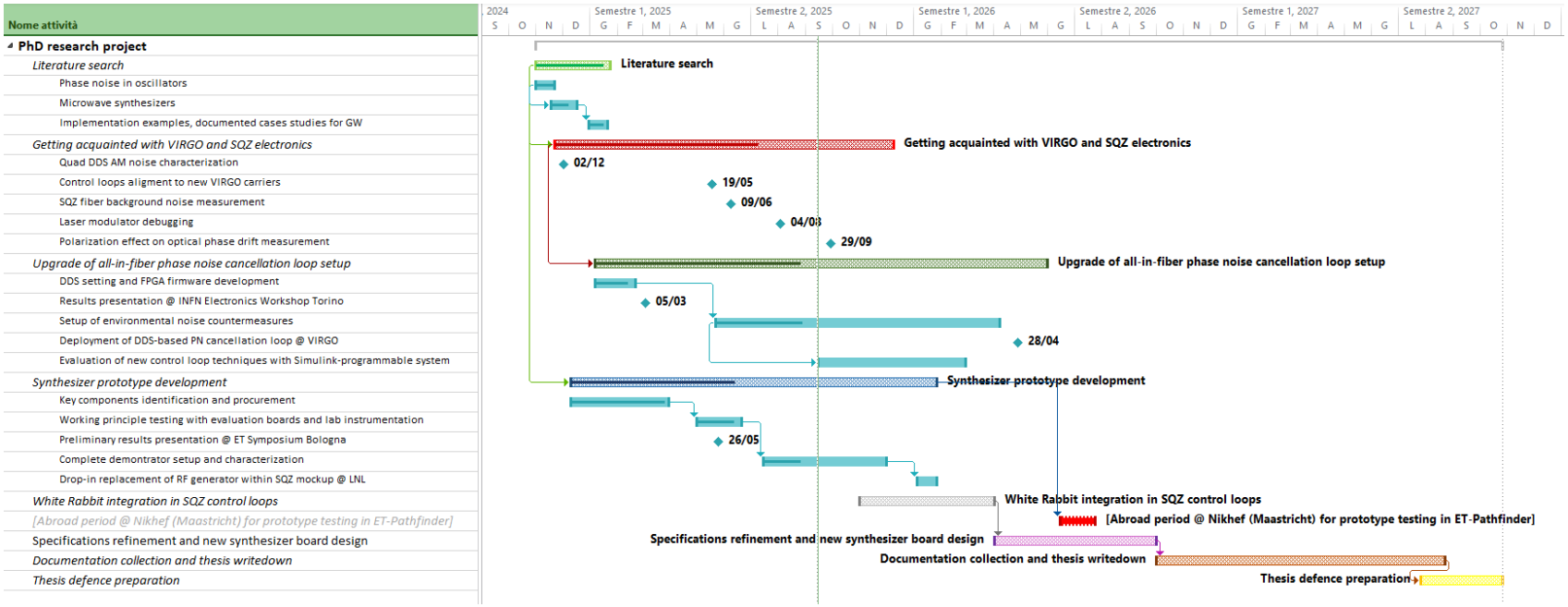
Integrated commercial solutions present high-end characteristics in terms of spectral purity within the frequency range typical of the world of telecommunications....

1. Design a custom frequency synthesizer with state-of-the-art phase noise performance suited for VIRGO
2. Prearrange external modulation capabilities for integration with VIRGO carrier stabilization loops
3. Grasp requirements for new ET electronics, which are yet to be defined
4. Practice measurements and characterization methods to validate synthesizer performance in situ
5. Observe the influence of environmental factors typical of the detector and develop strategies to rule it out as much as possible

> More specifically, the aim is to understand whether, starting from an hypothetically "noisy" reference signal that also directly provides synchronization for the synthesizer, the quality of the programmed output tone is still compliant with the target detector sensitivity

→ Currently, the most likely candidate for synchronization in ET is White Rabbit, which is already in use at CERN & has been partially tested also at VIRGO

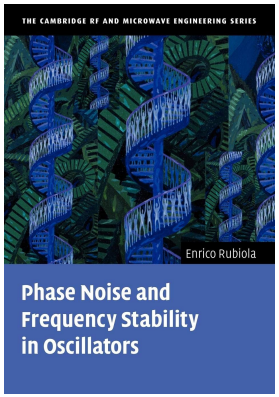
Overall research activities planning

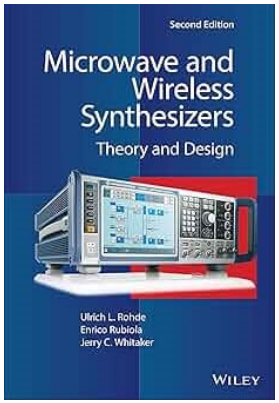


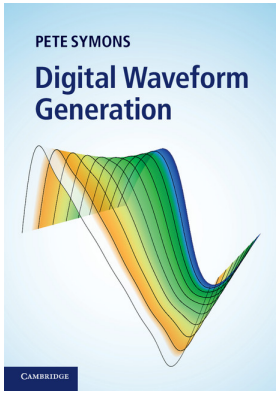
[N.B: Higly simplified Gantt chart - just to get a work outline...]

Research activities - 1

First and fundamental step - literature review on the topic:

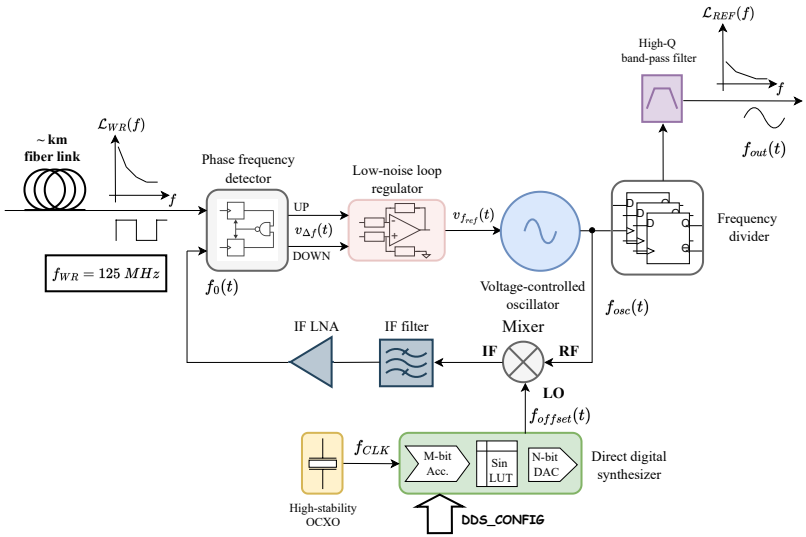






Architecture definition & procurement of components and evaluation boards:

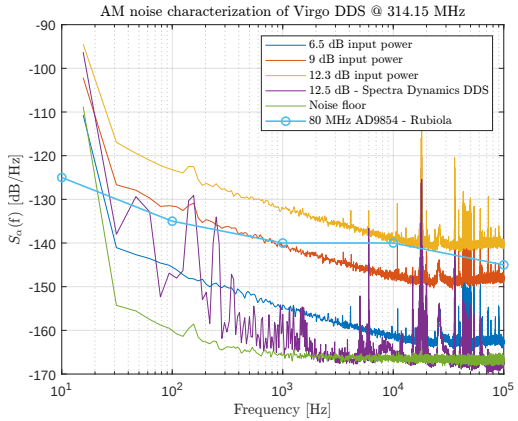
- integrated low-noise VCO, mixer, IF filter & LNA
- high-performance DDS
- digital FPD & frequency divider
- ultra-stable OCXO (PCB-mount version still underway)
- resonant-cavity filter (built @ INFN mechanical workshop)



Research activities - 2

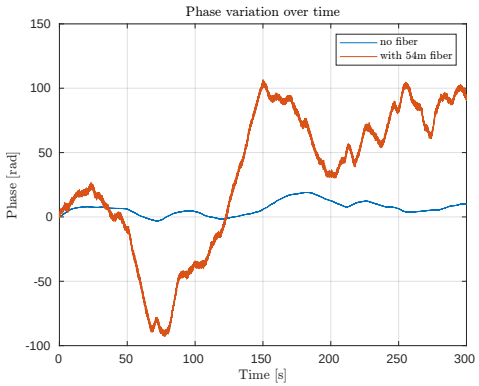
Hands-on with current RF carriers generation system developed at INFN Padova:

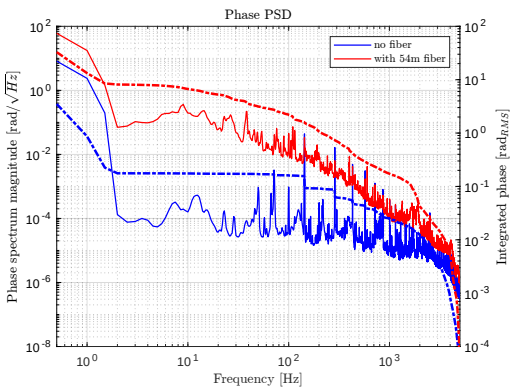
- amplitude noise characterization
- extra filtering of phase truncation spurs
- analysis of applied circuit techniques for low noise
- exact measure of Wenzel OCXO reference phase noise with cross-correlation analyzer

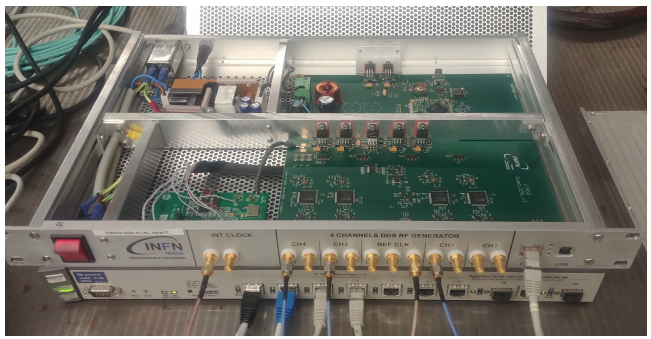


In-situ measurement of optical loops small-signal trasnfer function with VNA:

- with & without thermalization $\Longrightarrow$ temperature gradient effect
- monitoring residual phase drift with increasing SQZ-ITF fiber length (ascribed to polarization shift, but to verify)







[logbook.virgo-gw.eu/virgo/?r=66951]

Research activities - 3

Electro-optical setup for *all-in-fiber noise cancellation loop* requires an analog RF generator with external frequency modulation command

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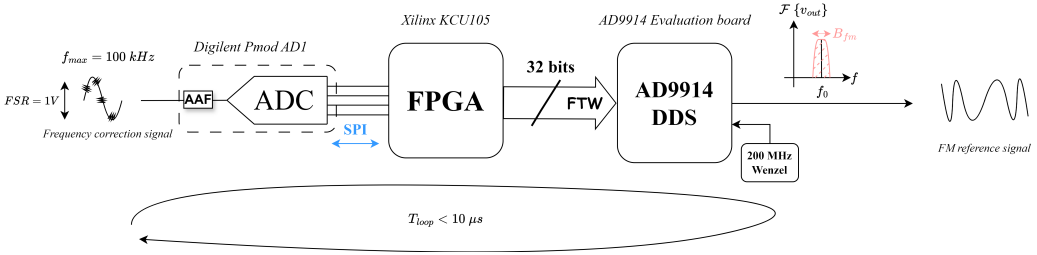
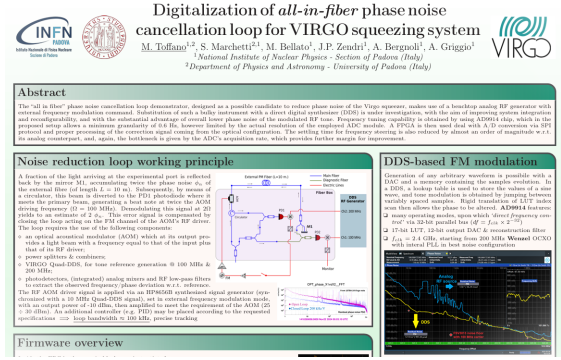
Evaluating substitution with DDS and associated control logic





- Modulator latency cut by 5 times: increased noise rejection bandwidth
- Limitation of this setup: $df \approx 8$ Hz in typical application ($k_{FM} = 10$ kHz/V)

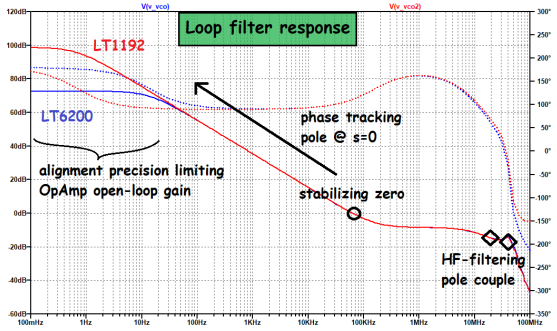
Due to ADC resolution (12 bits), not DDS minimum frequency granularity: if the modulating signal is directly provided digitally, the lower limit $f_{clk}/2^{n_{acc}}$ can be exploited!

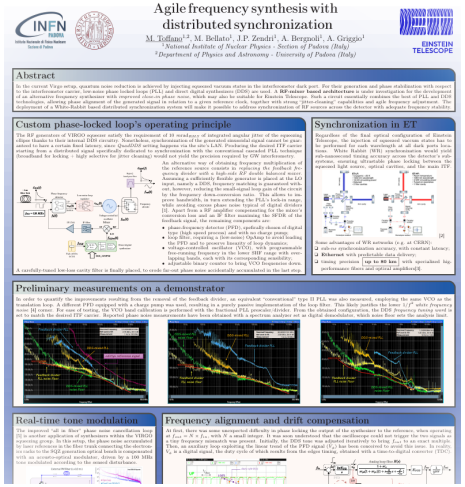
⇓

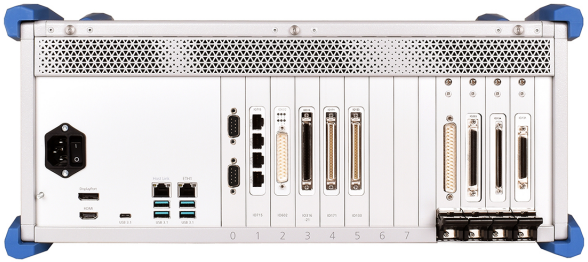
A versatile, almost-continuous modulation capability is **essential** for the final synthesizer realization → high-performance 16-bit DAC with user-selectable DSP functions selected as local oscillator for the translation loop demo

Upcoming activities for 2^{nd} year

- Extensive testing, debugging, fine-tuning and benchmarking of current prototype







- Setup of hardware-in-the-loop real-time PC & FPGA monitoring/control module for squeezing lab @ LNL

- Integration of variable-gain LNA for optical AM noise compensation
- Development of a wideband balanced homodyne receiver for squeezing setup
  ↪ transimpedance input stage now under test

Under discussion: Abroad period @ Nikhef in Maastricht for prototype electronics evaluation at *ET Pathfinder* facility

Courses

Within educational offer:

- Design of readout integrated circuits for particle detectors [**2.5 CFU**]
  ↪ Exam passed: discussion on low power radhard ASIC design techniques
- Cabling and shielding for low noise applications [**1.25 CFU**] → Attended
- Microelectronics for radiation detectors II [**3 CFU**] → Exam planned
- Advanced FPGA design and management techniques [**2.5 CFU**] → Ongoing

Other specific training courses:

- Time and frequency metrology & instrumentation (prof. Rubiola - CNRS)
- Microwave Engineering 101 by Interlligent (provided by INFN Padova)

Transversal skills courses:

- Scientific Publication (prof. Rubiola - CNRS)
- Introduction to Academic English (prof. Leone/Crestani - CLA UniPD)

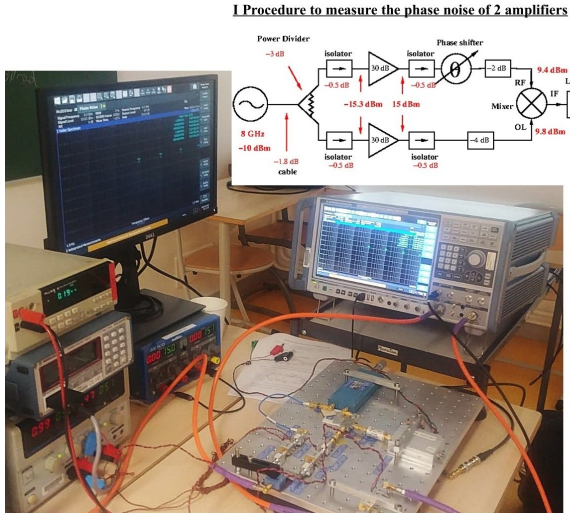
Planned courses for next year:

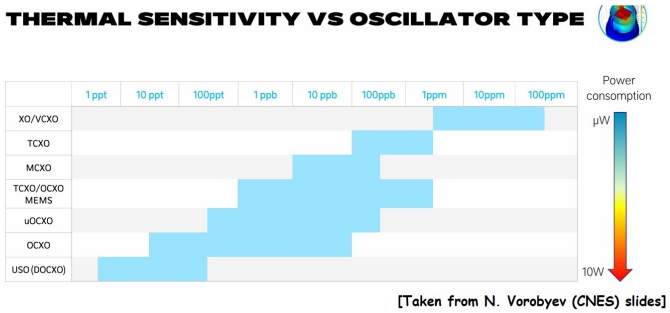
- Embedded Design with FPGA (prof. Stanco/Vogrig/Triossi)
  ↪ borrowed from PhD school in Information Engineering

Schools and workshops

Schools

- EFTS: European Time and Frequency Seminar (Jun 30 - Jul 4)



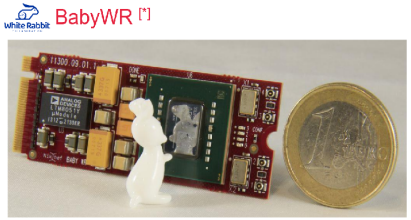


[Taken from N. Vorobyev (CNES) slides]

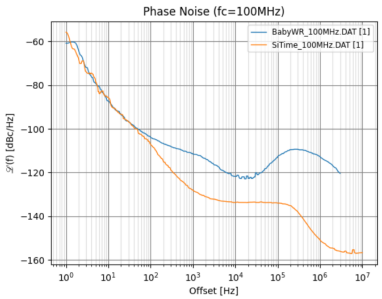
- Advanced course to FPGA programming by ICSC (Oct 27-29)

Workshops

- 14^{th} White Rabbit Workshop (Jun 25-26)



[Taken from K. Asteriou (Nikhef) slides]



WR timing signals originate form the WR reference clock in a noisy digital FPGA

- First Virgo Detector Workshop (Sep 29-30)

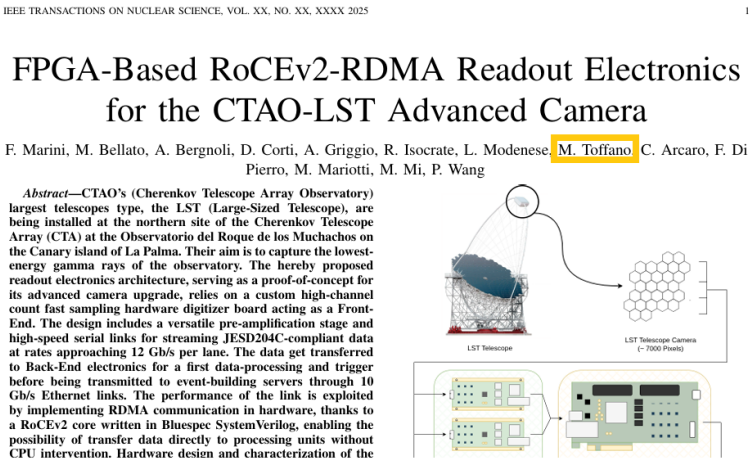
Other academic achievements

Scientific collaborations: joined VIRGO and Einsten Telescope experiments

Publication on IEEE Tra. Nuc. Sci:

Contributed to

- Simulation of the analog front-end including parasitics
- Reliability analysis
- RMS jitter characterization



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FPGA-Based RoCEv2-RDMA Readout Electronics for the CTAO-LST Advanced Camera

F. Marini, M. Bellato, A. Bergnoli, D. Corti, A. Griggio, R. Isocrate, L. Modenese, M. Toffano, C. Arcaro, F. Di Pierro, M. Mariotti, M. Mi, P. Wang

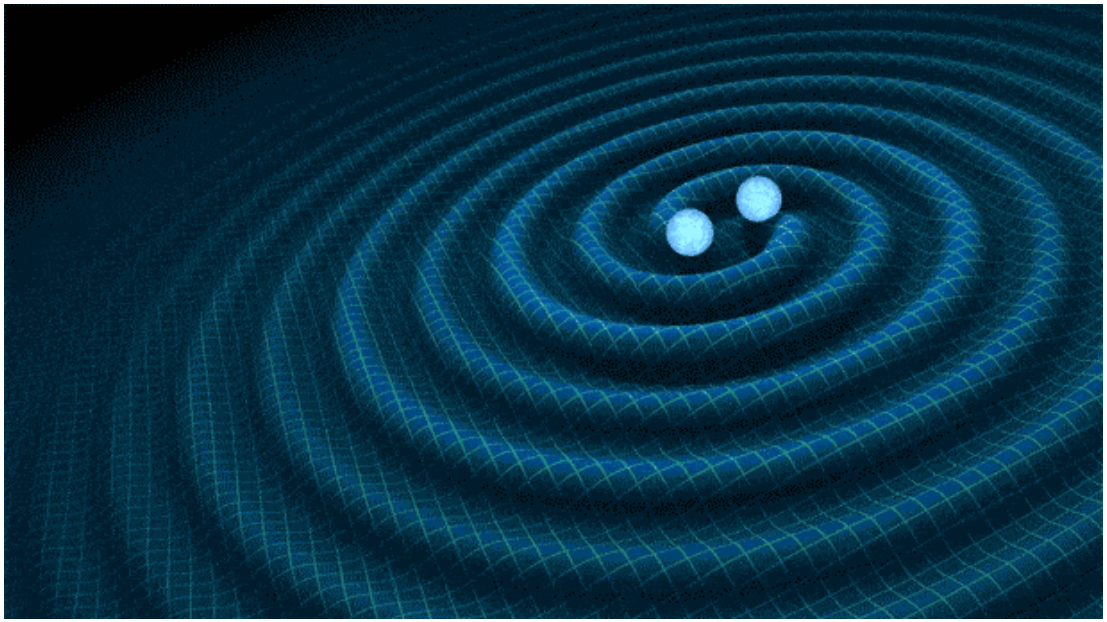
***Abstract*—CTAO's (Cherenkov Telescope Array Observatory) largest telescopes type, the LST (Large-Sized Telescope), are being installed at the northern site of the Cherenkov Telescope Array (CTA) at the Observatorio del Roque de los Muchachos on the Canary island of La Palma. Their aim is to capture the lowest-energy gamma rays of the observatory. The hereby proposed readout electronics architecture, serving as a proof-of-concept for its advanced camera upgrade, relies on a custom high-channel count fast sampling hardware digitizer board acting as a Front-End. The design includes a versatile pre-amplification stage and high-speed serial links for streaming JESD204C-compliant data at rates approaching 12 Gb/s per lane. The data get transferred to Back-End electronics for a first data-processing and trigger before being transmitted to event-building servers through 10 Gb/s Ethernet links. The performance of the link is exploited by implementing RDMA communication in hardware, thanks to a RoCEv2 core written in Bluespec SystemVerilog, enabling the possibility of transfer data directly to processing units without CPU intervention. Hardware design and characterization of the**

Planned conference contributions in the 2^{nd} year:

- 7^{th} International workshop on new photon-detectors (Dec 3-5)
  $\hookrightarrow$ abstract submitted
- Gravitational Waves and Detection Technologies – PAS Rome Meeting (Mar 16-17, 2026) $\rightarrow$ refining abstract for submission
- 25^{th} IEEE Real Time Conference (May 25-29, 2026)

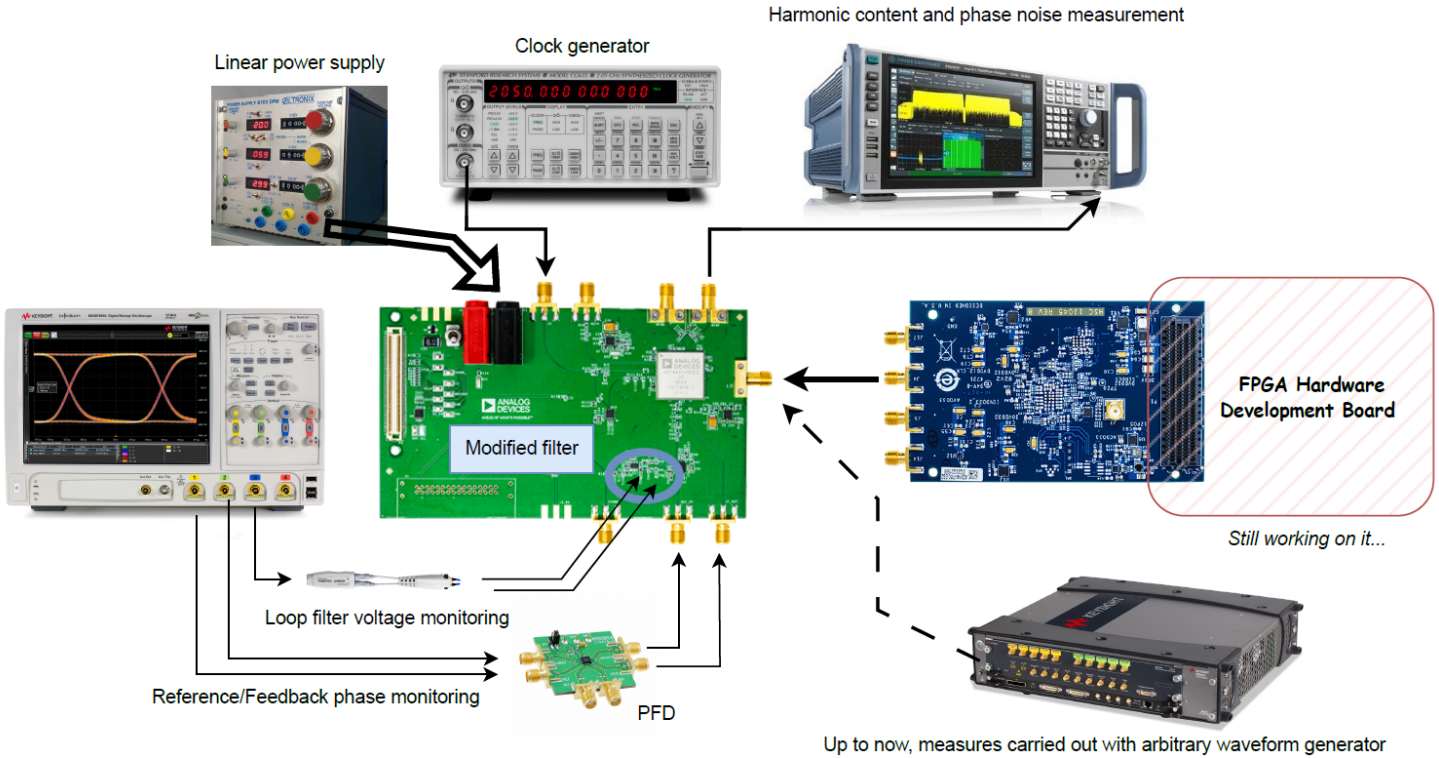
Thanks for your attention!

Any questions?



Backup slides

Test setup


Linear power supply
Clock generator
Harmonic content and phase noise measurement
Modified filter
FPGA Hardware Development Board
Still working on it...
Loop filter voltage monitoring
Reference/Feedback phase monitoring
PFD
Up to now, measures carried out with arbitrary waveform generator

All-in-fiber PN cancellation loop