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DI PADOVA

PhD course of National Interest in Technologies for
Fundamental Research in Physics and Astrophysics

Annual report

Name and surname: **Simran Yadav**

Cycle and a.a.: **40th and 2024-2025**

Supervisor: **Angelo Cotta Ramusino, Nicolò Vladi Biesuz**

- **Research activity carried out during the year**

Describe the aim of the project (very briefly), discuss the research activity carried out during the year mentioning the difficulties encountered until now and the actions taken to face them. 1 page max in total.

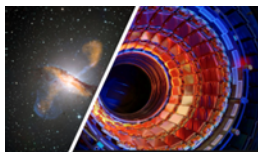
My research is part of the R&D program aimed at enhancing the performance of the Ring Imaging Cherenkov (RICH) detectors of the LHCb experiment at CERN. This upgrade is essential to ensure that the RICH detectors maintain their particle identification efficiency under the significantly higher particle rates expected following the High-Luminosity LHC (HL-LHC) upgrade, scheduled for Long Shutdown 4 (LS4), currently planned for 2034.

As an intermediate milestone, the front-end electronics of the RICH detectors will undergo a partial upgrade during Long Shutdown 3 (LS3), scheduled to begin in July 2026. This upgrade will implement a new readout chain for the Multianode Photomultiplier Tubes (MaPMTs) currently installed in the detectors. At the core of the new readout system is the "FASTRICH" ASIC—a custom chip developed at CERN to meet the demanding timing precision and high data-rate requirements of the upgraded environment. The first FASTRICH prototypes were delivered to CERN on May 7, 2025, and in August, a set was mounted onto Front-End Boards (FEBs) developed by INFN-Ferrara.

During my first year of research, I focused on understanding the features of the FASTRICH ASIC and contributing to the development of a Quality Control (QC) system for the FASTRICH-based front-end boards (FASTRICH-FEBs).

The QC system is designed around the recently developed **TEI1000-02-A3I11-A** module from Trenz Electronic GmbH, which integrates an **ALTERA 1SX040HH3F35I3VG Stratix 10 SoC FPGA** with an ARM processor. This device provides a sufficient number of high performance LVDS I/O ports and sufficient resources to control up to two FASTRICH-FEBs, corresponding to eight ASICs, each equipped with four serial links capable of operating at data rates of up to **1.28 Gbps**.

For this platform, I developed firmware modules implementing the following key functions:



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- **Locking and deserialization** of serial data transmitted via FASTRICH output links at data rates of **320, 640, or 1280 Mbps**.
- **Stripping of the AURORA 64b/66b framing protocol**, used by the FASTRICH output serial ports, to ensure robustness against synchronization losses caused by serial bit errors.
- **Decoding of FASTRICH data packets**, which encode digitized information for particle “hits”.

To support development and validation, I made extensive use of a **QuestaSim simulation framework** provided by the LHCb back-end experts which allowed me to deepen my understanding of FASTRICH operation by following the data flow originated by running the simulation scripts. I am also using QuestaSim to test the HDL modules I implemented. The next step will be real-world validation, which will become possible once the first batch of Trenz modules is delivered to INFN.

- **List of attended courses and passed exams**

1. Design of Readout Integrated circuits for particle detectors- 2,5 credits
2. Programmable System on Chip (SoC) for data acquisition and processing- 4 credits
3. Advanced scientific programming in Matlab- 6 credits
4. Electronic systems in high energy physics - 4 credits
5. Fundamental of FPGA-based digital design- 2,5 credits

- **List of attended conferences, workshops and schools, with mention of the presented talks**

1. Workshop on electronics for Physics Experiments and Applications
2. 2nd FPGA Developers’ Forum (FDF) meeting

- **List of published papers/proceedings**

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- **Thesis title (even temporary)**

TEMPORARY: “Development of a time-resolved RICH detector for the LHCb RICH upgrade program”



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Date, 11/09/2025

Signature

Seen, the Supervisors