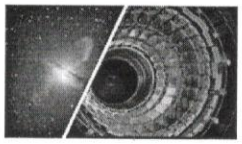


1222·2022 800 ANNI

UNIVERSITÀ DEGLI STUDI DI PADOVA

PhD course of National Interest in Technologies for Fundamental Research in Physics and Astrophysics

Annual report

Name and surname: Julisa Verdejo Palacios
Cycle and a.a.: 40th Series 2024/2025
Supervisor: Giuseppe De Robertis

• Research activity carried out during the year

The proposed research activity focuses on the development and testing of a scalable readout system for advanced particle detectors, with particular emphasis on drift wire chambers. These detectors require efficient and reliable data acquisition, achieved through the design of high-performance architectures implemented on an FPGA-based platform (MOSAIC). The work includes the development of interface circuits to ensure robust communication with the detector and the implementation of high-speed serial links for data transmission. The goal is to provide a versatile laboratory setup suitable for both detector characterization and beam test environments.

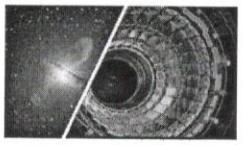
During the year, I focused on developing a serializer/deserializer in SystemVerilog for a waveform digitizer (HDSoCv1), using 8b/10b encoding to enable communication. These modules interface with the MOSAIC through the Wishbone bus for configuration and monitoring. Since the Wishbone bus and the digitizer operate at different clock frequencies, synchronization circuits were implemented to prevent clock domain crossing issues.

The main activities carried out to achieve these tasks were:

- Study of SystemVerilog by reviewing its syntax and core concepts, practicing coding exercises, creating testbenches, and exploring different FSM implementation styles.
- Learned to use Synopsys simulation tools to validate the designed modules.
- Reviewed and developed an 8b/10b encoder/decoder in C++ to verify the correct operation of the serializer/deserializer (SerDes).
- Studied Clock Domain Crossing (CDC) principles to handle modules operating at different frequencies.

During the development process, several challenges have been encountered:

- Limited documentation on the waveform digitizer: One of the main difficulties was the lack of detailed information regarding the digitizer's functionality. To address this, I reviewed the device's schematic and researched the specification of its internal components, which allowed me to better understand its behavior and operational characteristics.
- Designing the serializer and deserializer: Another significant challenge was the design of the serializer and deserializer modules, as they must continuously send and receive data to and from the waveform digitizer. To overcome this, I studied the 8b/10b encoding scheme, developed a C++ implementation to verify the correctness of the design, and performed simulations to ensure reliable data transmission.



1222·2022 800 ANNI

UNIVERSITÀ DEGLI STUDI DI PADOVA

PhD course of National Interest in Technologies for
Fundamental Research in Physics and Astrophysics

- **List of attended courses and passed exams**

1.	Design of readout integrated circuits for particle detectors	Passed – 2.5 CFUs
2.	Programmable System on Chip (SoC) for data acquisition and processing	Passed – 2.5 CFUs
3.	Fundamentals of FPGA-based digital design	Passed – 2.5 CFUs
4.	Cabling and shielding for low noise applications	Exam left

- **List of attended conferences, workshops and schools, with mention of the presented talks**
  1. INFN Bari – Synopsys, Language: SystemVerilog Testbench
  2. INFN Bari – La moderna programazione in C++
  3. Duolos - Using AMD High Level Synthesis to Supercharge your Design Performance
  4. Duolos – Clock Domain Crossing
- **List of published papers/proceedings**
- **Thesis title (even temporary)**

Development and test of the readout system of advanced particle detectors.

Date, 10/09/2025 **Signature:**

Seen, the supervisor