UNIVERSITÀ
DEGLI STUDI
DI PADOVA

Admission to the 2nd year

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General Information

- **Name and surname:** Julisa Verdejo Palacios
- **Cycle and A.Y:** 40th Series, 2024/2025
- **Curriculum:** Electronics
- **Tutor:** Giuseppe De Robertis
- **Research Center:** INFN Bari
- **Topic:** Development and test of the readout system of advanced particle detectors.

Agenda

- Courses and training activities
- Research topic and objectives
- Research activities carried out so far (1st year)
- Plan for 2nd and 3rd years

Courses and training activities

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Courses	Credits	Professor	Hours	Year
Design of readout integrated circuits for particle detectors	2.5	Flavio Loddo	20	1st
Programmable System on Chip (SoC) for data acquisition and processing	2.5	Andrea Fabbri	20	1st
Fundamentals of FPGA-based digital design	2.5	Cristian Zambelli Nicolò Vladi Biesuz	20	1st
Cabling and shielding for low noise applications	1.25	Alberto Aloisio	10	1st
Advanced FPGA design and design management techniques	2.5	Nicolò Vladi Biesuz Enrico Calore	20	2nd

Training activities	Place	Year
Synopsys, Language: System Verilog Testbench	Online	1st
Doulos: Using AMD High Level Synthesis to Supercharge your Design Performance	Online	1st
Doulos: Clock Domain Crossing	Online	1st
La moderna programazione in C++	Online	1st

Research topic and objectives

Research topic and objectives

The proposed research activity focuses on the development and testing of a scalable readout system for advanced particle detectors, with particular emphasis on drift wire chambers. These detectors require efficient and reliable data acquisition, achieved through the design of high-performance architectures implemented on an FPGA-based platform (MOSAIC).

The work includes the development of interface circuits to ensure robust communication with the detector and the implementation of high-speed serial links for data transmission. The goal is to provide a versatile laboratory setup suitable for both detector characterization and beam test environments.

System Overview: MOSAIC and HDSoCv1

MOSAIC – Modular System for Acquisition, Interface and Control

Core FPGA: Xilinx XC7A200T-2 FFG1156C

- 215,360 Logic Cells
- 730 Block RAMs (12.8 Mb)
- 10 I/O Banks, 10 Clock Tiles
- 500 User I/O
- 16 Low-Power GTs (up to 6.6 Gbps)

Firmware Architecture

- Modular design: supports high-speed data acquisition and control
- Data Collector: Transfers data from receivers to DDR3 at 5 GB/s
- Wishbone Bus: Used for configuration and monitoring
- IP Bus Transactor: Translates UDP/IP commands into Wishbone transactions
- Hardware-specific blocks for detectors & control interfaces

Embedded CPU

- 8-bit CISC microprocessor @ 50 MHz
- 12 KB Program Memory, 2 KB RAM
- Implements TCP/IP & UDP/IP stacks, diagnostics, firmware updates, and board management

High-Speed Networking

- Gigabit Ethernet interface (10/100/1000 Mbps)
- Hardware DMA engine for low CPU load (30% @ 120 MB/s)
- Supports direct PC connection, auto-configuration

HDSoCv1

Waveform Digitizer HDSoC v1 Features

- Sampling Rate: 1 GSa/s
- 32 channels
- 2k Sample Buffer
- > 600MHz Analog Bandwidth
- < 100 ps Timing Resolution
- Internally configurable triggering schemes
- **Serial interface that requires a pair of LVDS lines**
- **Encoding data with 8b10b**
- Communication based on short packets, with maximum 5 words

Research activities carried out so far (1st year)

Knowledge & Tools Improvement

Technical Skills Acquired

- SystemVerilog
  - Syntax and core concepts
  - **Testbench (very important)**
- Design of FSM with datapath
- Synopsys Tools
- C++
- Clock Domain Crossing (CDC)
  - Synchronization techniques
- Vivado Tooling

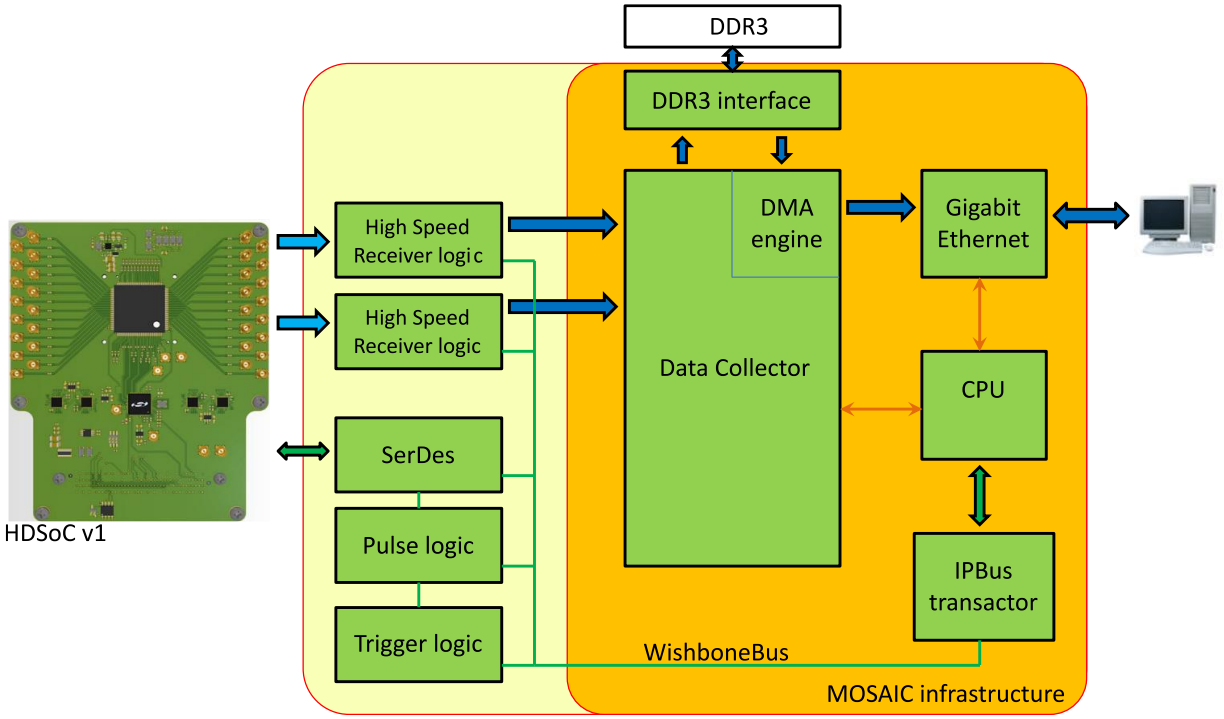
SYNOPSYS®

First-Year PhD Activities

Development of a **serializer/deserializer in SystemVerilog** for the HdSoCv1, using 8b10b encoding to enable communication with MOSAIC.

Key Achievements:

1. Designed, implemented and simulated SerDes modules with 8b10b encoding.
2. Developed an 8b10b encoder/decoder in C++ to verify the correct operation of the SerDes.
3. Integrated communication with MOSAIC via the Wishbone bus for configuration and monitoring.
4. Implemented synchronization circuits to manage clock domain crossing between the Wishbone bus and the digitizer.



Plan for 2nd and 3rd years

Plan for 2nd and 3rd years

- **2nd Year**
  - Integrate firmware blocks into MOSAIC and validate internal communication.
  - Development of C++ firmware to enable interaction between the MOSAIC platform and the SerDes modules.
  - Perform full system test with real HDSoC v1 board.
  - Implement data readback and on-FPGA processing using High-Level Synthesis (HLS) to extract and analyze key detector parameters.
- **3rd Year**
  - Continue developing FPGA-based modules on the MOSAIC platform to ensure reliable detector communication and enable efficient data readout using High-Level Synthesis (HLS).
  - Write the thesis
  - Prepare for thesis defense

Thank you for your attention

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