PhD course of National Interest in Technologies for Fundamental Research in Physics and Astrophysics

Annual report

Name and surname: Fatima Bzeih
Cycle and a.a.: 39th Cycle
Supervisor: Prof. Paolo Musico

- **Research activity carried out during the year**

The PhD project aims to design and characterize a new Ethernet-based data acquisition (DAQ) board for high-energy physics experiments. The objective is to replace the legacy VME readout system with a modern 1G/10G Ethernet architecture, enabling higher throughput, easier integration with computing infrastructures, and greater flexibility for distributed detector systems. The system is designed for use with Gas Electron Multiplier (GEM) detectors equipped with APV25 front-end chips, and it will contribute to future experiments at Jefferson Lab (JLab), including the MOLLER experiment. MOLLER (Measurement of a Lepton-Lepton Electroweak Reaction) is a flagship experiment that will make the most precise measurement of the weak charge of the electron through polarized electron–electron scattering. Its extremely high luminosity and large detector systems demand state-of-the-art DAQ electronics capable of handling very high data rates with reliability, making this project directly relevant.
During the second year, the research progressed in several directions:

- **Validation of the 1G Ethernet system**
  Prototype boards were delivered and fully tested. The 1G firmware was successfully implemented on the FPGA, with the board recognized on the network and responding to TCP/IP communication (ping). Tests on the Genoa laboratory bench demonstrated stable operation with a throughput of ~30 MB/s, while tests at JLab confirmed correct integration with real GEM detectors, marking the first validation of the system in an experimental environment. Although not yet tested with real detector data, the streaming interface achieved a maximum throughput of 100 MB/s using synthetic data generated internally on the FPGA.
- **Advancement towards 10G Ethernet implementation**
  Development of the 10G firmware was initiated. TCP connectivity was demonstrated at the simulation level, showing scalability to higher bandwidth. To verify hardware readiness, IBERT (Integrated Bit Error Ratio Test) scans confirmed that the board's high-speed transceivers support reliable 10G operation. Work is ongoing to integrate and optimize the 10G stack to reach stable performance.
- **Experimental activities and international mobility**
  A two-week stay at JLab in June 2025 was dedicated to testing the board with GEM

detectors. Subsequently, a 65-day period abroad began at JLab, involving direct participation in the installation of the MOLLER experiment.

- **Difficulties encountered** included limited throughput in the first 1G implementation (~30 MB/s vs. higher expected rates), debugging of communication issues, and the complexity of scaling to 10G. These challenges were addressed by firmware refinement, modular design, extensive simulation, and systematic testing at both Genoa and JLab.

In conclusion, the second year consolidated the 1G Ethernet system with detector validation, demonstrated the feasibility of 10G Ethernet operation, and ensured integration of the work into a major physics experiment (MOLLER). The third year will focus on finalizing the 10G firmware, performing large-scale detector validation, contributing to MOLLER's commissioning, and preparing the doctoral thesis and journal publications.

- **List of attended courses and passed exams**

Course Title	Credit	Status
Machine Learning programming in physics	2.5	Passed
Gaseous detector for experimental particle physics	2.5	Passed
Design of readout integrated circuits for particle detectors	2.5	Passed
Advanced FPGA design and design management techniques	2.5	Finishes before the end of September 2025

- **List of attended conferences, workshops and schools, with mention of the presented talks**
  - **PhD Retreat – LNGS (Gran Sasso National Laboratories), February 2025**
    Poster presentation on Design and Characterization of a DAQ Board for High-Energy Physics with 1G/10G Ethernet Connectivity.
  - **NEWCAS 2025 – Paris, June 2025**
    Poster presented in the Young Professional Session based on the abstract submission.
  - **PRIME 2025 – Taormina, September 2025 (upcoming)**
    Accepted paper on Real-Time Histogramming Module for a Multichannel ADC Board (oral presentation scheduled).

- **ICECS 2025 – Morocco, November 2025 (upcoming)**
  Accepted paper on Modular 1 Gbps Hardware TCP/IP FPGA Readout for MPGD Applications with APV25 (oral presentation scheduled).
- **Journal paper** on the **1G Ethernet system**, the target venues are like **IEEE Transactions on Nuclear Science (TNS)** or **Nuclear Instruments and Methods in Physics Research (NIM).**

- **List of published papers/proceedings**

  The research outcomes have been actively disseminated through multiple international conferences:

  - NEWCAS 2025 (Paris, June): Poster presented in the Young Professional Session. "Hardware-TCP Ethernet Readout Architecture for Real-Time DAQ in APV25-Based GEM Detectors".
  - PRIME 2025 (Taormina, September): Accepted paper on the Histogramming module. "Real-Time Histogramming Module for a Multichannel ADC Board".
  - ICECS 2025 (Morocco, November): Accepted paper on modular 1G TCP/IP FPGA readout for GEM detectors. "Modular 1 Gbps Hardware TCP/IP FPGA Readout for MPGD Applications with APV25".

- **Thesis title (even temporary)**

  "Design and Characterization of a Data Acquisition Board for High Energy Physics Experiment with a 1G/10G Copper/Optical Ethernet connection"

Date, 28/08/2025 **Signature** F.B

Seen, the supervisor