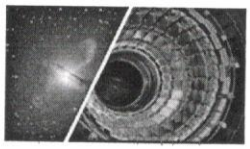


1222·2022 800 ANNI

UNIVERSITÀ DEGLI STUDI DI PADOVA

PhD course of National Interest in Technologies for Fundamental Research in Physics and Astrophysics

Annual report

Name and surname: Ciro Fabian Bermudez Marquez
Cycle and a.a.: 39th Series 2023/2024
Supervisor: Flavio Loddo

• Research activity carried out during the year

The research focuses on the development of a SystemVerilog UVM-based verification framework to validate the correctness of pixel readout chip designs to be used in future projects in the field of High Energy Physics (HEP). To this end, the work aims to develop a modular and reusable verification environment specifically for pixel chip architectures, supported by a comprehensive set of resources such as register models and verification IPs to streamline the verification process. Furthermore, it seeks to enhance simulation efficiency and coverage, enabling faster design validation cycles, while ensuring that the developed components can be readily reused across future ASIC projects within HEP collaborations.

In collaboration with the IGNITE project, which aims at developing readout and processing solutions for high-intensity 4D tracking, this year I developed the following building blocks, structured as Git repositories and hosted on Baltig:

1. UVC Code Generator: A Python-based tool that follows UVM coding guidelines from Doulos and Verification Academy to automate the generation of UVC components, significantly reducing development time.

2. RAL Code Generator: A Python-based UVM register abstraction layer generator that uses the SystemRDL language to automate the modeling of registers for the device under test.

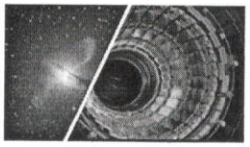
3. Hits UVC: A verification component that emulates particle hits to stimulate the device under test. It can also read files produced by physics simulations and includes a C++ extension to accelerate simulation times.

4. Matt protocol UVC: A component that models the registers inside the ASIC under verification and generates the READ/WRITE signals required to communicate with the device.

5. Readout UVC: A component responsible for dynamically generating readout signals based on the chip's output.

By combining these components, I developed a UVM verification framework to validate the core element of the IGNITE chip, called the *mattonella*. Due to its fractal architecture, this component is the most critical one to verify first. Furthermore, the verification of the complete chip is in progress, this is accomplished by modifying the base UVM framework with the new DUT and slightly tweaking the environment.

The primary challenge this year was to develop each building block independently and then integrate them into a single project. Because of the modular nature of UVM, verification activities require managing multiple small projects simultaneously, an approach that is time-consuming and challenging for a small team. The implementation of coverage and the development of a verification plan were also challenging due to the lack of experience and know-how.



1222·2022 800 ANNI

UNIVERSITÀ DEGLI STUDI DI PADOVA

PhD course of National Interest in Technologies for Fundamental Research in Physics and Astrophysics

- **List of attended courses and passed exams**

1. Design of readout integrated circuits for particle detectors
2. Programmable System on Chip (SoC) for data acquisition and processing
3. Electronic systems in high energy physics
4. Cabling and shielding for low noise applications
5. Introduction to FPGA programming using Xilinx Vivado and VHDL

- **List of attended conferences, workshops and schools, with mention of the presented talks**

1. Technical meeting IGNITE (Cagliari) March 2025 (2025/03/11)
2. General meeting IGNITE (Cagliari) April 2025 (2025/04/07)
3. Verification meeting IGNITE (Milano) June 2025 (2025/06/18)
4. Teamwork meeting for verification modeling (Cagliari) July 2025 (2025/07/14)
5. Oral presentation TWEPP 2025 (Creta) October 2025 (2025/10/06)

- **List of published papers/proceedings**

- **Thesis title (even temporary)**

Verification of read-out ASIC in 28 nm CMOS technology for next generation pixel detectors

Date, 05/09/2025 **Signature:**

Seen, the supervisor