



UNIVERSITÀ DEGLI STUDI DI PADOVA

# Admission to the 3rd year

**Ciro Fabian Bermudez Marquez**

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16 September 2025

# General Information

- **Name and surname:** Ciro Fabian Bermudez Marquez
- **Cycle and A.Y:** 39th Series, 2023/2024
- **Curriculum:** Electronics
- **Tutor:** Flavio Loddo
- **Research Center:** INFN Bari
- **Topic:** Verification of read-out electronics in 28 nm CMOS technology for next generation pixel detector

# Agenda

- Courses and training activities
- Research topic and objectives
- Verification of ASIC designs for HEP applications
- Verification Methodology
- Research activities carried out so far
- Plan for the 3rd year

# Courses and training activities

# Courses and training activities

| Courses | Credits | Professor | Year |
|---|---|---|---|
| Design of readout integrated circuits for particle detectors | 2.5 | Flavio Loddo | 2nd |
| Programmable System on Chip (SoC) for data acquisition and processing | 2.5 | Domizia Orestano | 2nd |
| Electronic systems in high energy physics | 4.0- | Adriano Lai | 2nd |
| Cabling and shielding for low noise applications | 1.0 | Alberto Aloisio | 2nd |
| Introduction to FPGA programming using Xilinx Vivado and VHDL | 2.0 | Luca Pacher | 2nd |

| Training activities | Dates | Place | Year |
|---|---|---|---|
| Verification with UVM for HEP Workshop | (27/02/2024 – 01/03/2024) | CERN | 1st |
| Training Framework PixESL for simulation of pixel chip | (07/04/2024 – 12/04/2024) | CERN | 1st |
| Cadence, System Verilog for design and verification | (07/02/2024 – 07/04/2024) | Online | 1st |
| Synopsys, Language: System Verilog Testbench | (06/02/2024 – 06/04/2024) | Online | 1st |
| Synopsys, Language: System Verilog Verification using UVM | (12/04/2024 – 12/06/2024) | Online | 1st |

# Missions and conferences

| Missions | Date |
|---|---|
| Meeting IGNITE (Bologna) April 2024 | 2024/04/15 |
| Collaboration IGNITE (Cagliari) July 2024 | 2024/07/09 |
| Technical meeting IGNITE (Cagliari) March 2025 | 2025/03/11 |
| General meeting IGNITE (Cagliari) April 2025 | 2025/04/07 |
| Verification meeting IGNITE (Milano) June 2025 | 2025/06/18 |
| Teamwork meeting for verification modeling (Cagliari) July 2025 | 2025/07/14 |
| Oral presentation TWEPP 2025 (Creta)  October 2025 | 2025/10/06 |

# Research topic and objectives

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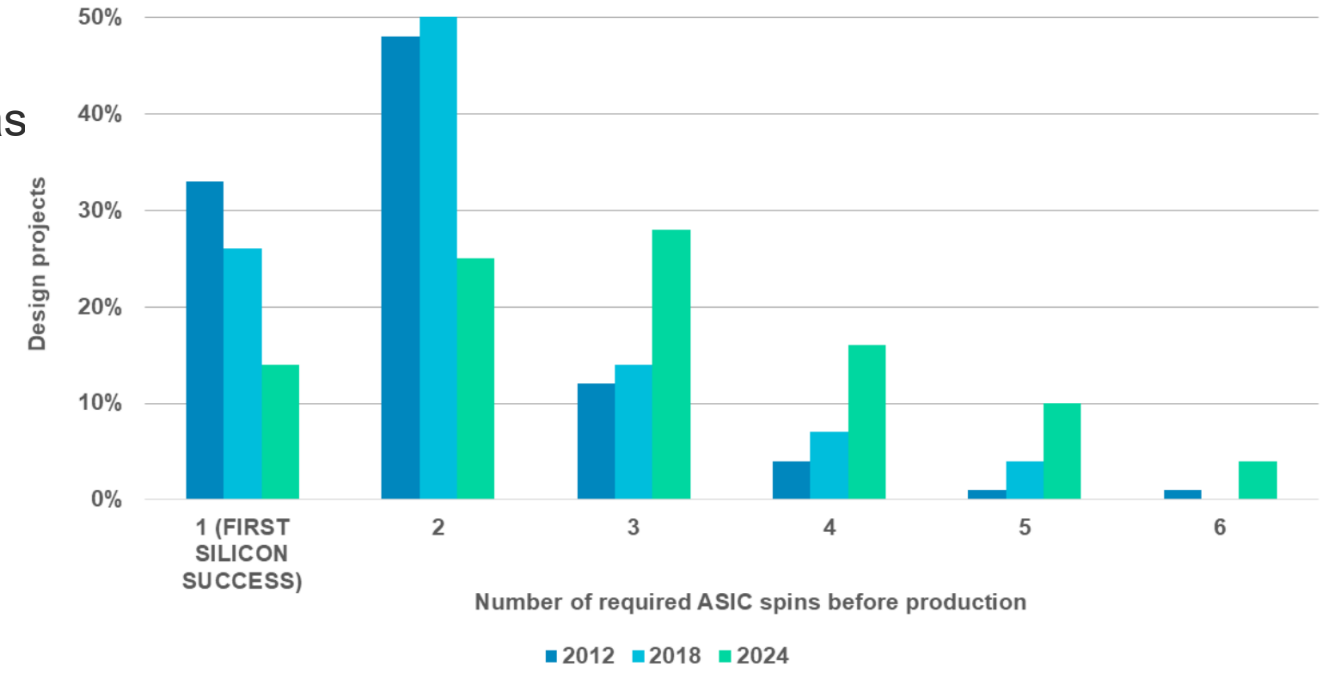
**The research focuses on the development of a SystemVerilog UVM-based verification framework to validate the correctness of pixel readout chip designs to be used in future projects in the field of High Energy Physics (HEP).**

- Develop a modular and reusable verification environment designed for pixel chip architectures.
- Provide a comprehensive set of resources (register models, verification IPs) to streamline the verification process.
- Enhance simulation efficiency and coverage, enabling faster design validation cycles.
- Facilitate reuse of components across future ASIC projects in HEP collaborations.


# Verification of ASIC designs for HEP applications

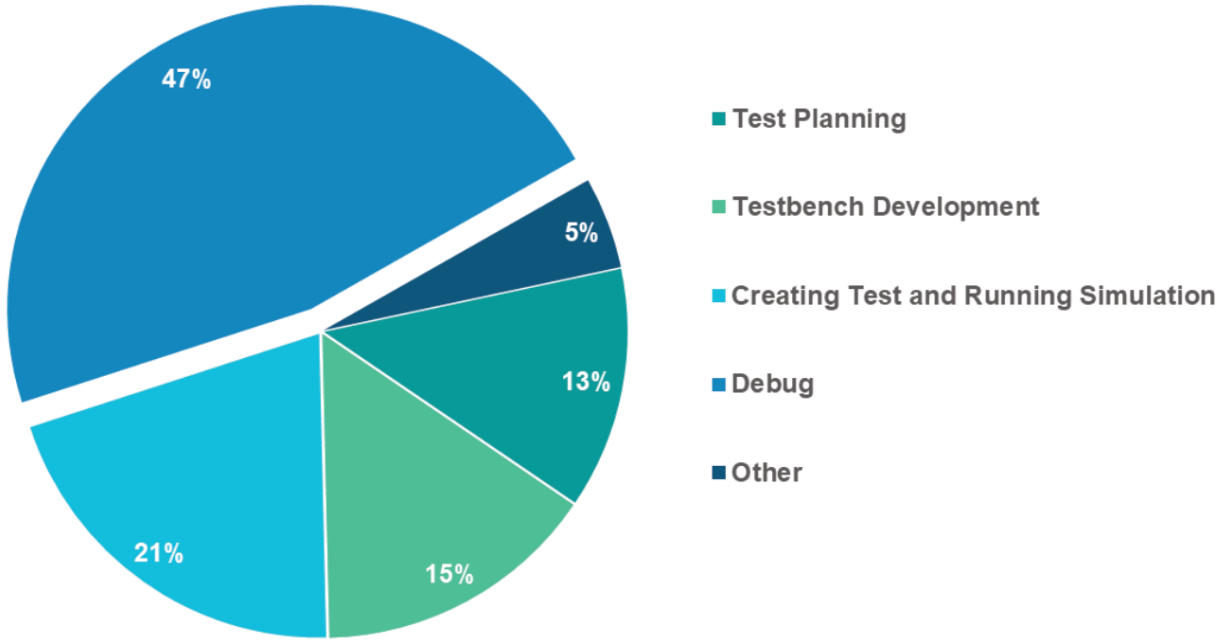
# What is verification?

- **Design activity to prone correctness**
  - Verification is a resource limited quest to find as many bugs as possible before shipping.
- **Hard problem**
  - How to prove absence of bugs?
- **Bottleneck**
  - ASIC verification is more complex and time consuming than design
  - Verification is resource intensive

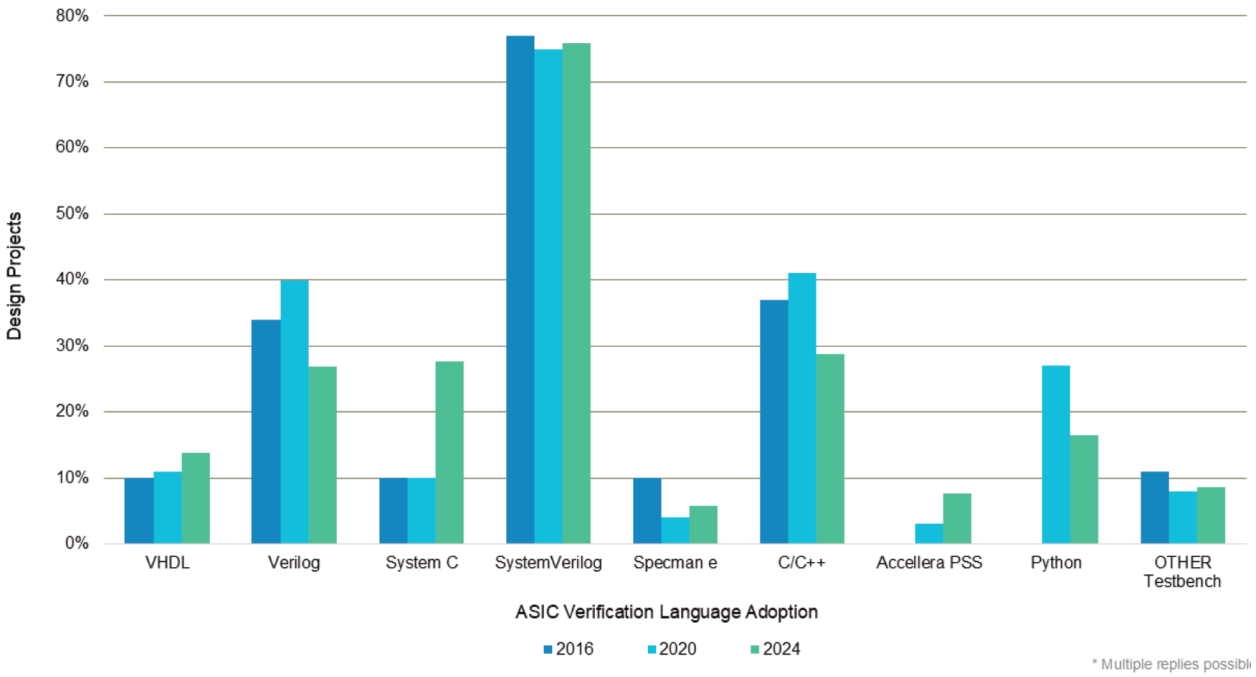


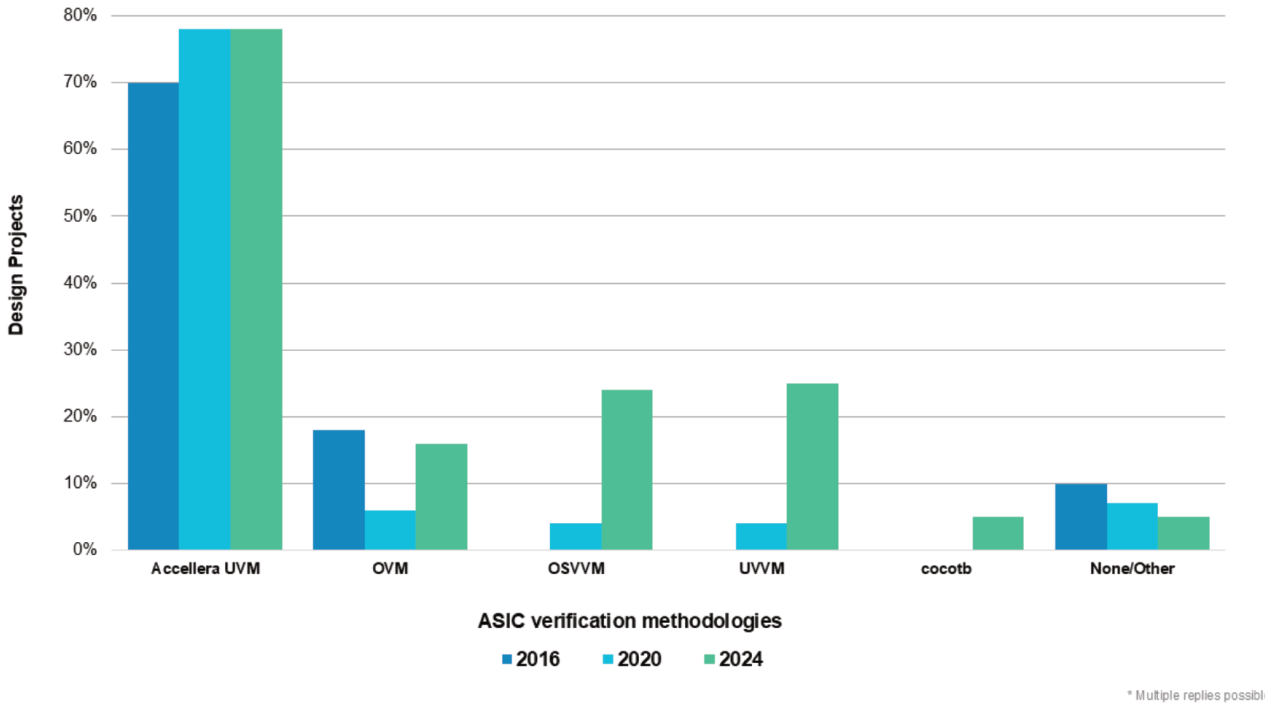
# Verification for HEP ASICs

- **Extreme Radiation Tolerance**
  - Fault injection campaigns
  - Single Event Transient
  - TID (Total Ionizing Dose) aware designs
- **High data-rate**
  - High-Luminosity Large Hadron Collider (HL-LHC), hit rate of 3.5 GHz/cm2
  - Trigger-based architectures (RD53)
  - Data-driven architectures (Velopix, IGNITE)



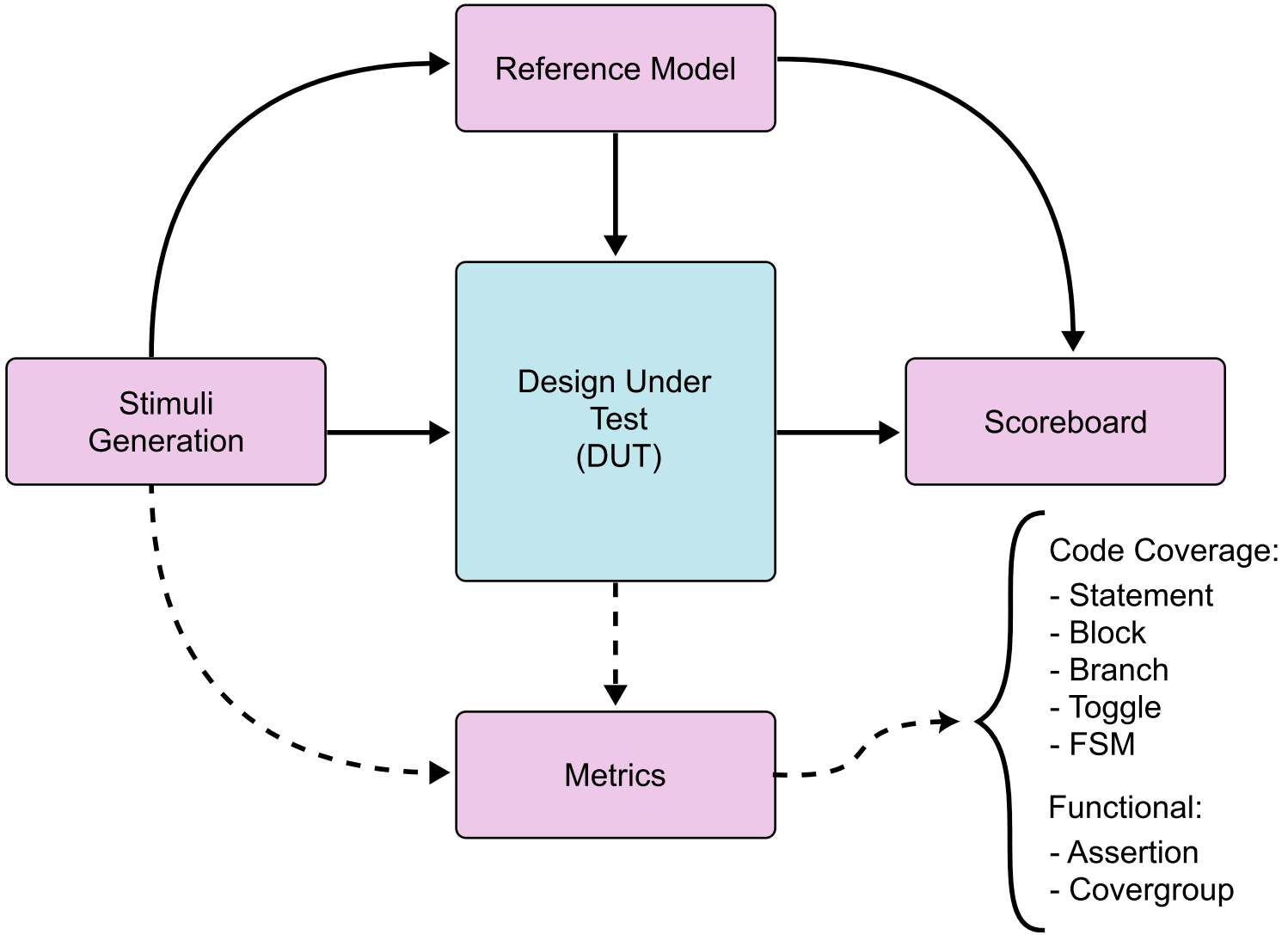
# Verification language adoption & methodology



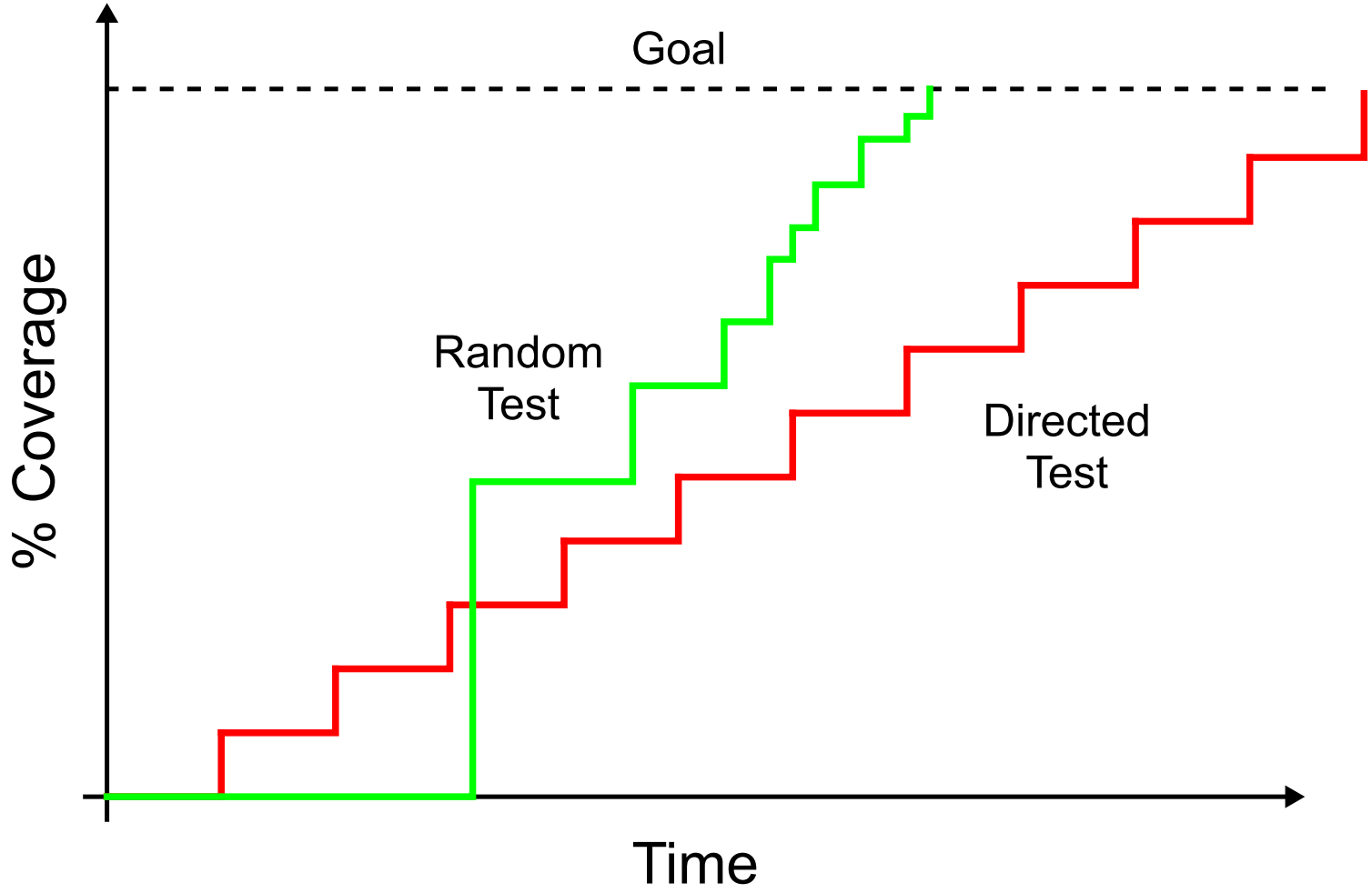



# Verification Methodology

# Anatomy of a Verification Environment



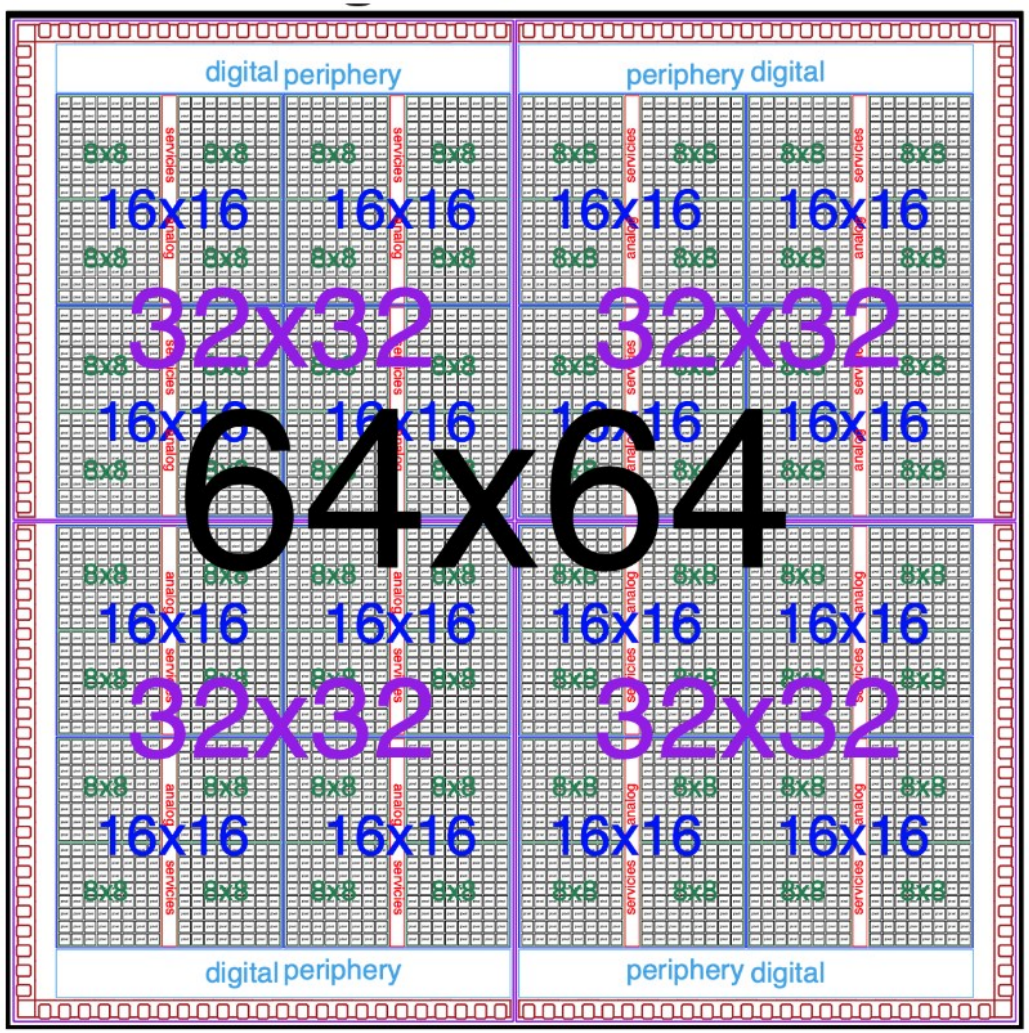
# Constrained-random test progress over time vs directed testing



# Research activities carried out so far (2nd year)

# IGNITE ASIC

- **The IGNITE project aims at developing read-out and processing solutions for high intensity 4D-tracking**
  - Concurrent high time less than 50 ps and space resolution of 10 μm
  - Power density as low as possible around 1 W $cm^{-2}$
  - Operate at large fluences (> 1x $10^{16}$ 1 MeV neutron per $cm^2$)
  - High total ionizing dose (TID > 1 Grad)
  - 28 nm CMOS technology



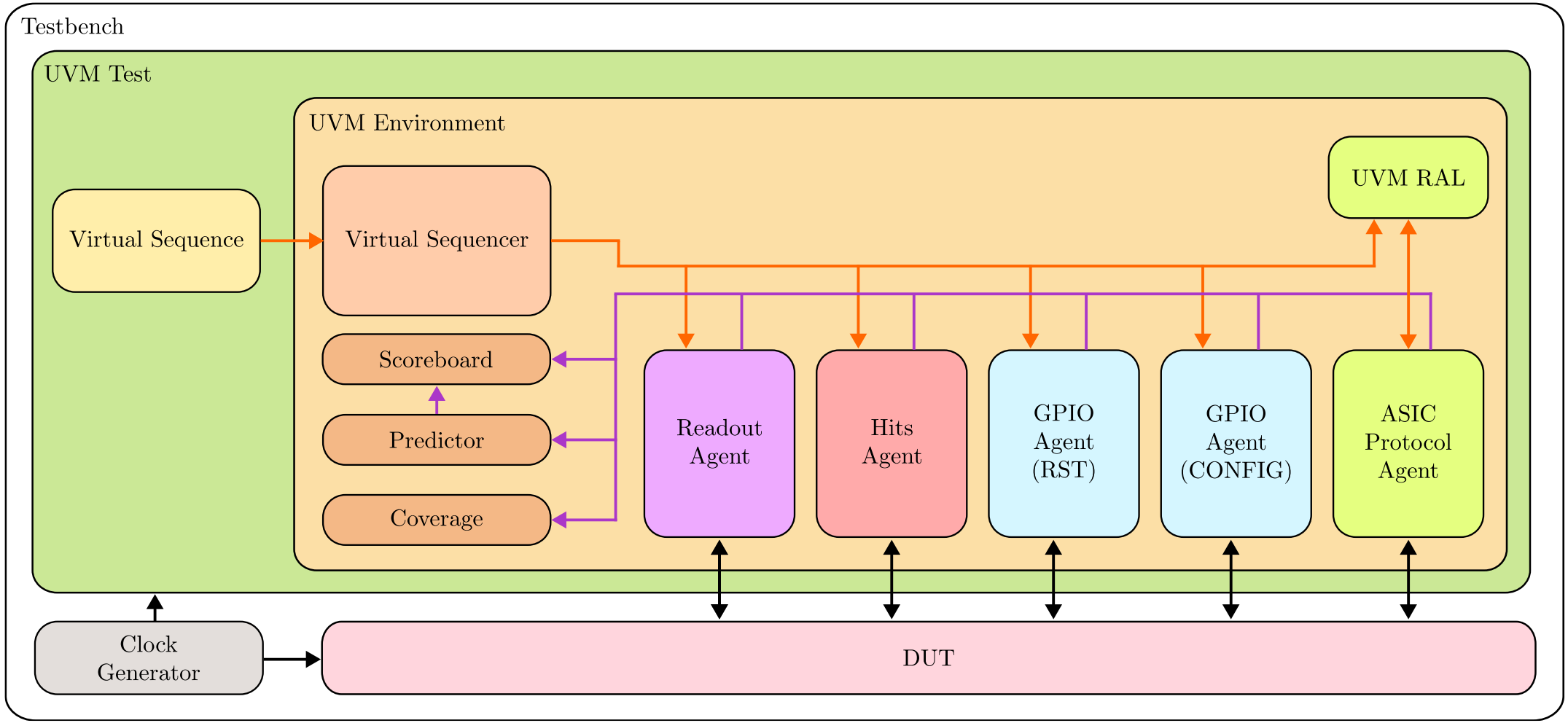
# Activities carried out

- **Development of Verification Utility Tools and Scripts to facilitate workflow.**
  - GitHub pyuvcgen
  - GitHub pyralgen
- **Development of general purpose UVM Verification IPs (VIP) to be use in different projects (baltig.infn.it)**
  - GPIO UVC
  - Clock Generator UVC
  - Hits UVC
  - Matt protocol UVC/RAL (SV/C++)
  - Readout UVC

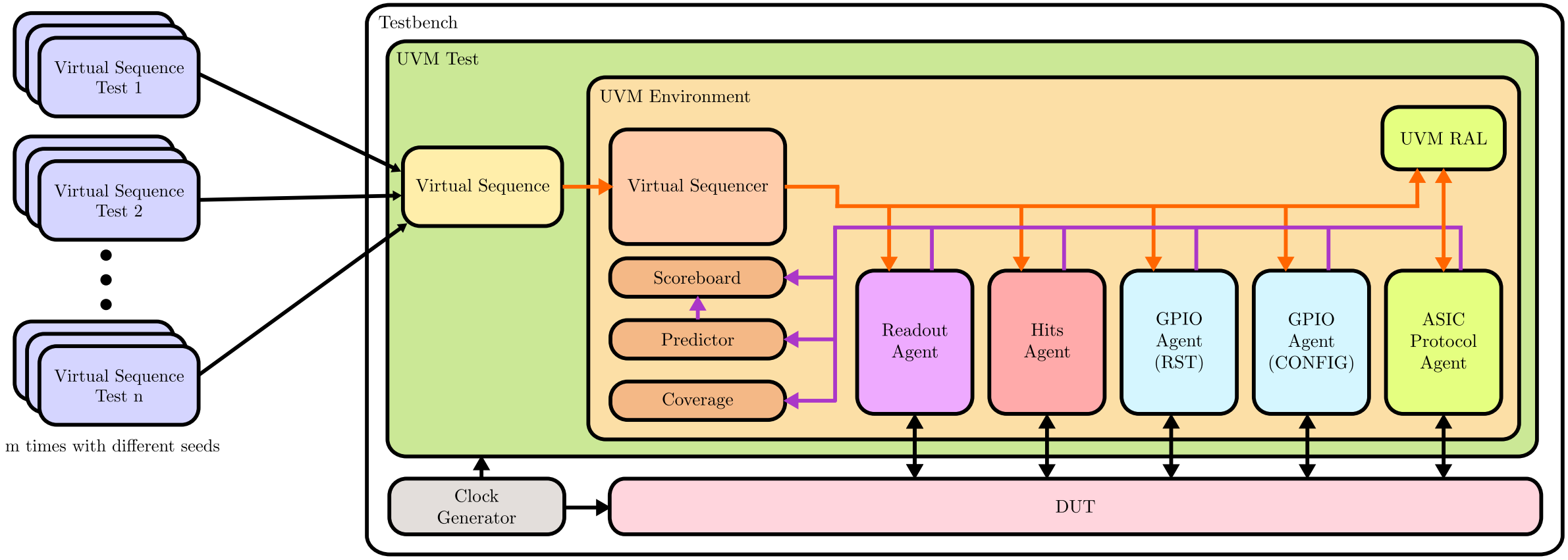




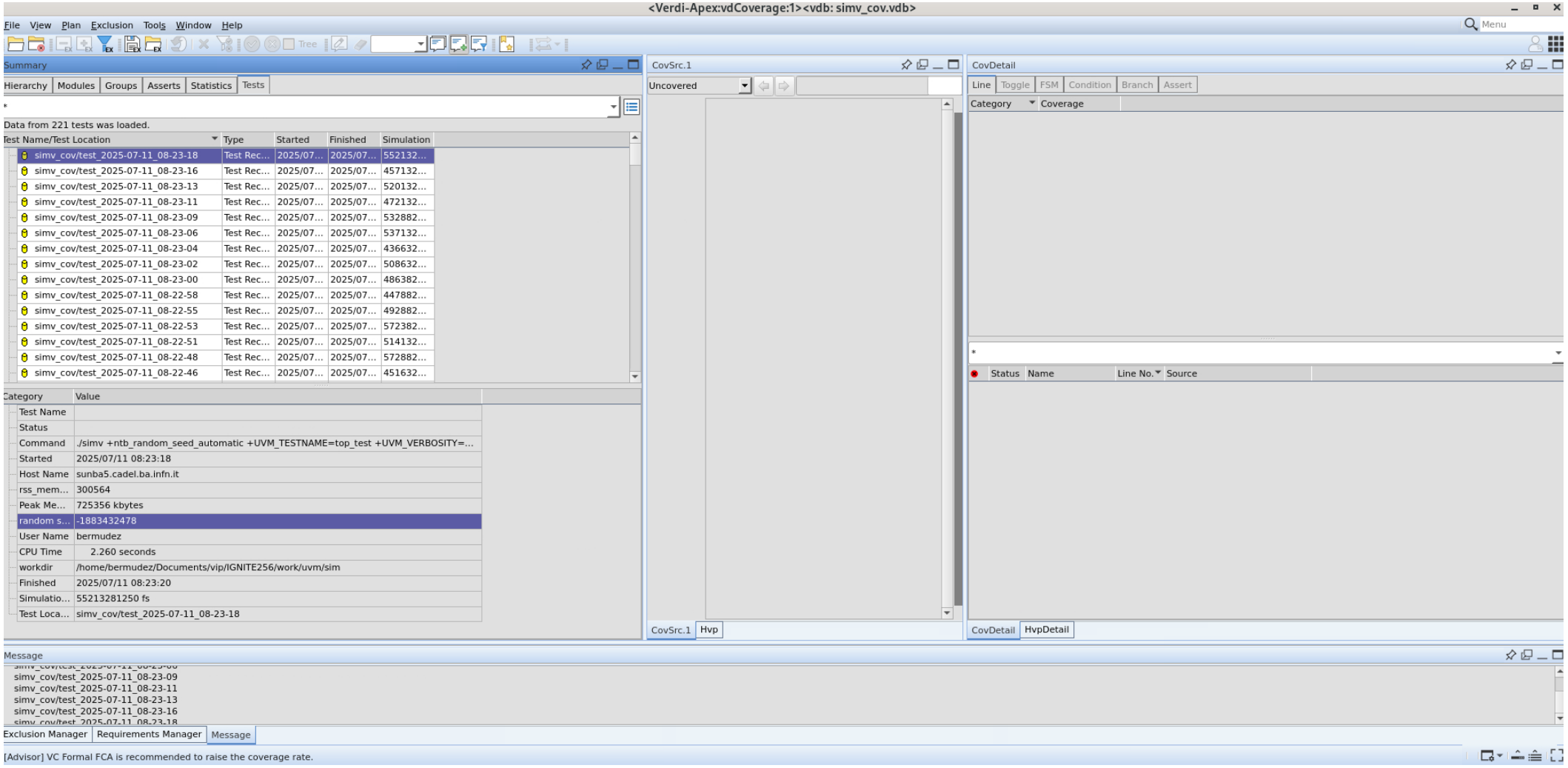

# IGNITE264 ASIC Verification Framework (1)



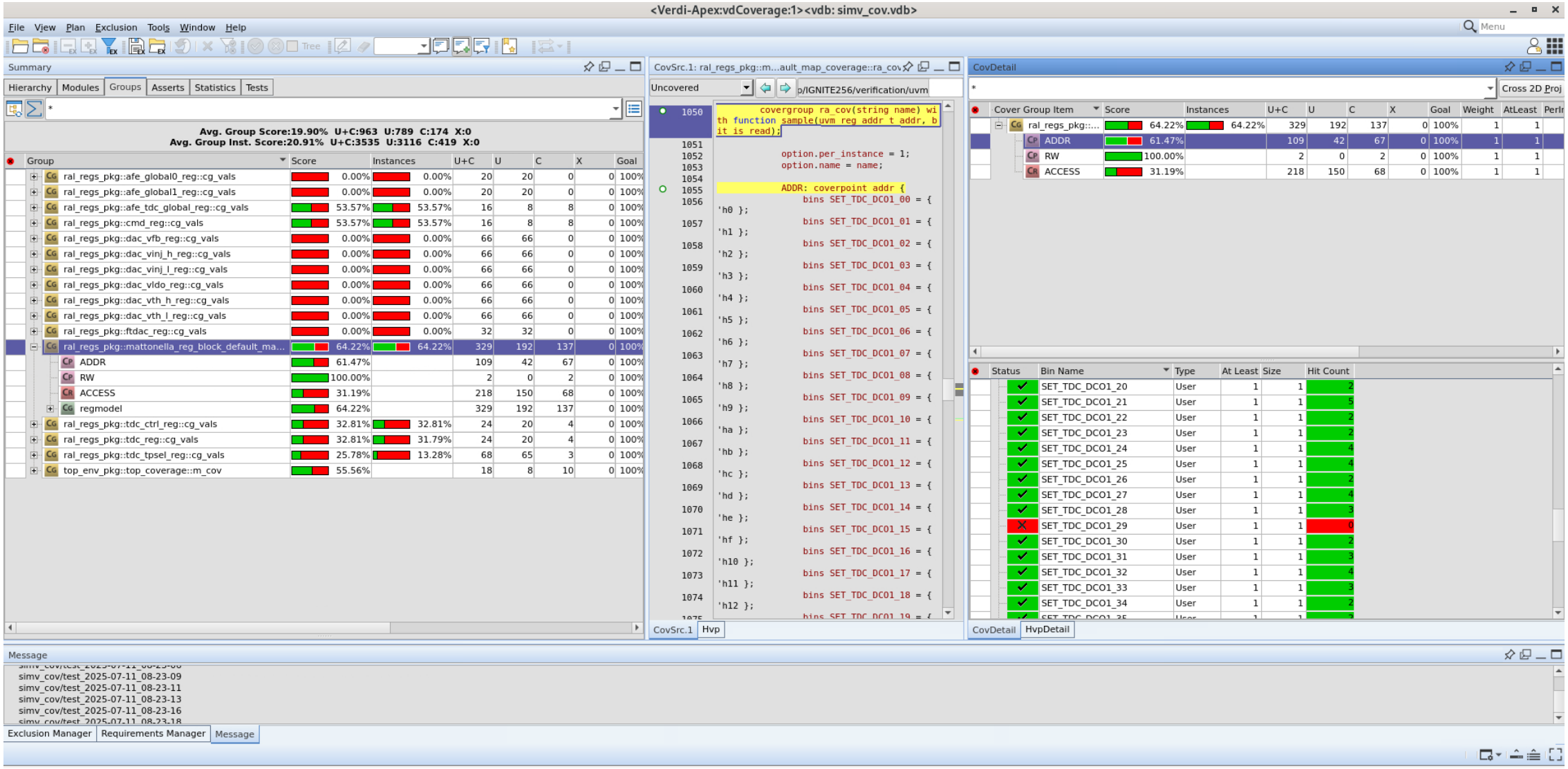
# IGNITE264 ASIC Verification Framework (2)



# Regression campaigns



# Register coverage



# Results

- **Modular & (GPIO, Hits, Readout, Matt Protocol)**
  - Readout UVC: behaves as a full readout system emulator
  - C++ acceleration in Hits UVC for faster simulations
- **Register Modeling: UVM RAL API integrated with auto-generated RAL models**
- **Automation: Makefile-driven regression suite with scalable test campaigns**
- **Coverage-Driven Verification:**
  - Registers (RAL model)
  - Pixel behavior
  - GPIO interfaces
- **Reusability & Portability: Designed for future ASIC projects across HEP collaborations**

# Plan for the 3rd year

# Plan for the 3rd year

- **3rd Year**
  - Continue working in the development of the verification framework and use it to verify the IGNITE chip
  - Optimize the verification environment according to the project goals.
  - Write the thesis
  - Prepare for thesis defense

# Thank you for your attention



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# Backup slides


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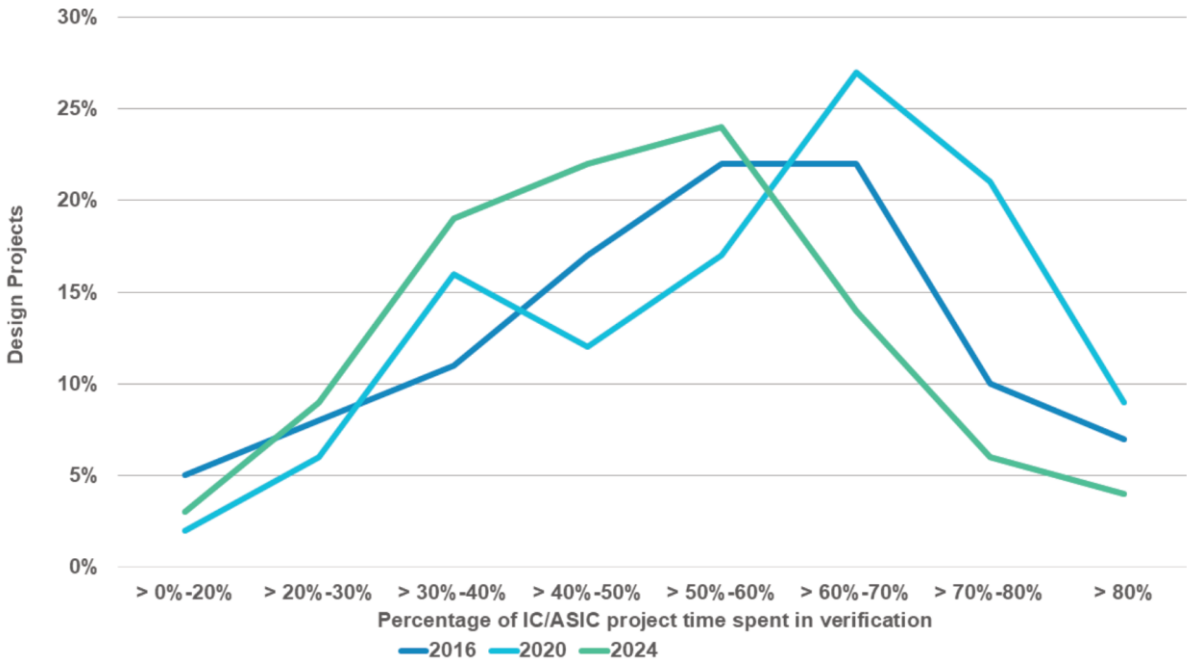
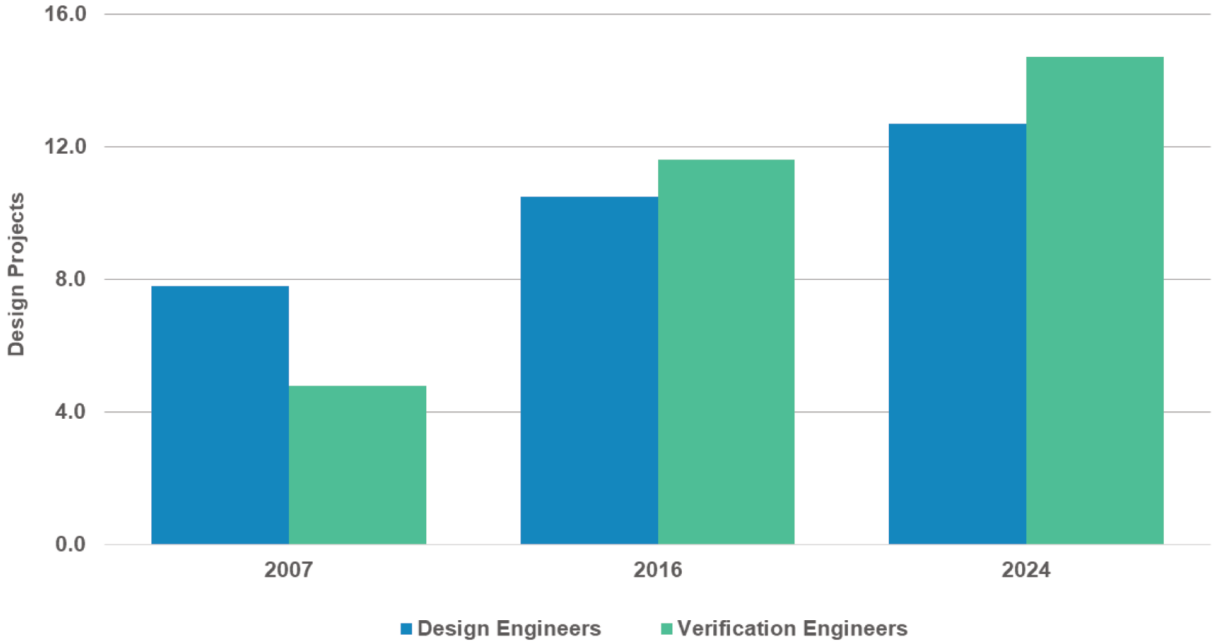
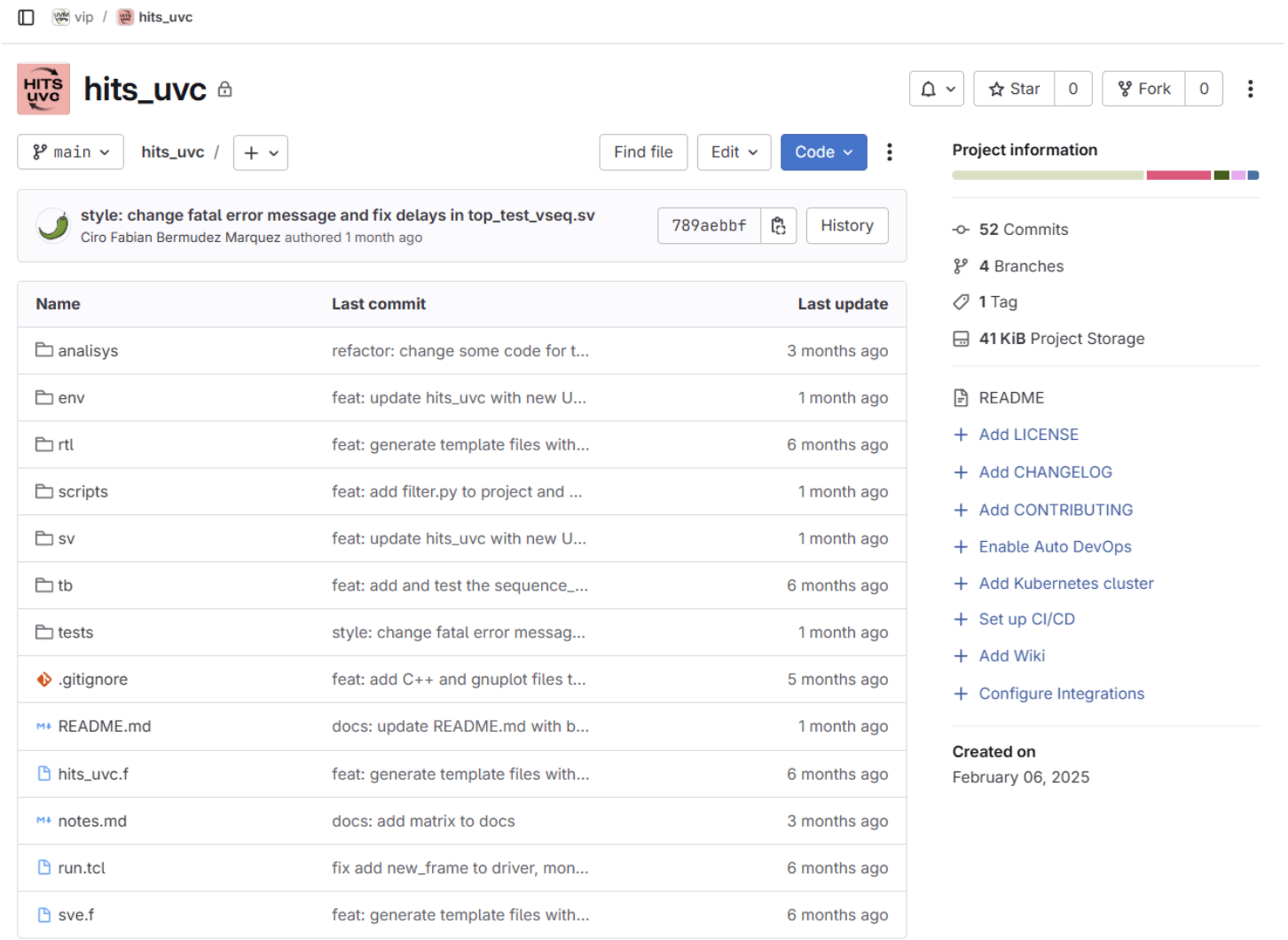
# Project time spent in verification & mean peak number of engineers



# Example


vip / hits_uvc
hits_uvc
Star 0
Fork 0
main
hits_uvc /
Find file
Edit
Code
style: change fatal error message and fix delays in top_test_vseq.sv
Ciro Fabian Bermudez Marquez authored 1 month ago
789aebbf
History
Name
Last commit
Last update
analisys
refactor: change some code for t...
3 months ago
env
feat: update hits_uvc with new U...
1 month ago
rtl
feat: generate template files with...
6 months ago
scripts
feat: add filter.py to project and ...
1 month ago
sv
feat: update hits_uvc with new U...
1 month ago
tb
feat: add and test the sequence_...
6 months ago
tests
style: change fatal error messag...
1 month ago
.gitignore
feat: add C++ and gnuplot files t...
5 months ago
README.md
docs: update README.md with b...
1 month ago
hits_uvc.f
feat: generate template files with...
6 months ago
notes.md
docs: add matrix to docs
3 months ago
run.tcl
fix add new_frame to driver, mon...
6 months ago
sve.f
feat: generate template files with...
6 months ago
Project information
52 Commits
4 Branches
1 Tag
41 KiB Project Storage
README
Add LICENSE
Add CHANGELOG
Add CONTRIBUTING
Enable Auto DevOps
Add Kubernetes cluster
Set up CI/CD
Add Wiki
Configure Integrations
Created on
February 06, 2025

# Simulation technique trends