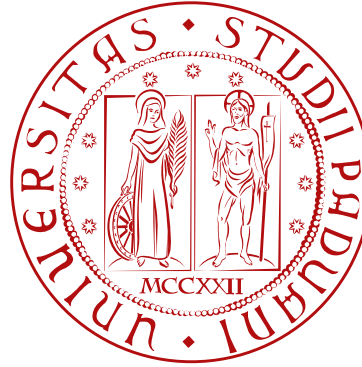




UNIVERSITÀ
DEGLI STUDI
DI PADOVA

Admission to the 3rd year

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16 September 2025

General Information

- **Name and surname:** Ciro Fabian Bermudez Marquez
- **Cycle and A.Y:** 39th Series, 2023/2024
- **Curriculum:** Electronics
- **Tutor:** Flavio Loddo
- **Research Center:** INFN Bari
- **Topic:** Verification of read-out electronics in 28 nm CMOS technology for next generation pixel detector

Agenda

- **Courses and training activities**
- **Research topic and objectives**
- **Verification of ASIC designs for HEP applications**
- **Verification Methodology**
- **Research activities carried out so far**
- **Plan for the 3rd year**

Courses and training activities

Courses and training activities

Courses	Credits	Professor	Year
Design of readout integrated circuits for particle detectors	2.5	Flavio Loddo	2 nd
Programmable System on Chip (SoC) for data acquisition and processing	2.5	Domizia Orestano	2 nd
Electronic systems in high energy physics	4.0-	Adriano Lai	2 nd
Cabling and shielding for low noise applications	1.0	Alberto Aloisio	2 nd
Introduction to FPGA programming using Xilinx Vivado and VHDL	2.0	Luca Pacher	2 nd

Training activities	Dates	Place	Year
Verification with UVM for HEP Workshop	(27/02/2024 – 01/03/2024)	CERN	1 st
Training Framework PixESL for simulation of pixel chip	(07/04/2024 – 12/04/2024)	CERN	1 st
Cadence, System Verilog for design and verification	(07/02/2024 – 07/04/2024)	Online	1 st
Synopsys, Language: System Verilog Testbench	(06/02/2024 – 06/04/2024)	Online	1 st
Synopsys, Language: System Verilog Verification using UVM	(12/04/2024 – 12/06/2024)	Online	1 st

Missions and conferences

Missions	Date
Meeting IGNITE (Bologna) April 2024	2024/04/15
Collaboration IGNITE (Cagliari) July 2024	2024/07/09
Technical meeting IGNITE (Cagliari) March 2025	2025/03/11
General meeting IGNITE (Cagliari) April 2025	2025/04/07
Verification meeting IGNITE (Milano) June 2025	2025/06/18
Teamwork meeting for verification modeling (Cagliari) July 2025	2025/07/14
Oral presentation TWEPP 2025 (Creta) October 2025	2025/10/06

Research topic and objectives

Research topic and objectives

The research focuses on the development of a SystemVerilog UVM-based verification framework to validate the correctness of pixel readout chip designs to be used in future projects in the field of High Energy Physics (HEP).

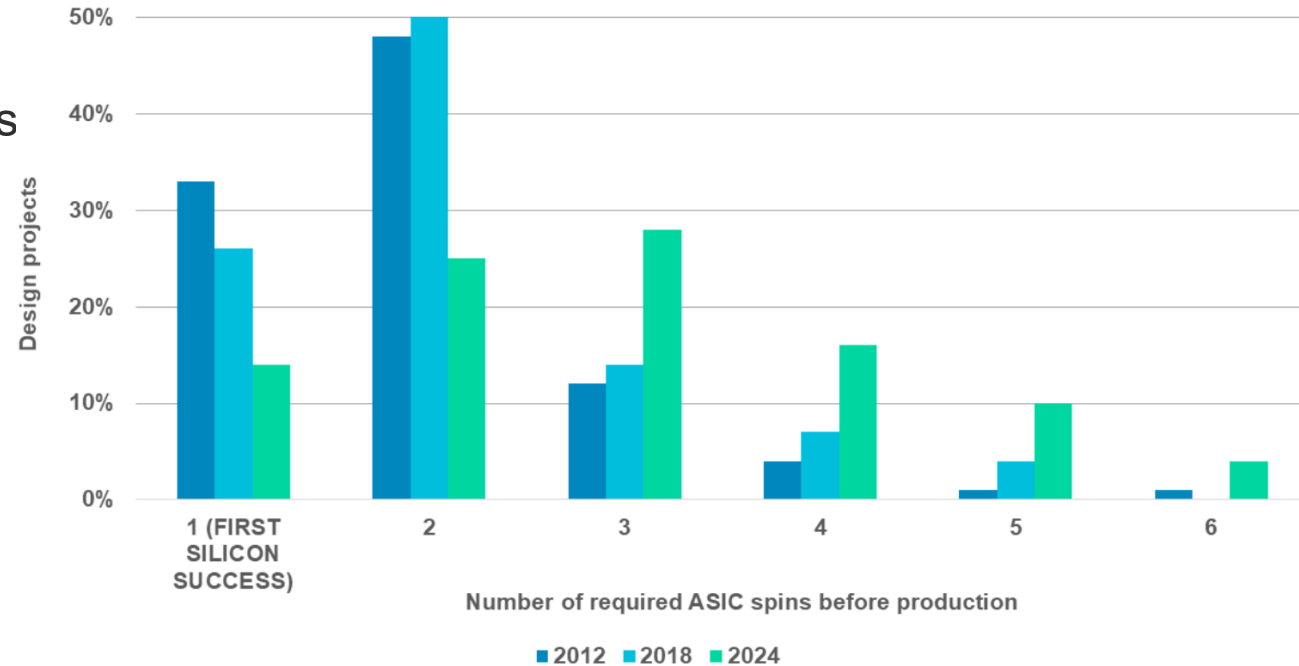
- Develop a modular and reusable verification environment designed for pixel chip architectures.
- Provide a comprehensive set of resources (register models, verification IPs) to streamline the verification process.
- Enhance simulation efficiency and coverage, enabling faster design validation cycles.
- Facilitate reuse of components across future ASIC projects in HEP collaborations.



Verification of ASIC designs for HEP applications

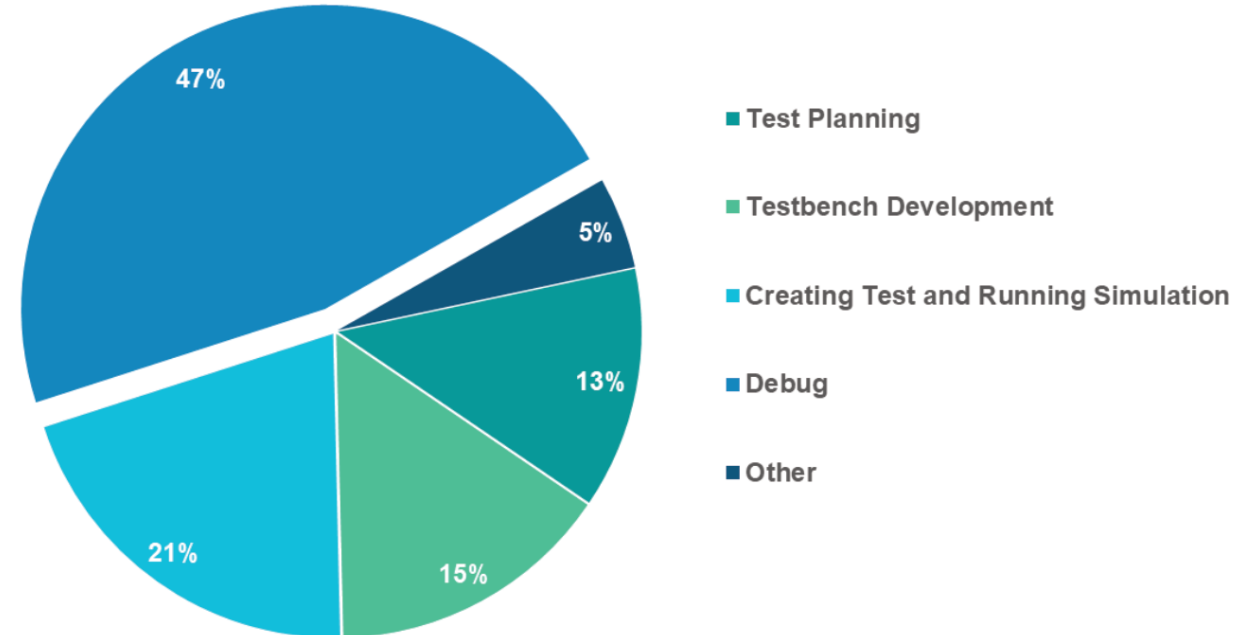
What is verification?

- **Design activity to prone correctness**
 - Verification is a resource limited quest to find as many bugs as possible before shipping.
- **Hard problem**
 - How to prove absence of bugs?
- **Bottleneck**
 - ASIC verification is more complex and time consuming than design
 - Verification is resource intensive

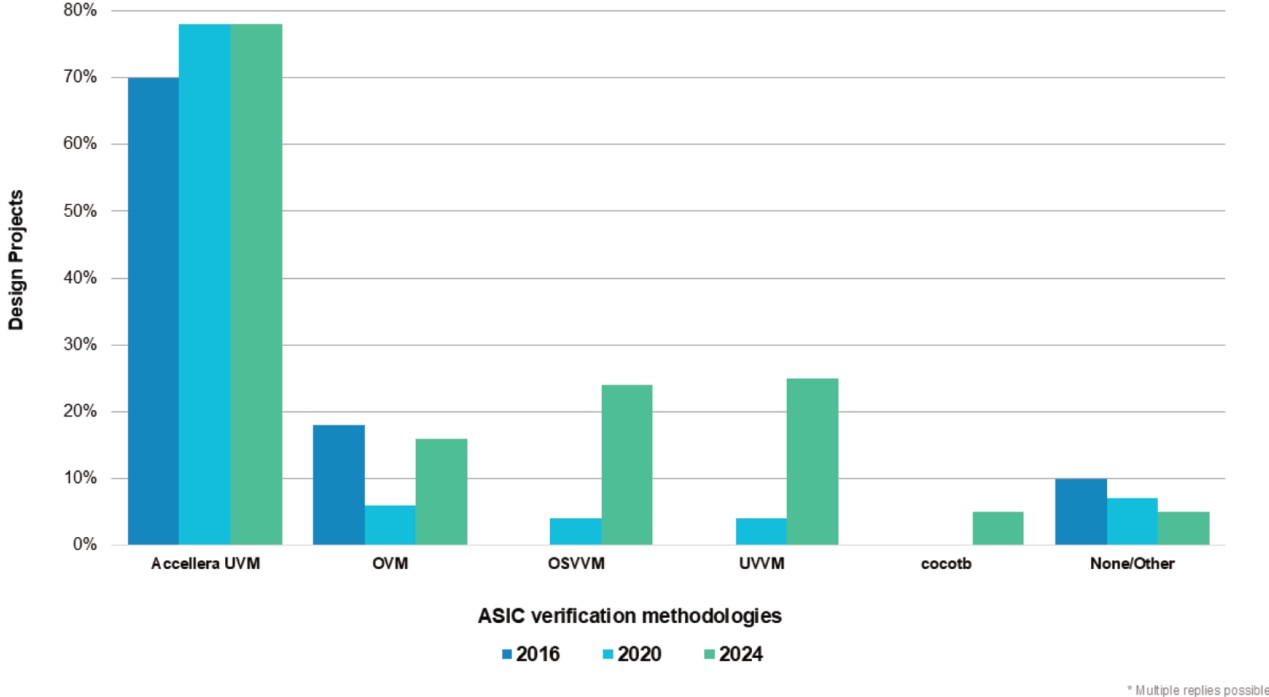
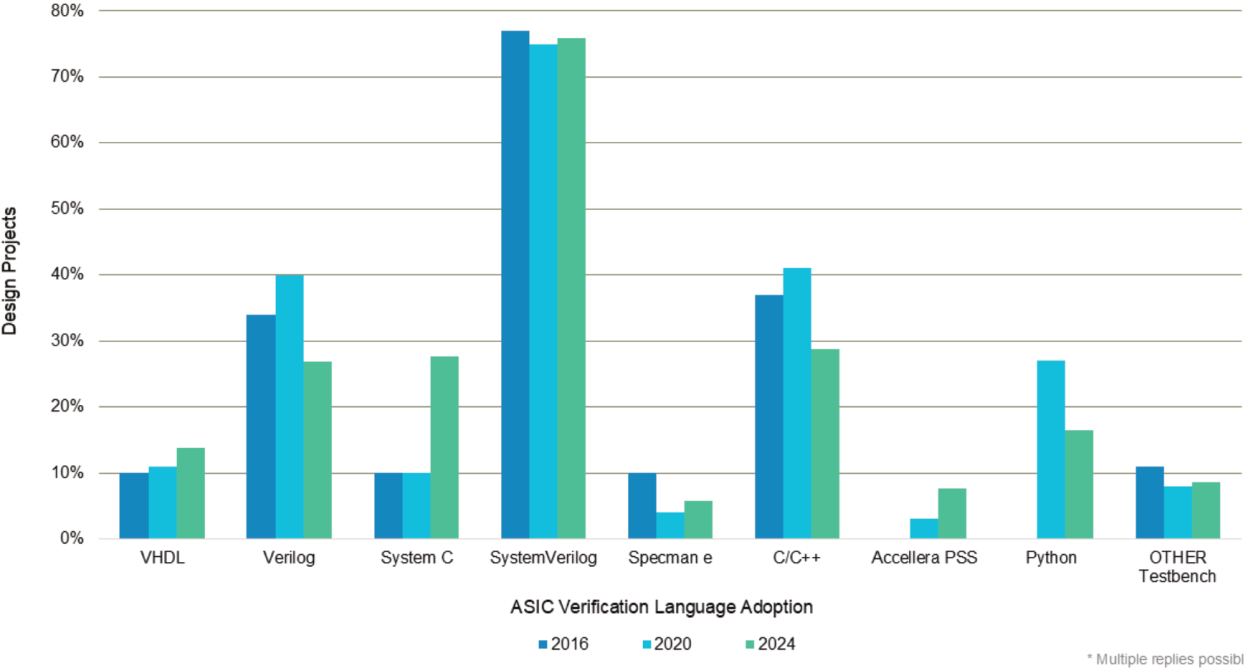


Verification for HEP ASICs

- **Extreme Radiation Tolerance**
 - Fault injection campaigns
 - Single Event Transient
 - TID (Total Ionizing Dose) aware designs
- **High data-rate**
 - High-Luminosity Large Hadron Collider (HL-LHC), hit rate of 3.5 GHz/cm²
 - Trigger-based architectures (RD53)
 - Data-driven architectures (Velopix, IGNITE)

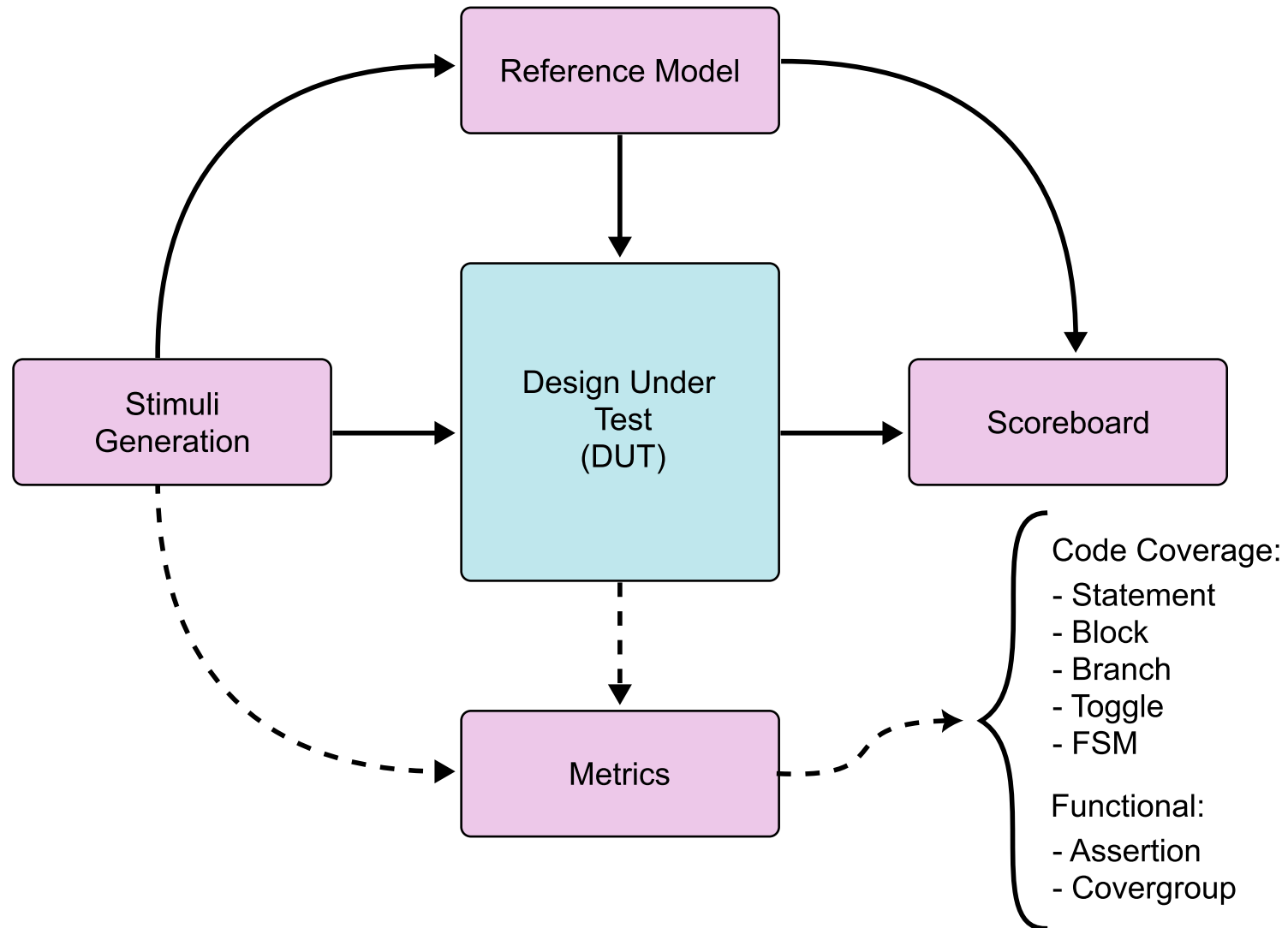


Verification language adoption & methodology

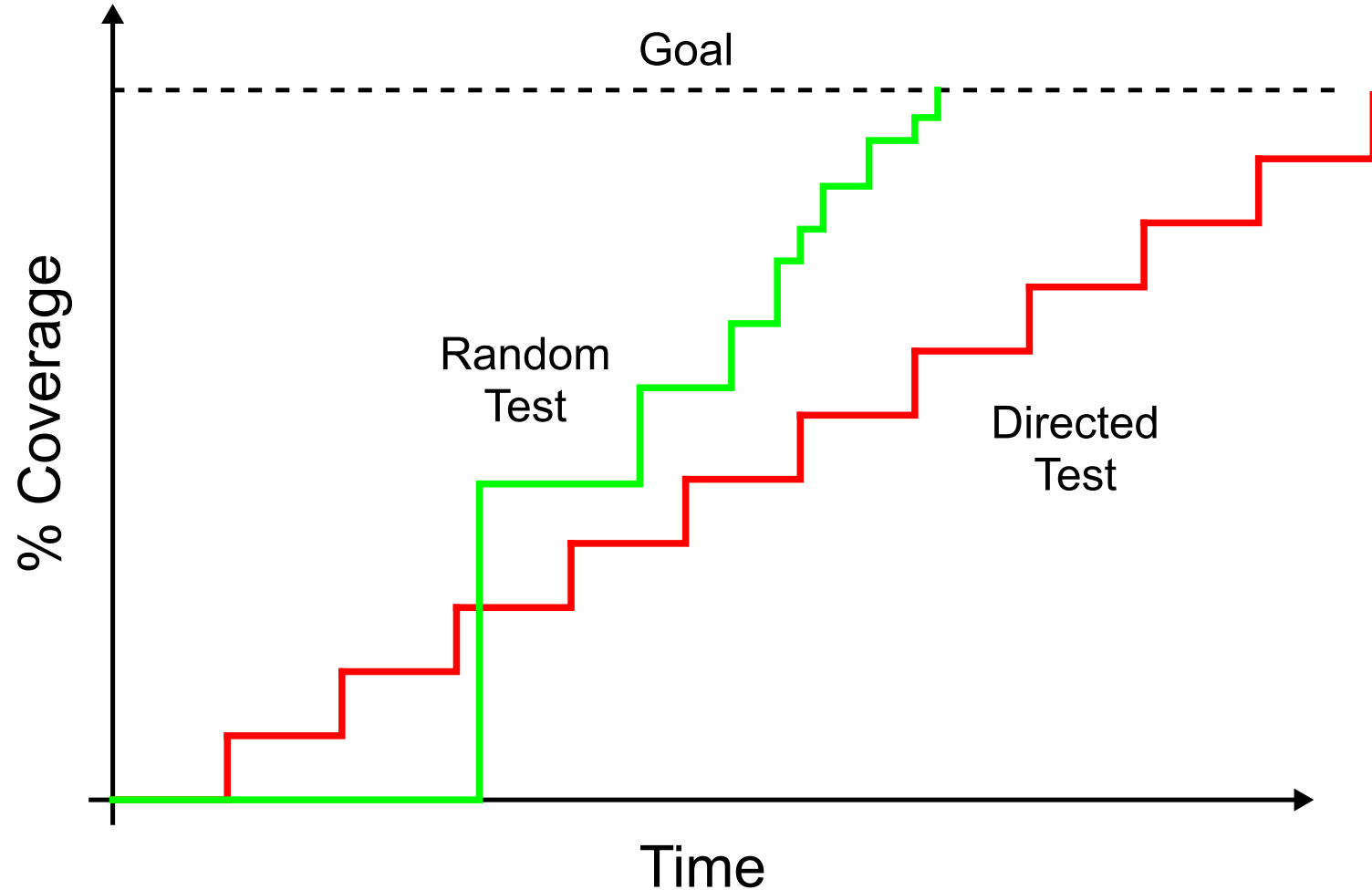


Verification Methodology

Anatomy of a Verification Environment



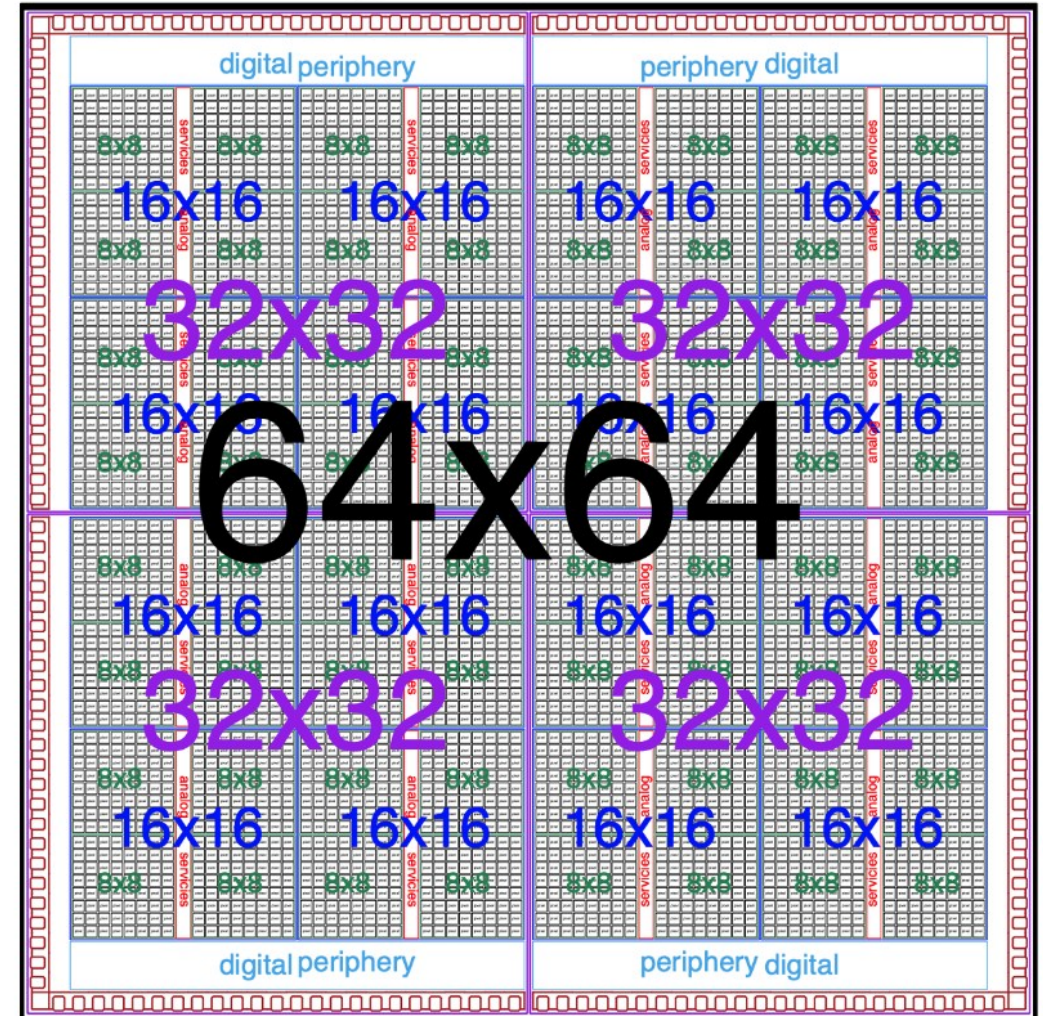
Constrained-random test progress over time vs directed testing



Research activities carried out so far (2nd year)

IGNITE ASIC

- **The IGNITE project aims at developing read-out and processing solutions for high intensity 4D-tracking**
 - Concurrent high time less than 50 ps and space resolution of 10 μm
 - Power density as low as possible around 1 W cm^{-2}
 - Operate at large fluences ($> 1 \times 10^{16}$ 1 MeV neutron per cm^2)
 - High total ionizing dose (TID > 1 Grad)
 - 28 nm CMOS technology

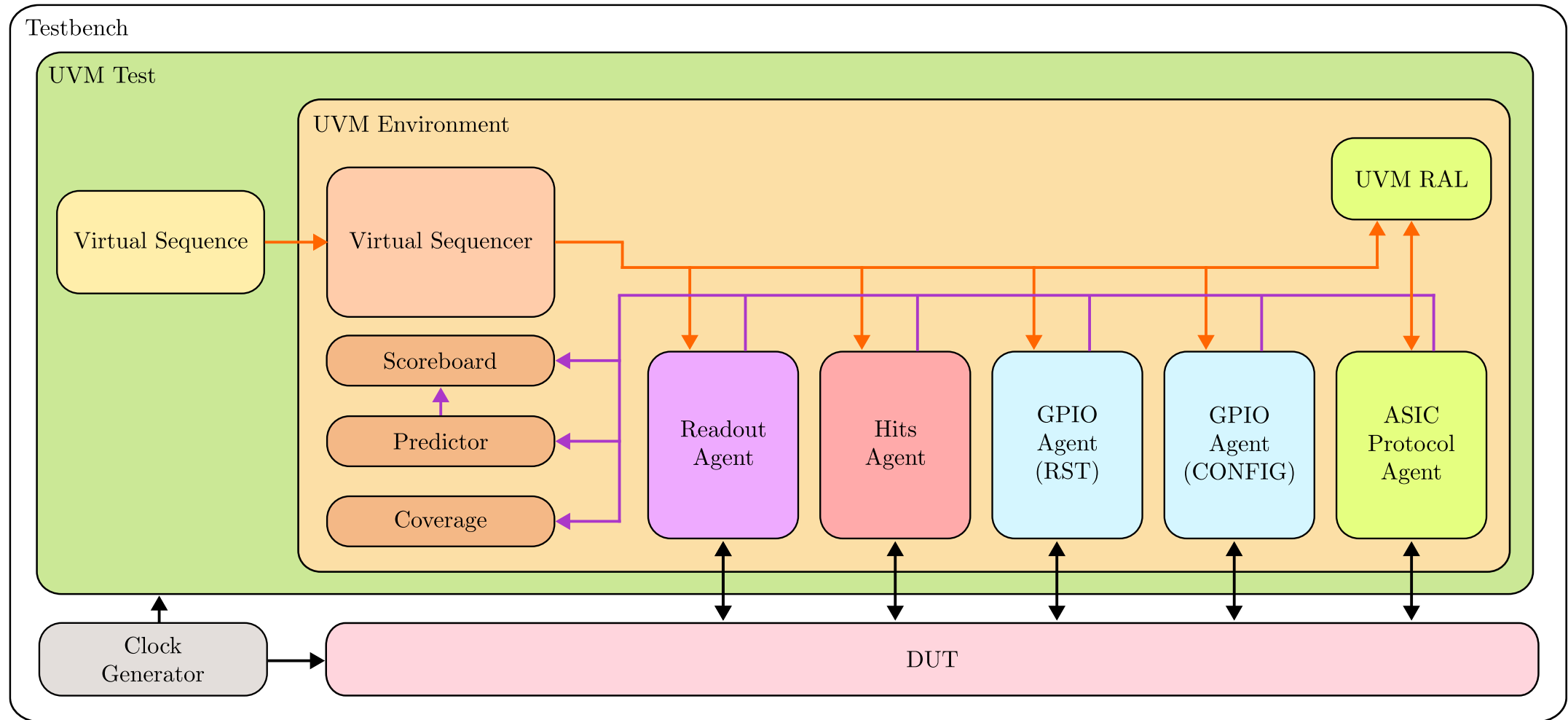


Activities carried out

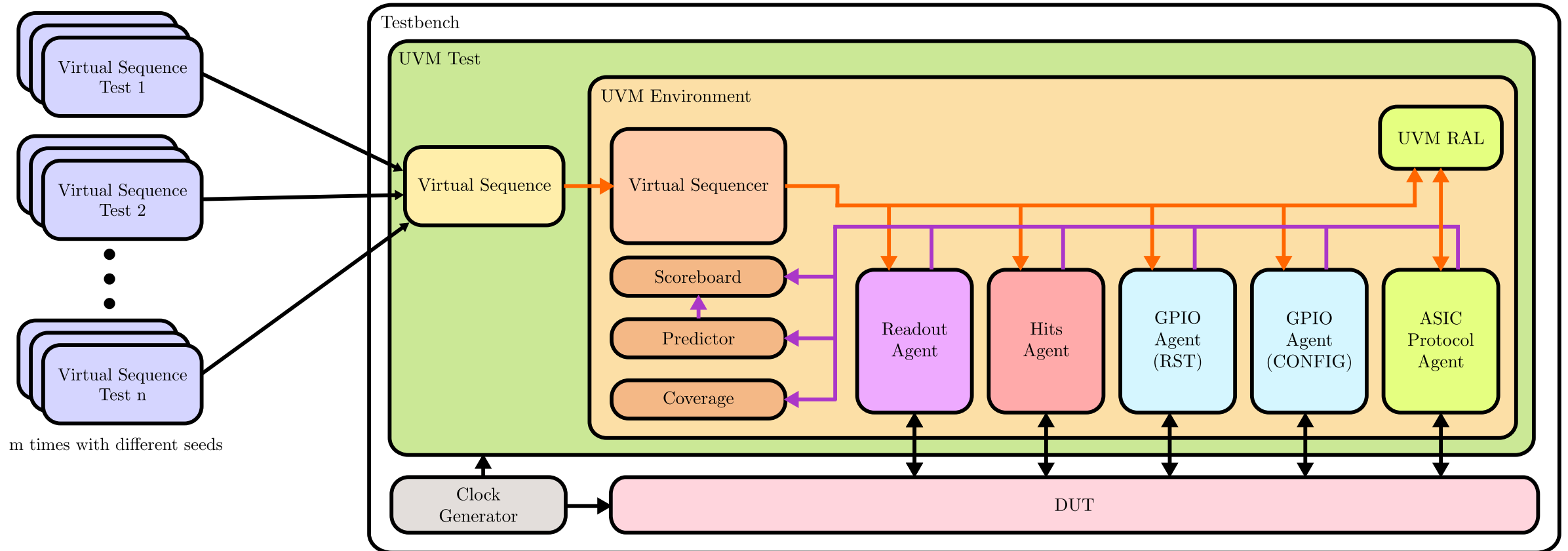
- Development of Verification Utility Tools and Scripts to facilitate workflow.
 - [GitHub pyuvcgen](#)
 - [GitHub pyralgen](#)
- Development of general purpose UVM Verification IPs (VIP) to be use in different projects (baltig.infn.it)
 - GPIO UVC
 - Clock Generator UVC
 - Hits UVC
 - Matt protocol UVC/RAL (SV/C++)
 - Readout UVC



IGNITE264 ASIC Verification Framework (1)



IGNITE264 ASIC Verification Framework (2)



Regression campaigns

Summary

Hierarchy Modules Groups Asserts Statistics Tests

Data from 221 tests was loaded.

Test Name/Test Location	Type	Started	Finished	Simulation
simv_cov/test_2025-07-11_08-23-18	Test Rec...	2025/07...	2025/07...	552132...
simv_cov/test_2025-07-11_08-23-16	Test Rec...	2025/07...	2025/07...	457132...
simv_cov/test_2025-07-11_08-23-13	Test Rec...	2025/07...	2025/07...	520132...
simv_cov/test_2025-07-11_08-23-11	Test Rec...	2025/07...	2025/07...	472132...
simv_cov/test_2025-07-11_08-23-09	Test Rec...	2025/07...	2025/07...	532882...
simv_cov/test_2025-07-11_08-23-06	Test Rec...	2025/07...	2025/07...	537132...
simv_cov/test_2025-07-11_08-23-04	Test Rec...	2025/07...	2025/07...	436632...
simv_cov/test_2025-07-11_08-23-02	Test Rec...	2025/07...	2025/07...	508632...
simv_cov/test_2025-07-11_08-23-00	Test Rec...	2025/07...	2025/07...	486382...
simv_cov/test_2025-07-11_08-22-58	Test Rec...	2025/07...	2025/07...	447882...
simv_cov/test_2025-07-11_08-22-55	Test Rec...	2025/07...	2025/07...	492882...
simv_cov/test_2025-07-11_08-22-53	Test Rec...	2025/07...	2025/07...	572382...
simv_cov/test_2025-07-11_08-22-51	Test Rec...	2025/07...	2025/07...	514132...
simv_cov/test_2025-07-11_08-22-48	Test Rec...	2025/07...	2025/07...	572882...
simv_cov/test_2025-07-11_08-22-46	Test Rec...	2025/07...	2025/07...	451632...

Category

Value

Test Name

Status

Command

Started

Host Name

rss_mem...

Peak Me...

random s...

User Name

CPU Time

workdir

Finished

Simulatio...

Test Loca...

Test Name

Status

Command

Started

Host Name

rss_mem...

Peak Me...

random s...

User Name

CPU Time

workdir

Finished

Simulatio...

Test Loca...

CovSrc.1

Uncovered

CovDetail

Line Toggle FSM Condition Branch Assert

Category Coverage

Message

simv_cov/test_2025-07-11_08-23-09

simv_cov/test_2025-07-11_08-23-11

simv_cov/test_2025-07-11_08-23-13

simv_cov/test_2025-07-11_08-23-16

simv_cov/test_2025-07-11_08-23-18

Exclusion Manager

Requirements Manager

Message

[Advisor] VC Formal FCA is recommended to raise the coverage rate.

Register coverage

<Verdi-Apex:vdCoverage:1>>vdb: simv_cov.vdb>

File View Plan Exclusion Tools Window Help

Summary

Hierarchy Modules Groups Asserts Statistics Tests

Avg. Group Score:19.90% U+C:963 U:789 C:174 X:0
Avg. Group Inst. Score:20.91% U+C:3535 U:3116 C:419 X:0

Group	Score	Instances	U+C	U	C	X	Goal
ral_regs_pkg::afe_global0_reg::cg_vals	0.00%	0.00%	20	20	0	0	100%
ral_regs_pkg::afe_global1_reg::cg_vals	0.00%	0.00%	20	20	0	0	100%
ral_regs_pkg::afe_tdc_global_reg::cg_vals	53.57%	53.57%	16	8	8	0	100%
ral_regs_pkg::cmd_reg::cg_vals	53.57%	53.57%	16	8	8	0	100%
ral_regs_pkg::dac_vfb_reg::cg_vals	0.00%	0.00%	66	66	0	0	100%
ral_regs_pkg::dac_vinj_h_reg::cg_vals	0.00%	0.00%	66	66	0	0	100%
ral_regs_pkg::dac_vinj_l_reg::cg_vals	0.00%	0.00%	66	66	0	0	100%
ral_regs_pkg::dac_vldo_reg::cg_vals	0.00%	0.00%	66	66	0	0	100%
ral_regs_pkg::dac_vth_h_reg::cg_vals	0.00%	0.00%	66	66	0	0	100%
ral_regs_pkg::dac_vth_l_reg::cg_vals	0.00%	0.00%	66	66	0	0	100%
ral_regs_pkg::ftdac_reg::cg_vals	0.00%	0.00%	32	32	0	0	100%
ral_regs_pkg::mattonella_reg_block_default_ma...	64.22%	64.22%	329	192	137	0	100%
ADDR	61.47%		109	42	67	0	100%
RW	100.00%		2	0	2	0	100%
ACCESS	31.19%		218	150	68	0	100%
regmodel	64.22%		329	192	137	0	100%
ral_regs_pkg::tdc_ctrl_reg::cg_vals	32.81%	32.81%	24	20	4	0	100%
ral_regs_pkg::tdc_reg::cg_vals	32.81%	31.79%	24	20	4	0	100%
ral_regs_pkg::tdc_tpsel_reg::cg_vals	25.78%	13.28%	68	65	3	0	100%
top_env_pkg::top_coverage::m_cov	55.56%		18	8	10	0	100%

CovSrc:1: ral_regs_pkg::m...ault_map_coverage::ra_cov

Uncovered

```

1050  covergroup ra_cov(string name) w
1051  th function sample(uvm reg addr t_addr, b
1052  it is read);
1053
1054  option.per_instance = 1;
1055  option.name = name;
1056
1057  ADDR: coverpoint addr {
1058    bins SET_TDC_DCO1_00 = {
1059      'h0 };
1060    bins SET_TDC_DCO1_01 = {
1061      'h1 };
1062    bins SET_TDC_DCO1_02 = {
1063      'h2 };
1064    bins SET_TDC_DCO1_03 = {
1065      'h3 };
1066    bins SET_TDC_DCO1_04 = {
1067      'h4 };
1068    bins SET_TDC_DCO1_05 = {
1069      'h5 };
1070    bins SET_TDC_DCO1_06 = {
1071      'h6 };
1072    bins SET_TDC_DCO1_07 = {
1073      'h7 };
1074    bins SET_TDC_DCO1_08 = {
1075      'h8 };
1076    bins SET_TDC_DCO1_09 = {
1077      'h9 };
1078    bins SET_TDC_DCO1_10 = {
1079      'ha };
1080    bins SET_TDC_DCO1_11 = {
1081      'hb };
1082    bins SET_TDC_DCO1_12 = {
1083      'hc };
1084    bins SET_TDC_DCO1_13 = {
1085      'hd };
1086    bins SET_TDC_DCO1_14 = {
1087      'he };
1088    bins SET_TDC_DCO1_15 = {
1089      'hf };
1090    bins SET_TDC_DCO1_16 = {
1091      'h10 };
1092    bins SET_TDC_DCO1_17 = {
1093      'h11 };
1094    bins SET_TDC_DCO1_18 = {
1095      'h12 };
1096    bins SET_TDC_DCO1_19 = {
1097      'h13 };
1098  }
1099
1100  RW: coverpoint t_addr {
1101    bins SET_TDC_DCO1_20 = {
1102      'h0 };
1103    bins SET_TDC_DCO1_21 = {
1104      'h1 };
1105    bins SET_TDC_DCO1_22 = {
1106      'h2 };
1107    bins SET_TDC_DCO1_23 = {
1108      'h3 };
1109    bins SET_TDC_DCO1_24 = {
1110      'h4 };
1111    bins SET_TDC_DCO1_25 = {
1112      'h5 };
1113    bins SET_TDC_DCO1_26 = {
1114      'h6 };
1115    bins SET_TDC_DCO1_27 = {
1116      'h7 };
1117    bins SET_TDC_DCO1_28 = {
1118      'h8 };
1119    bins SET_TDC_DCO1_29 = {
1120      'h9 };
1121    bins SET_TDC_DCO1_30 = {
1122      'ha };
1123    bins SET_TDC_DCO1_31 = {
1124      'hb };
1125    bins SET_TDC_DCO1_32 = {
1126      'hc };
1127    bins SET_TDC_DCO1_33 = {
1128      'hd };
1129    bins SET_TDC_DCO1_34 = {
1130      'he };
1131    bins SET_TDC_DCO1_35 = {
1132      'hf };
1133  }
1134
1135  ACCESS: coverpoint t_addr {
1136    bins SET_TDC_DCO1_36 = {
1137      'h0 };
1138    bins SET_TDC_DCO1_37 = {
1139      'h1 };
1140    bins SET_TDC_DCO1_38 = {
1141      'h2 };
1142    bins SET_TDC_DCO1_39 = {
1143      'h3 };
1144    bins SET_TDC_DCO1_40 = {
1145      'h4 };
1146    bins SET_TDC_DCO1_41 = {
1147      'h5 };
1148    bins SET_TDC_DCO1_42 = {
1149      'h6 };
1150    bins SET_TDC_DCO1_43 = {
1151      'h7 };
1152    bins SET_TDC_DCO1_44 = {
1153      'h8 };
1154    bins SET_TDC_DCO1_45 = {
1155      'h9 };
1156    bins SET_TDC_DCO1_46 = {
1157      'ha };
1158    bins SET_TDC_DCO1_47 = {
1159      'hb };
1160    bins SET_TDC_DCO1_48 = {
1161      'hc };
1162    bins SET_TDC_DCO1_49 = {
1163      'hd };
1164    bins SET_TDC_DCO1_50 = {
1165      'he };
1166    bins SET_TDC_DCO1_51 = {
1167      'hf };
1168    bins SET_TDC_DCO1_52 = {
1169      'h10 };
1170    bins SET_TDC_DCO1_53 = {
1171      'h11 };
1172    bins SET_TDC_DCO1_54 = {
1173      'h12 };
1174    bins SET_TDC_DCO1_55 = {
1175      'h13 };
1176    bins SET_TDC_DCO1_56 = {
1177      'h14 };
1178    bins SET_TDC_DCO1_57 = {
1179      'h15 };
1180    bins SET_TDC_DCO1_58 = {
1181      'h16 };
1182    bins SET_TDC_DCO1_59 = {
1183      'h17 };
1184    bins SET_TDC_DCO1_60 = {
1185      'h18 };
1186    bins SET_TDC_DCO1_61 = {
1187      'h19 };
1188    bins SET_TDC_DCO1_62 = {
1189      'h20 };
1190    bins SET_TDC_DCO1_63 = {
1191      'h21 };
1192    bins SET_TDC_DCO1_64 = {
1193      'h22 };
1194    bins SET_TDC_DCO1_65 = {
1195      'h23 };
1196    bins SET_TDC_DCO1_66 = {
1197      'h24 };
1198    bins SET_TDC_DCO1_67 = {
1199      'h25 };
1200    bins SET_TDC_DCO1_68 = {
1201      'h26 };
1202    bins SET_TDC_DCO1_69 = {
1203      'h27 };
1204    bins SET_TDC_DCO1_70 = {
1205      'h28 };
1206    bins SET_TDC_DCO1_71 = {
1207      'h29 };
1208    bins SET_TDC_DCO1_72 = {
1209      'h30 };
1210    bins SET_TDC_DCO1_73 = {
1211      'h31 };
1212    bins SET_TDC_DCO1_74 = {
1213      'h32 };
1214    bins SET_TDC_DCO1_75 = {
1215      'h33 };
1216    bins SET_TDC_DCO1_76 = {
1217      'h34 };
1218    bins SET_TDC_DCO1_77 = {
1219      'h35 };
1220    bins SET_TDC_DCO1_78 = {
1221      'h36 };
1222    bins SET_TDC_DCO1_79 = {
1223      'h37 };
1224    bins SET_TDC_DCO1_80 = {
1225      'h38 };
1226    bins SET_TDC_DCO1_81 = {
1227      'h39 };
1228    bins SET_TDC_DCO1_82 = {
1229      'h40 };
1230    bins SET_TDC_DCO1_83 = {
1231      'h41 };
1232    bins SET_TDC_DCO1_84 = {
1233      'h42 };
1234    bins SET_TDC_DCO1_85 = {
1235      'h43 };
1236    bins SET_TDC_DCO1_86 = {
1237      'h44 };
1238    bins SET_TDC_DCO1_87 = {
1239      'h45 };
1240    bins SET_TDC_DCO1_88 = {
1241      'h46 };
1242    bins SET_TDC_DCO1_89 = {
1243      'h47 };
1244    bins SET_TDC_DCO1_90 = {
1245      'h48 };
1246    bins SET_TDC_DCO1_91 = {
1247      'h49 };
1248    bins SET_TDC_DCO1_92 = {
1249      'h50 };
1250    bins SET_TDC_DCO1_93 = {
1251      'h51 };
1252    bins SET_TDC_DCO1_94 = {
1253      'h52 };
1254    bins SET_TDC_DCO1_95 = {
1255      'h53 };
1256    bins SET_TDC_DCO1_96 = {
1257      'h54 };
1258    bins SET_TDC_DCO1_97 = {
1259      'h55 };
1260    bins SET_TDC_DCO1_98 = {
1261      'h56 };
1262    bins SET_TDC_DCO1_99 = {
1263      'h57 };
1264    bins SET_TDC_DCO1_100 = {
1265      'h58 };
1266    bins SET_TDC_DCO1_101 = {
1267      'h59 };
1268    bins SET_TDC_DCO1_102 = {
1269      'h60 };
1270    bins SET_TDC_DCO1_103 = {
1271      'h61 };
1272    bins SET_TDC_DCO1_104 = {
1273      'h62 };
1274    bins SET_TDC_DCO1_105 = {
1275      'h63 };
1276    bins SET_TDC_DCO1_106 = {
1277      'h64 };
1278    bins SET_TDC_DCO1_107 = {
1279      'h65 };
1280    bins SET_TDC_DCO1_108 = {
1281      'h66 };
1282    bins SET_TDC_DCO1_109 = {
1283      'h67 };
1284    bins SET_TDC_DCO1_110 = {
1285      'h68 };
1286    bins SET_TDC_DCO1_111 = {
1287      'h69 };
1288    bins SET_TDC_DCO1_112 = {
1289      'h70 };
1290    bins SET_TDC_DCO1_113 = {
1291      'h71 };
1292    bins SET_TDC_DCO1_114 = {
1293      'h72 };
1294    bins SET_TDC_DCO1_115 = {
1295      'h73 };
1296    bins SET_TDC_DCO1_116 = {
1297      'h74 };
1298    bins SET_TDC_DCO1_117 = {
1299      'h75 };
1300    bins SET_TDC_DCO1_118 = {
1301      'h76 };
1302    bins SET_TDC_DCO1_119 = {
1303      'h77 };
1304    bins SET_TDC_DCO1_120 = {
1305      'h78 };
1306    bins SET_TDC_DCO1_121 = {
1307      'h79 };
1308    bins SET_TDC_DCO1_122 = {
1309      'h80 };
1310    bins SET_TDC_DCO1_123 = {
1311      'h81 };
1312    bins SET_TDC_DCO1_124 = {
1313      'h82 };
1314    bins SET_TDC_DCO1_125 = {
1315      'h83 };
1316    bins SET_TDC_DCO1_126 = {
1317      'h84 };
1318    bins SET_TDC_DCO1_127 = {
1319      'h85 };
1320    bins SET_TDC_DCO1_128 = {
1321      'h86 };
1322    bins SET_TDC_DCO1_129 = {
1323      'h87 };
1324    bins SET_TDC_DCO1_130 = {
1325      'h88 };
1326    bins SET_TDC_DCO1_131 = {
1327      'h89 };
1328    bins SET_TDC_DCO1_132 = {
1329      'h90 };
1330    bins SET_TDC_DCO1_133 = {
1331      'h91 };
1332    bins SET_TDC_DCO1_134 = {
1333      'h92 };
1334    bins SET_TDC_DCO1_135 = {
1335      'h93 };
1336    bins SET_TDC_DCO1_136 = {
1337      'h94 };
1338    bins SET_TDC_DCO1_137 = {
1339      'h95 };
1340    bins SET_TDC_DCO1_138 = {
1341      'h96 };
1342    bins SET_TDC_DCO1_139 = {
1343      'h97 };
1344    bins SET_TDC_DCO1_140 = {
1345      'h98 };
1346    bins SET_TDC_DCO1_141 = {
1347      'h99 };
1348    bins SET_TDC_DCO1_142 = {
1349      'h100 };
1350    bins SET_TDC_DCO1_143 = {
1351      'h101 };
1352    bins SET_TDC_DCO1_144 = {
1353      'h102 };
1354    bins SET_TDC_DCO1_145 = {
1355      'h103 };
1356    bins SET_TDC_DCO1_146 = {
1357      'h104 };
1358    bins SET_TDC_DCO1_147 = {
1359      'h105 };
1360    bins SET_TDC_DCO1_148 = {
1361      'h106 };
1362    bins SET_TDC_DCO1_149 = {
1363      'h107 };
1364    bins SET_TDC_DCO1_150 = {
1365      'h108 };
1366    bins SET_TDC_DCO1_151 = {
1367      'h109 };
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1369      'h110 };
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1371      'h111 };
1372    bins SET_TDC_DCO1_154 = {
1373      'h112 };
1374    bins SET_TDC_DCO1_155 = {
1375      'h113 };
1376    bins SET_TDC_DCO1_156 = {
1377      'h114 };
1378    bins SET_TDC_DCO1_157 = {
1379      'h115 };
1380    bins SET_TDC_DCO1_158 = {
1381      'h116 };
1382    bins SET_TDC_DCO1_159 = {
1383      'h117 };
1384    bins SET_TDC_DCO1_160 = {
1385      'h118 };
1386    bins SET_TDC_DCO1_161 = {
1387      'h119 };
1388    bins SET_TDC_DCO1_162 = {
1389      'h120 };
1390    bins SET_TDC_DCO1_163 = {
1391      'h121 };
1392    bins SET_TDC_DCO1_164 = {
1393      'h122 };
1394    bins SET_TDC_DCO1_165 = {
1395      'h123 };
1396    bins SET_TDC_DCO1_166 = {
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1398    bins SET_TDC_DCO1_167 = {
1399      'h125 };
1400    bins SET_TDC_DCO1_168 = {
1401      'h126 };
1402    bins SET_TDC_DCO1_169 = {
1403      'h127 };
1404    bins SET_TDC_DCO1_170 = {
1405      'h128 };
1406    bins SET_TDC_DCO1_171 = {
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1408    bins SET_TDC_DCO1_172 = {
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1412    bins SET_TDC_DCO1_174 = {
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1414    bins SET_TDC_DCO1_175 = {
1415      'h133 };
1416    bins SET_TDC_DCO1_176 = {
1417      'h134 };
1418    bins SET_TDC_DCO1_177 = {
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1420    bins SET_TDC_DCO1_178 = {
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1425      'h138 };
1426    bins SET_TDC_DCO1_181 = {
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1428    bins SET_TDC_DCO1_182 = {
1429      'h140 };
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1432    bins SET_TDC_DCO1_184 = {
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1463      'h157 };
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1471      'h161 };
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1483      'h167 };
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1647      'h249 };
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1744    bins SET_TDC_DCO1_340 = {
1745      'h298 };
1746    bins SET_TDC_DCO1_341 = {
1747      'h299 };
17
```

Results

- **Modular & (GPIO, Hits, Readout, Matt Protocol)**
 - Readout UVC: behaves as a full readout system emulator
 - C++ acceleration in Hits UVC for faster simulations
- **Register Modeling: UVM RAL API integrated with auto-generated RAL models**
- **Automation: Makefile-driven regression suite with scalable test campaigns**
- **Coverage-Driven Verification:**
 - Registers (RAL model)
 - Pixel behavior
 - GPIO interfaces
- **Reusability & Portability: Designed for future ASIC projects across HEP collaborations**

Plan for the 3rd year

Plan for the 3rd year

- **3rd Year**

- Continue working in the development of the verification framework and use it to verify the IGNITE chip
- Optimize the verification environment according to the project goals.
- Write the thesis
- Prepare for thesis defense

Thank you for your attention



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Backup slides



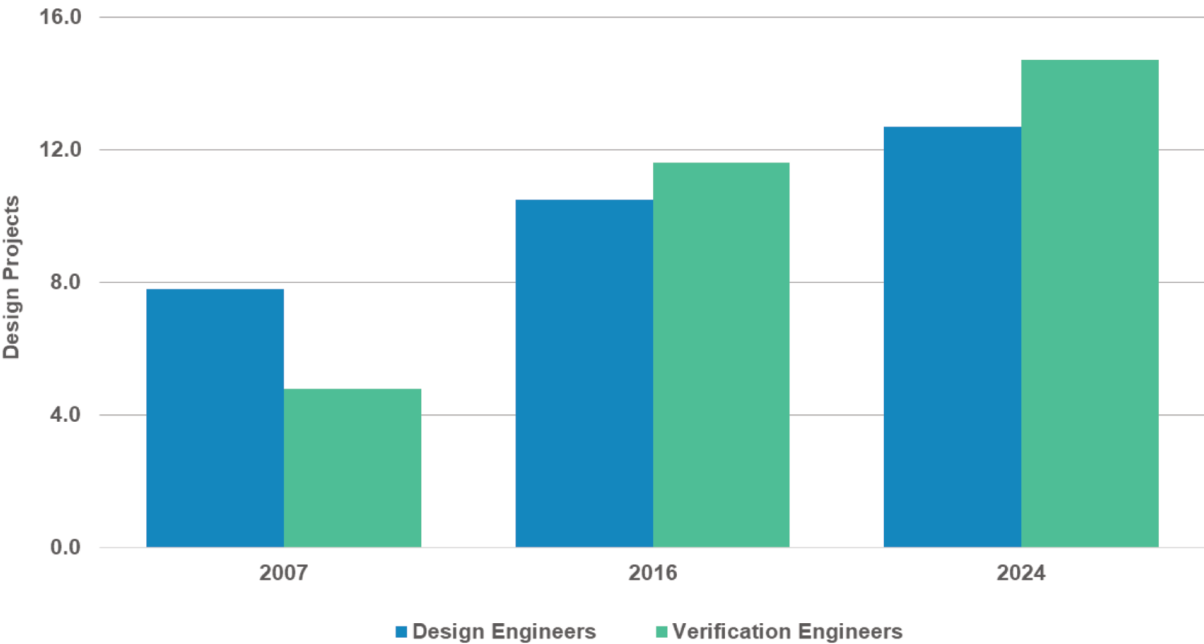
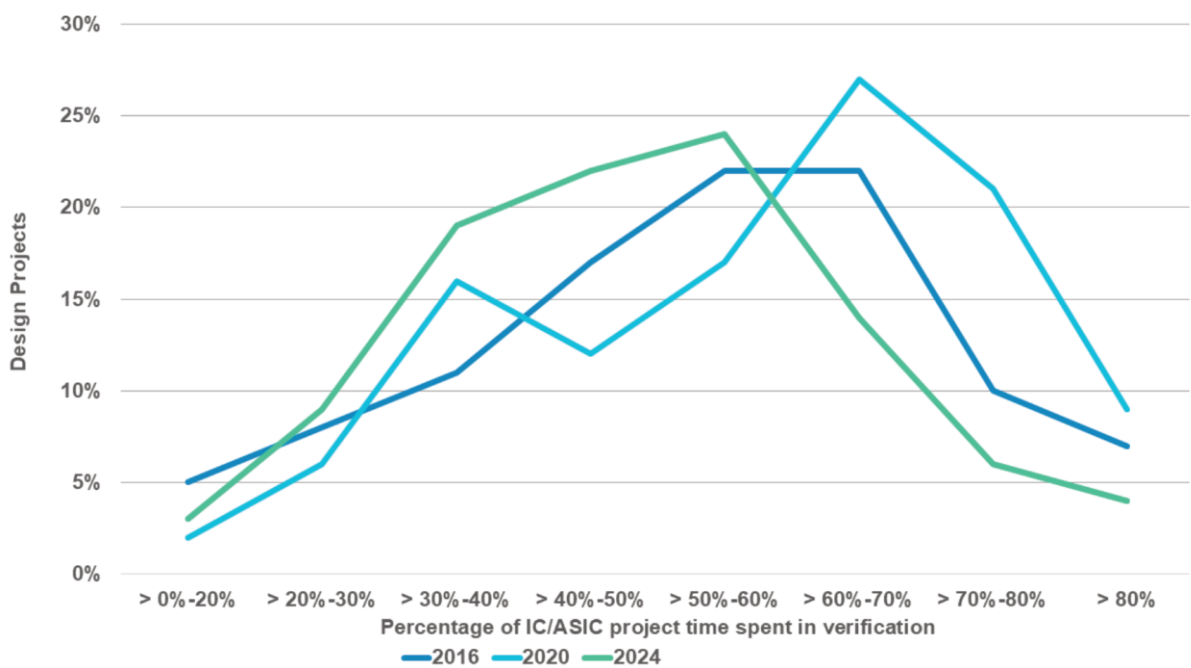
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Project time spent in verification & mean peak number of engineers



Example



hits_uvc

🔒

🔔

☆ Star 0

🍴 Fork 0

⋮

🔗 main

hits_uvc /

+ ▾

Find file

Edit ▾

Code ▾

⋮

🌿

style: change fatal error message and fix delays in top_test_vseq.sv
 Ciro Fabian Bermudez Marquez authored 1 month ago

789aebbf

📄

History

Name	Last commit	Last update
📁 analisys	refactor: change some code for t...	3 months ago
📁 env	feat: update hits_uvc with new U...	1 month ago
📁 rtl	feat: generate template files with...	6 months ago
📁 scripts	feat: add filter.py to project and ...	1 month ago
📁 sv	feat: update hits_uvc with new U...	1 month ago
📁 tb	feat: add and test the sequence_...	6 months ago
📁 tests	style: change fatal error messag...	1 month ago
🔖 .gitignore	feat: add C++ and gnuplot files t...	5 months ago
📄 README.md	docs: update README.md with b...	1 month ago
📄 hits_uvc.f	feat: generate template files with...	6 months ago
📄 notes.md	docs: add matrix to docs	3 months ago
📄 run.tcl	fix add new_frame to driver, mon...	6 months ago
📄 sve.f	feat: generate template files with...	6 months ago

Project information

🔗 52 Commits

🌿 4 Branches

🔖 1 Tag

📁 41 KiB Project Storage

📄 README

+ Add LICENSE

+ Add CHANGELOG

+ Add CONTRIBUTING

+ Enable Auto DevOps

+ Add Kubernetes cluster

+ Set up CI/CD

+ Add Wiki

+ Configure Integrations

Created on

February 06, 2025

Simulation technique trends

