



We are pleased to announce the upcoming "Advanced Course to FPGA Programming", scheduled for the coming October 27th–29th in Perugia. This comprehensive program is designed to equip participants with the latest advances in VHDL-based design for FPGA. This course is considered as a natural continuation of the [introductory course organized in Milano at the end of June](#).

The course is targeted at postgraduate researchers including bachelor degree or equivalent in fields such as physics, computer science, computer vision, engineering, working at any research institute, with interest in working on data acquisition, trigger or fast inference projects with at least a minimal knowledge of FPGA or VHDL.

### **Academic Program:**

The course is structured in 2.5 days of lectures and relatives hands-on sessions. The hands-on sections will be based on guided exercises and will be organized in order to grant students the real exploitation of FPGA equipped hardware.

The academic program consists of lectures and hands-on activities on the following topics:

Session 1 - Introduction and basic concepts: FPGA architecture, VHDL basic recap, VHDL general design flow and simulation tools

Session 2 - VHDL advances and Vivado Design Flow: VHDL advanced syntax, Vivado tool for VHDL to bitstream, scripting language for shell

Session 3 - Advanced design flow: Timing analysis, debug via ILA/VIO, block design generation for IP

Session 4-5: Tools at work: design flow for a complete optimized FPGA-FPGA interconnect based on AURORA transceivers: IP design, compilation and timing analysis, test&debug via ILA, fine tuning, performance evaluation

### **Basic Requirements:**

For effective attendance of the course it is required a basic knowledge of digital electronics, logic design and hardware block architecture, VHDL language and FPGA design flow.



Finanziato  
dall'Unione europea  
NextGenerationEU



Ministero  
dell'Università  
e della Ricerca



Italiadomani  
PIANO NAZIONALE  
DI RIPRESA E RESILIENZA



### Lecturers and facilitators:

The course will be held by lecturers and facilitators. The lecturers and facilitators are people who have gained substantial experience in the field of FPGA programming and have also acquired teaching skills during their career.

- Piero Vicini (INFN Sezione di Roma)
- Francesca Lo Cicero (INFN Sezione di Roma)
- Ottorino Frezza (INFN Sezione di Roma)
- Francesco Simula (INFN Sezione di Roma)
- Andrea Biagioni (INFN Sezione di Roma)

### Registration Details:

Enrollment is open. To secure your spot and for more information on the course schedule and instructors, please visit indico agenda at the following link: <https://agenda.infn.it/event/48014/>

### Organized by

- Istituto Nazionale Fisica Nucleare
- University of Perugia, Department of Physics and Geology
- University of Rome, La Sapienza, Department of Physics
- University of Milano Bicocca, Department of Physics

### Supported by

- Italian High-Performance Computing, Big Data e Quantum Computing Research Centre (ICSC)
- Società Italiana di Fisica (SIF)