

Characterisation of the CE-65v2 MAPS Test Structure towards High-Resolution Vertexing at the FCC-ee

In the context of the ALICE ITS3 collaboration, a set of MAPS small-scale test structures were developed in the 65 nm TPSCo CMOS process with the validation of the process for future vertexing applications as its primary focus.

One such sensor, the Circuit Exploratoire 65nm (CE-65), and its evolution the CE-65v2, were developed to explore charge collection properties for varying configurations including collection layer process (standard, blanket, modified with gap), pixel pitch (15, 18, 22.5 μm), and matrix geometry (square vs hexagonal/staggered).

In this contribution the characterisation of the CE-65v2 chip, based on Fe-55 lab measurements and test beams at CERN and DESY will be presented.

Focus will be given to the study of charge collection properties, pixel input capacitance, and pixel-by-pixel gain variations observed in lab tests.

Subsequently, the position resolution, hit-detection efficiencies, and charge sharing properties of the different chip configurations will be detailed, as well as their dependence on process modifications, pixel pitch, and matrix geometry.

These studies highlight that a sub-3 μm spatial resolution is achievable in a fine-pitch Modified with Gap design coupled with a binary readout, or a coarser-pitch Standard process sensor with a charge-sensitive readout, offering two promising avenues to satisfy the multifaceted requirements of a vertex detector at the FCC-ee.

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