

Current and future FCC-ee vertex detector layouts and their performance

This contribution presents the layouts and performance of the CLD and IDEA/ALLEGRO vertex detectors. Starting from this, more advanced layouts are explored:

- Ultra-light IDEA vertex detector concept using wafer-scale monolithic active pixel sensors (MAPS) stitched in two dimensions
- FCC-SEED vertex detector concept using MAPS stitched in one dimension
- A first look at a potential vertex detector with a reduced-thickness beam pipe, inspired by the ALICE3 vertex detector

Besides the layout comparison, the impact of the first layer position and of the sensor resolution is investigated. The contribution ends with a discussion on what other layouts should be studied and what the findings mean for future MAPS R&D.

Session

Layout and Simulation

Author: ILG, Armin (University of Zürich)

Presenter: ILG, Armin (University of Zürich)

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