

NAPA-p1: A Nanosecond MAPS Prototype for Future e^+e^- Colliders

NAPA-p1 is a Monolithic Active Pixel Sensor (MAPS) prototype developed in 65 nm CMOS imaging technology to meet the fast-timing and low-mass tracking requirements of future e^+e^- colliders. The chip features a $1.5 \times 1.5 \text{ mm}^2$ active area with a 25 μm pixel pitch, targeting nanosecond-level time resolution and a power density below 20 mW/cm².

Simulations predict a timing resolution of 350 ps-rms and an Equivalent Noise Charge (ENC) of 12 e^- rms under nominal operating conditions. Here we present the result of the front-end characterization to study the response behavior, threshold performance, and pixel uniformity. A 1080 nm pulsed laser setup is being prepared for future testing of the timing and efficiency performance. Further testing at the LESA test beam facility at SLAC, expected to be available in 2027, will enable beam-based validation of the NAPA as well as future MAPS developments for FCC. These results will guide further NAPA developments toward large-area stitched sensors for precision tracking in next-generation collider detectors.

Session

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