Perspectives for CMOS sensors for HEP in TPSCo 65nm ISC

October 30th 2025

Presenting work by many people in ALICE, EP R&D, DRD, …

DRD7.6

Complex imaging ASICs and technologies – Work Package overview

Project 7.6a: Common Access to Selected Imaging Technologies

Project Description

This project aims to provide common access to advanced imaging technologies through the organization of common fabrication runs, initially envisaged for the *TowerJazz 180 nm*, *TPSCo 65 nm ISC*, and the *LFoundry 110 nm IS* CMOS imaging technologies. IP development is also foreseen to accelerate and streamline the design effort.

Contributors:

CERN, IN2P3: CPPM, IPHC, IP2I + others, INFN(TO, TIFPA, MI, BO, PD, PV, PG, PI), NIKHEF, UiB, UiO and USN, STFC and SLAC already doing effort

Contact persons: Marlon Barbero, Jerome Baudot, Iain Sedgwick, Manuel Rolo, Walter Snoeys

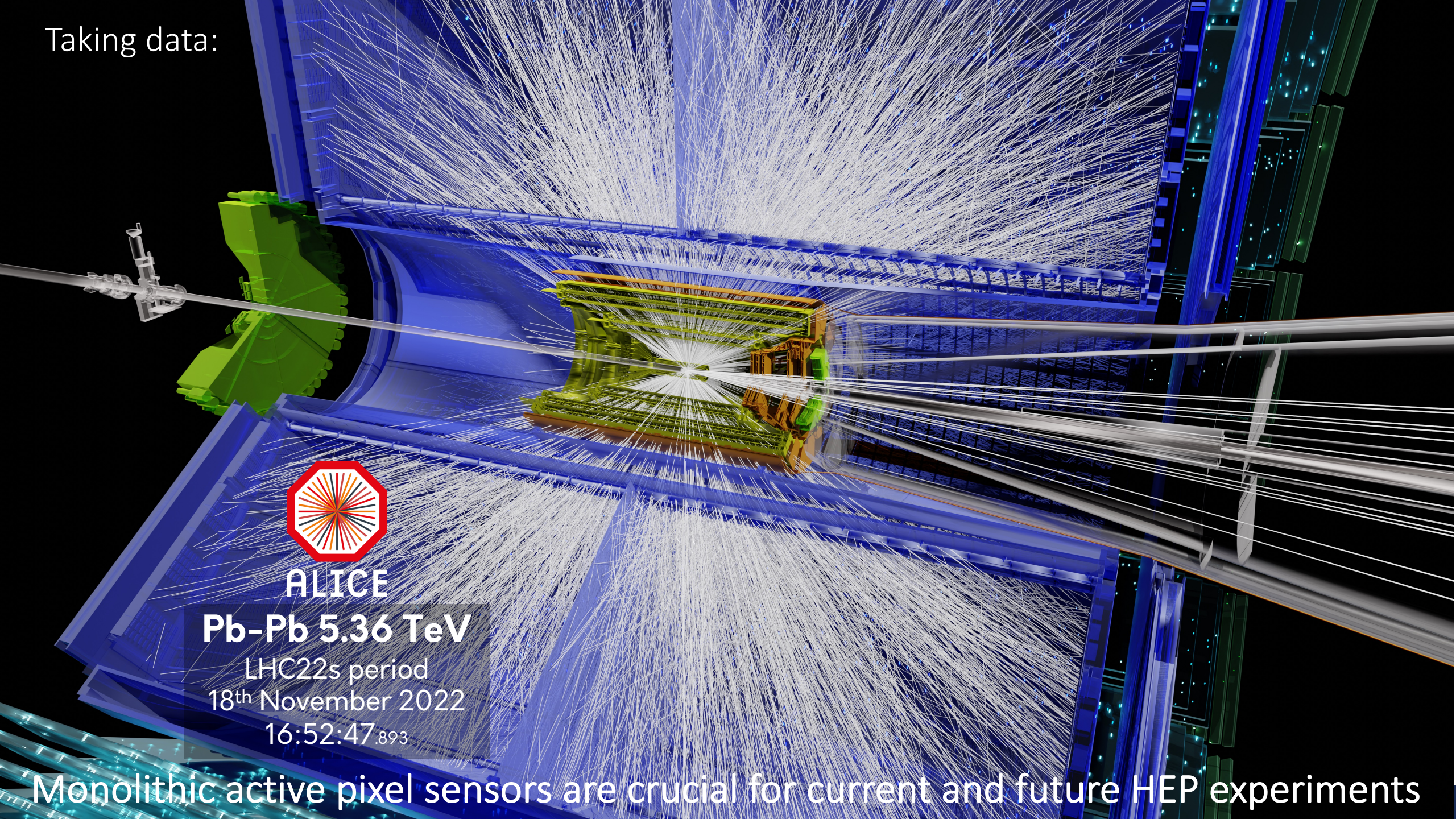
Project 7.6b: Shared access to 3D integration

Contact persons: Michele Caselle, Laci Andricek

This presentation will concentrate on TPSCo 65 nm ISC

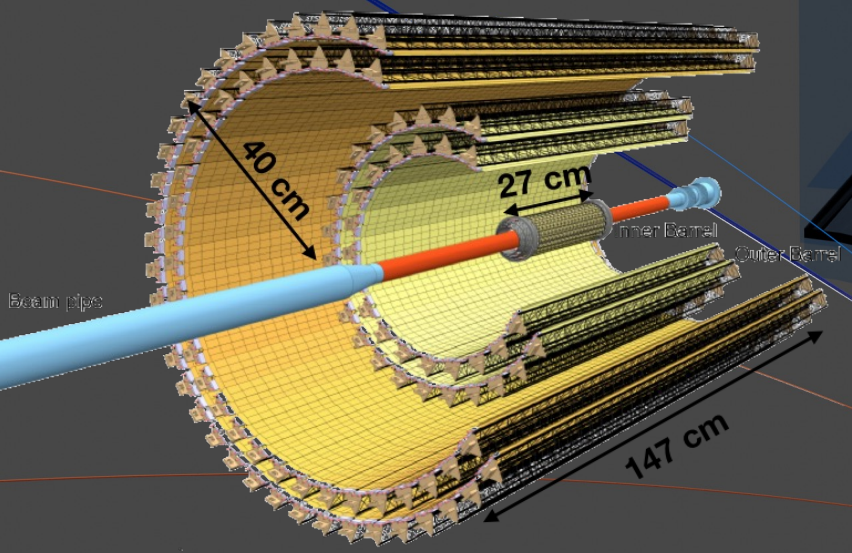
LFoundry 110 nm IS -> see Manuel Rolo's presentation

Taking data:



Monolithic active pixel sensors are crucial for current and future HEP experiments

ALICE Inner Tracker System 2 (ITS2) taking data



ITS 3 upgrade: replace 3 inner layers with wafer scale stitched sensors[1]

(1) https://indico.cern.ch/event/1071914, *ALICE ITS3 – a next generation vertex detector based on bent, wafer-scale CMOS* sensors, Magnus Mager (CERN)
(1) https://cds.cern.ch/record/2703140/files/LHCC-I-034.pdf - *Letter of Intent for an ALICE ITS Upgrade in LS3*

ALICE

CERN EP R&D WP1.2 for monolithic active pixel sensors

Targets the development of monolithic CMOS sensors for future HEP detectors in sub-100 nm technologies.

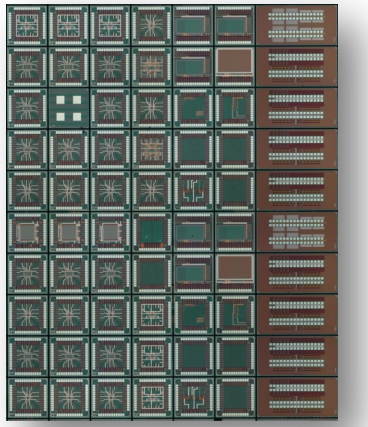
The first technology retained is the TPSCo 65 nm, and significant development in this technology was carried out in collaboration with the ALICE experiment for the upgrade of its inner tracking detector ITS3.

Main goals and activities:

- Design of wafer-scale stitched sensor on 300 mm wafers (application: ALICE vertex detector (ITS3), ALICE3…)
- Investigate new concepts for CMOS sensors:
  - Porting of hybrid pixel detector architecture into monolithic (hybrid to monolithic H2M)
- Performance optimization for future applications : smaller pitch, fast timing, low power, radiation tolerance
- Provide support and access to TPSCo 65 nm ISC imaging technology
  - **Continued in DRD7.6a**

CERN EP R&D day May 7th: https://indico.cern.ch/event/1524303/overview Giacomo Ripamonti's presentation
Presentation on support June 12th: https://indico.cern.ch/event/1553023/ Pedro Leitao's presentation

Timeline of TPSCo 65 nm submissions

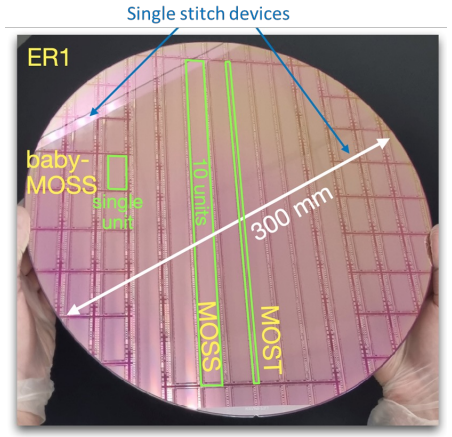


MLR1 (Multy-Layer Reticle, Dec 2020):

Learn about the technology, characterize pixels, transistors and building blocks

1.5 x 1.5 mm^2 test chips

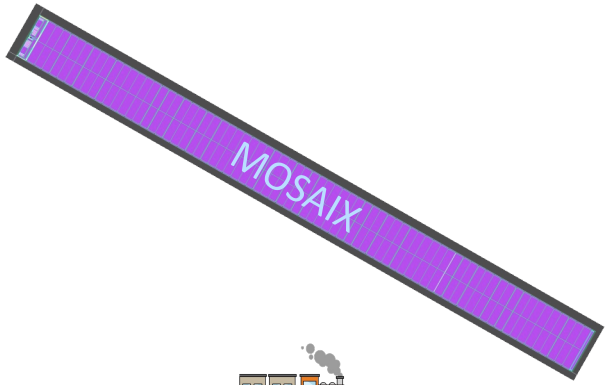
>50 chiplets from: DESY, IPHC, RAL, NIKHEF, CPPM, Yonsei, CERN



ER1 (Engineering Run, Dec. 2022):

Prove we can design wafer-scale stitched sensors

Included also chiplets



ER2 (August 2025):

Full-scale stitched sensor prototype for ALICE ITS3

Submitted, manufacturing just started

MPR2

Shared engineering run

WP 1.2 “rail”

ALICE “rail”

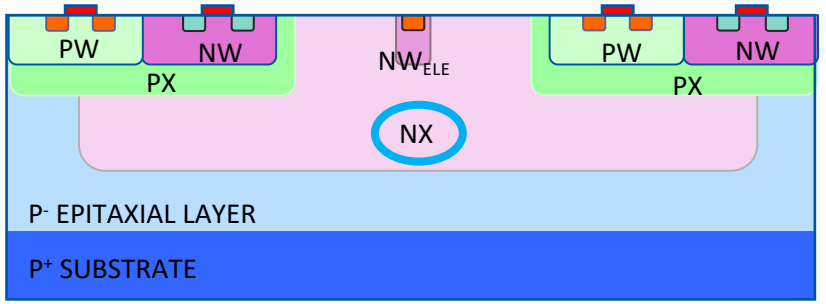
ER3 (2026):

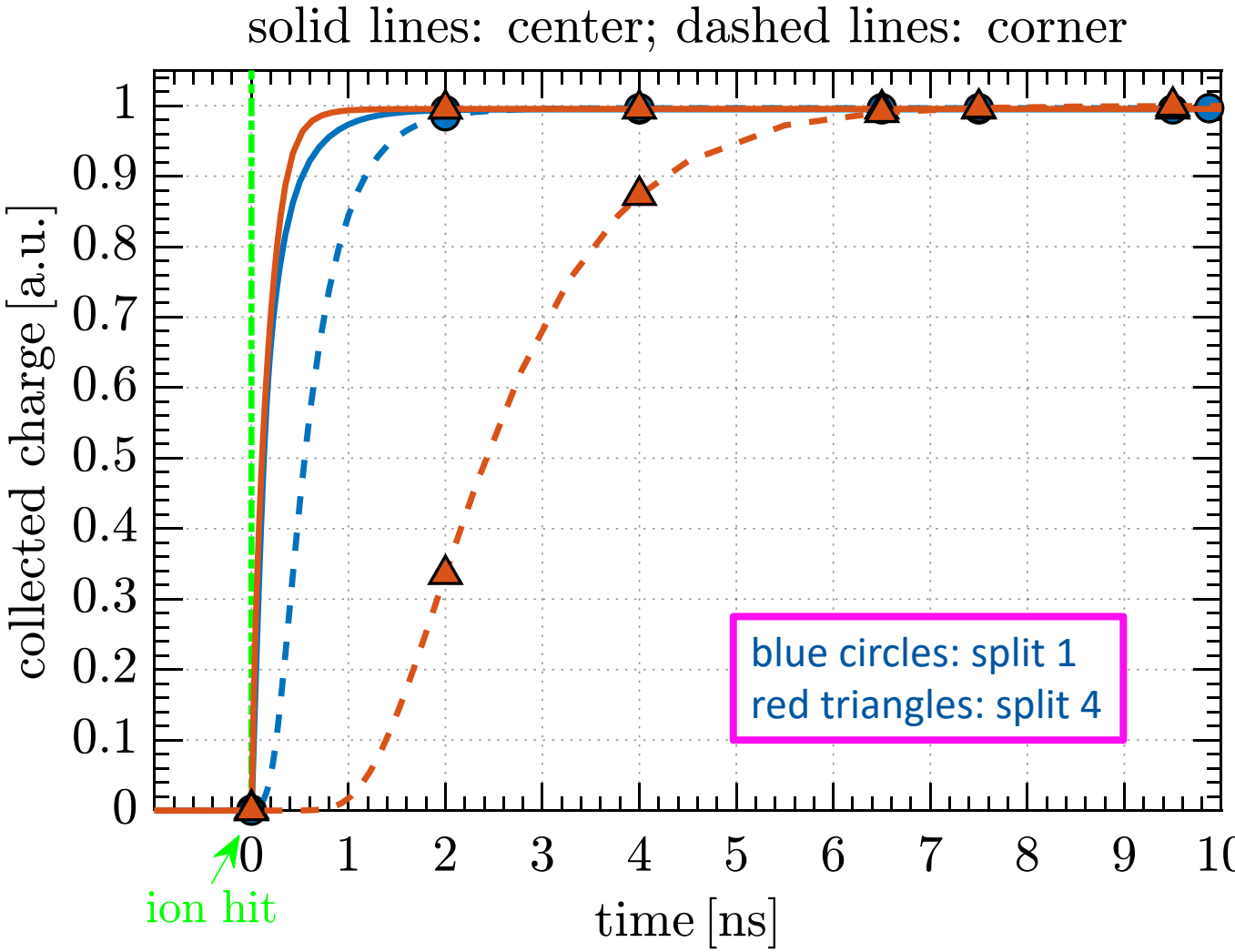
Stitched sensor production for ITS3 (ALICE-specific)

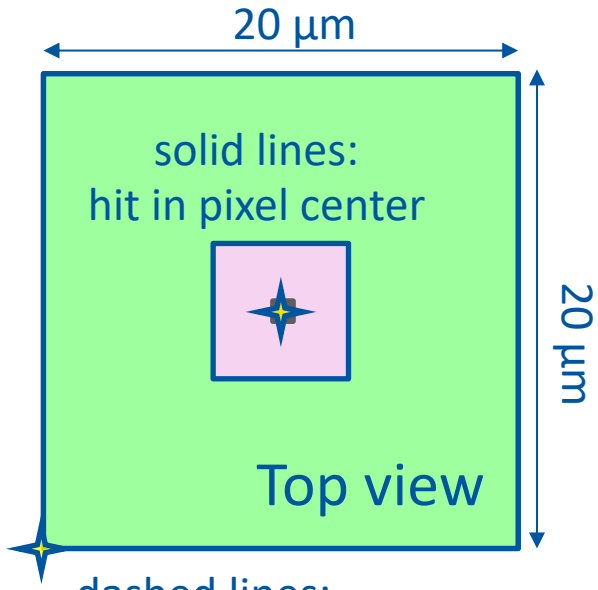
Sensor optimization: splits in ER1

Split 1: foundry doping
Split 4: reduced deep n-type implant (NX)

Structure similar to the one in 180 nm, modification more needed in 65 nm







Optimization requires inputs from large characterization effort

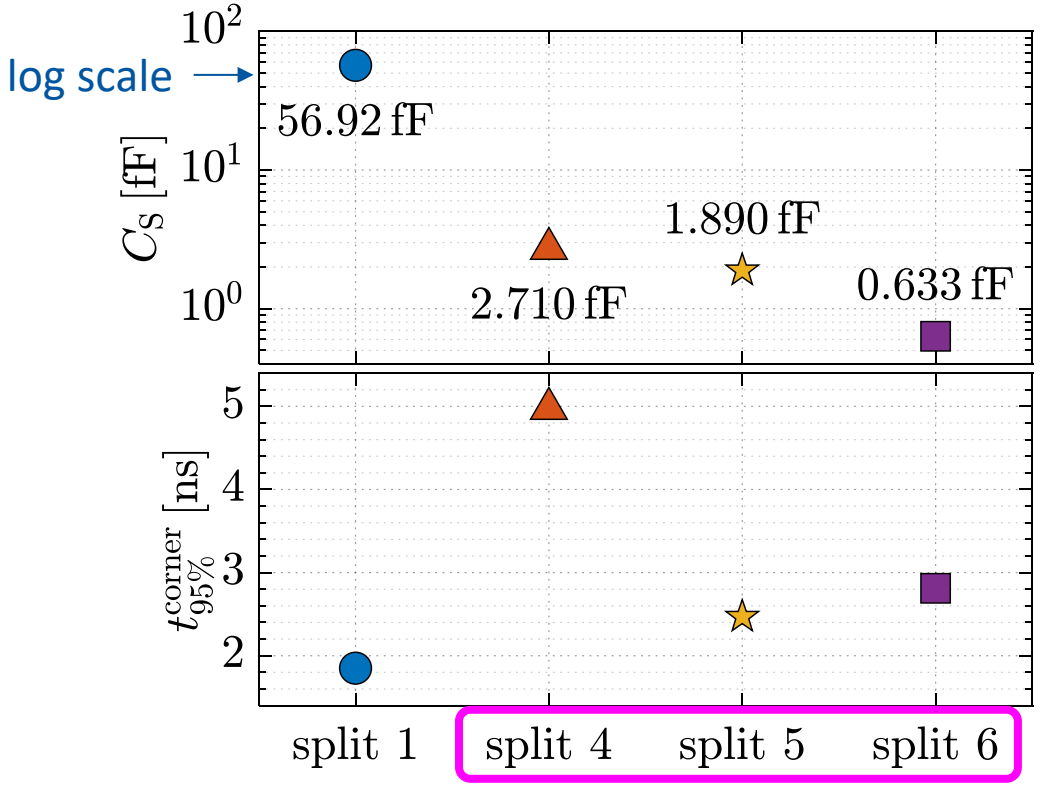
Further sensor optimization in ER2:

process modification in close collaboration with the foundry

G. Borghello, C. Lemoine, I. Sanna

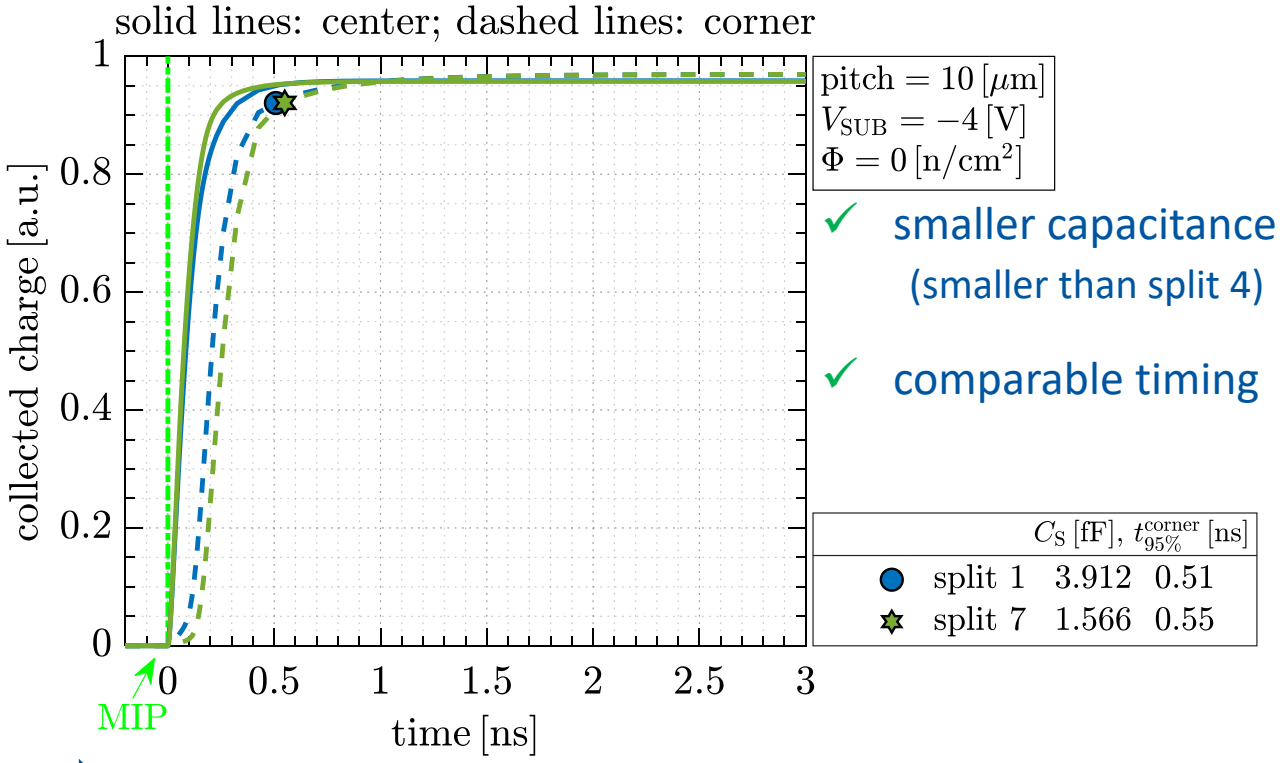
EP R&D

FOR ITS3: split 1 vs split 4 vs split 5 vs split 6



increasing deviations from standard profiles

FOR FUTURE UPGRADES: split 7

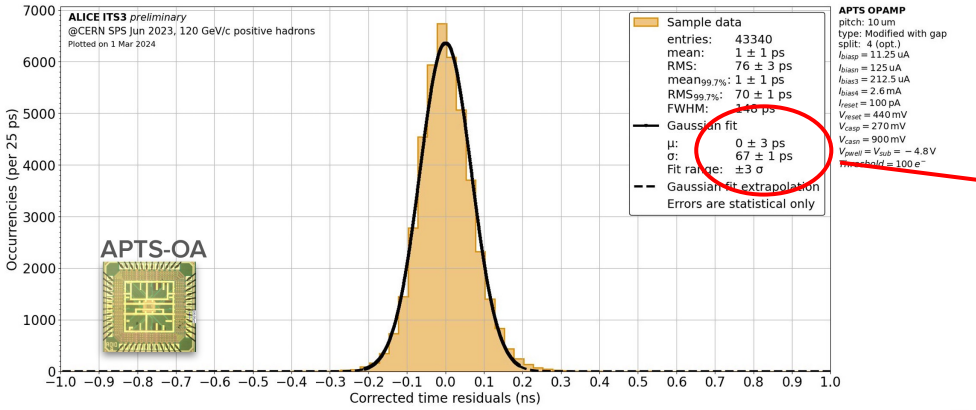


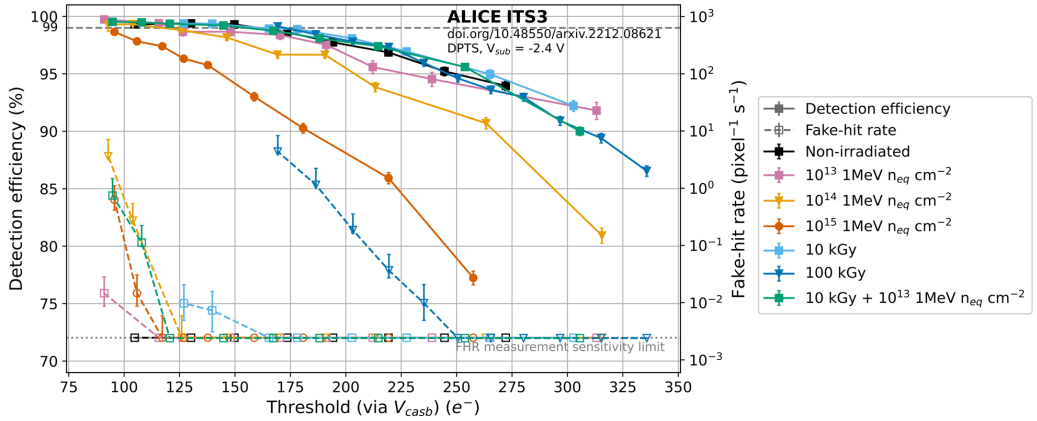
- ✓ smaller capacitance (smaller than split 4)
- ✓ comparable timing

10 μm pitch, -4 V reverse bias.

3 of the 4 splits for MOSAIX, the ITS3 prototype
~ 20 μm pitch, -1.2 V reverse bias.

MLR1: learning on sensor, front-end and readout





Lessons learned from MLR1:

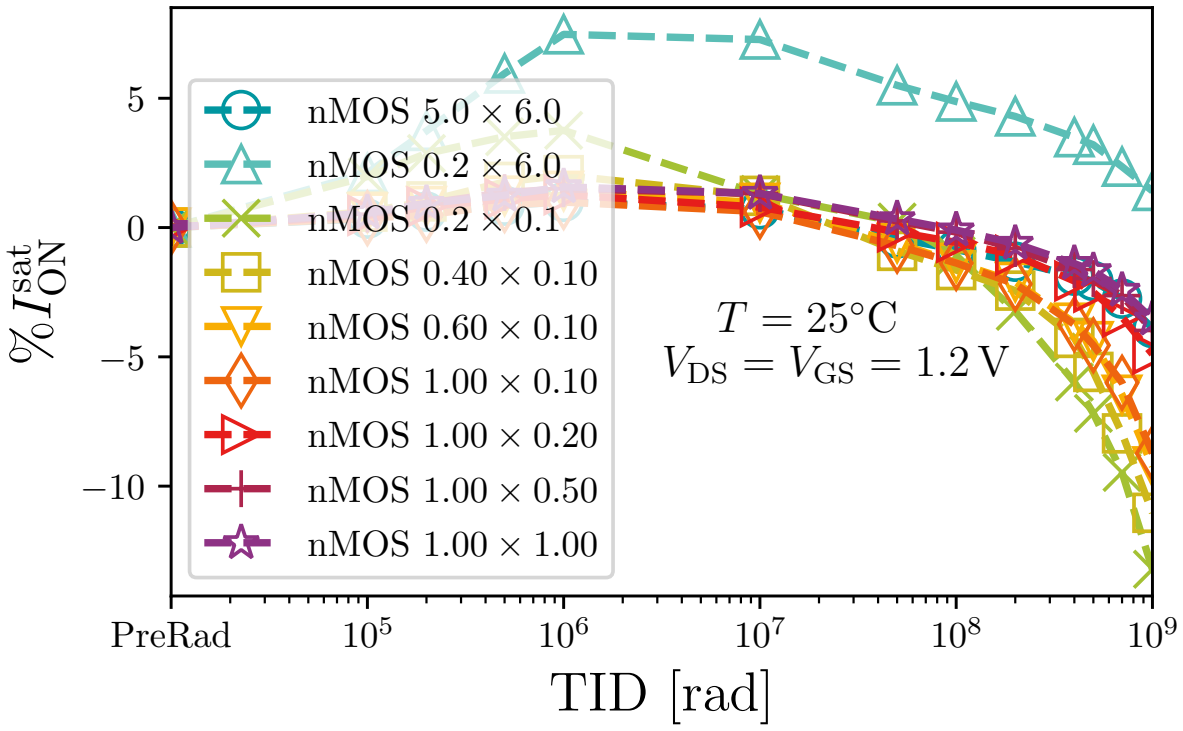
- < 100 ps timing precision (sensor + front-end only) [2]
- Fully efficient sensor, analog front end, digital readout chain with 15 x 15 µm^2 pixel [3]
- Transistor total ionizing dose tolerance and SEU in line with other 65 nm technologies
- Proof-of-principle that we can reach ~ 99 % detection efficiency at $10^{15}\ 1MeV\ neq\ cm^{-2}$ at room temperature

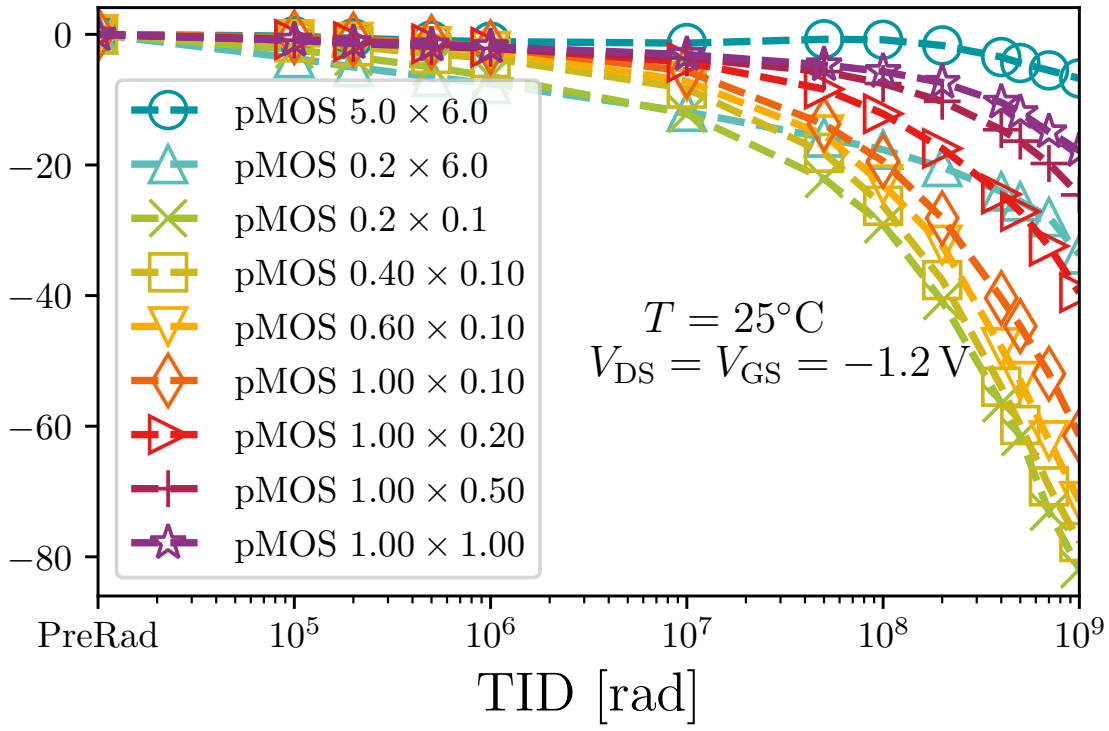
[1] “Characterization of analogue Monolithic Active Pixel Sensor test structures implemented in a 65 nm CMOS imaging process”. In: Nucl. Instr. and Meth. A 1070 (2025), 169896. doi: 10.1016/j.nima.2024.169896.

[2] “Time performance of Analog Pixel Test Structures with in-chip operational amplifier implemented in 65 nm CMOS imaging process”, In: Nucl. Instr. and Meth. A 1070 (2025), 170034. doi: 10.1016/j.nima.2024.170034.

[3] “Digital pixel test structures implemented in a 65 nm CMOS process” , In: Nucl. Instr. and Meth. A 1070 (2025), 168589. doi: 10.1016/j.nima.2024.168589.

Transistor radiation tolerance

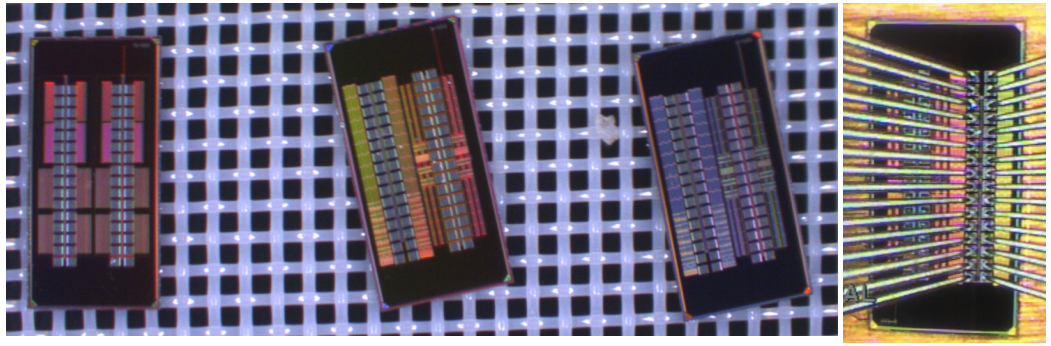




In line with other 65 nm technologies, no showstoppers.

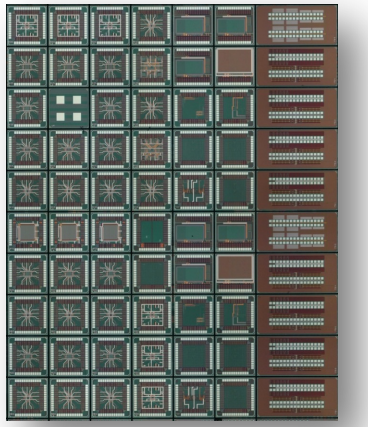
Small size PMOS transistors degrade significantly after several hundred Mrad.

Caveat: modeling of transistors with significant reverse bias



[4] A. Dorda Martin et al. “Measurements of total ionizing dose effects in TPSCo 65 nm and influence of NMOS bulk bias”. doi: 10.1088/1748-0221/18/02/C02036

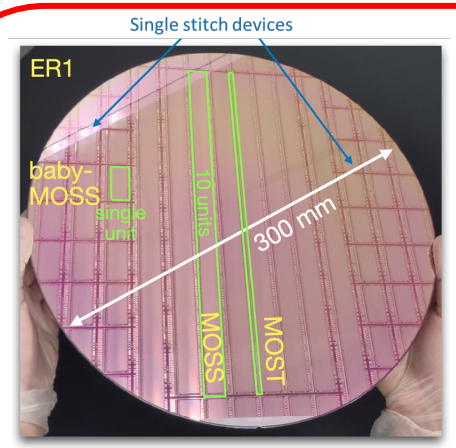
Timeline



MLR1 (Multy-Layer Reticle, Dec 2020):

1.5 x 1.5 mm^2 test chips

Learn about the technology, characterize pixels, transistors and building blocks



ER1 (Engineering Run, Dec. 2022):

Prove we can design wafer-scale stitched sensors

MOSS (1.4 x 25.9 cm)

MOST (0.25 x 25.9 cm)

Hybrid-To-Monolithic (H2M)

51 chiplets from: DESY, IPHC, RAL, NIKHEF, SLAC, INFN, CERN

ER2 (08/2025):

Full-scale stitched sensor prototype for ITS3

MPR2

Shared engineering run

WP 1.2 "rail"

ALICE "rail"

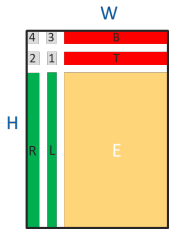
ER3 (2026):

Stitched sensor production for ITS3 (ALICE-specific)

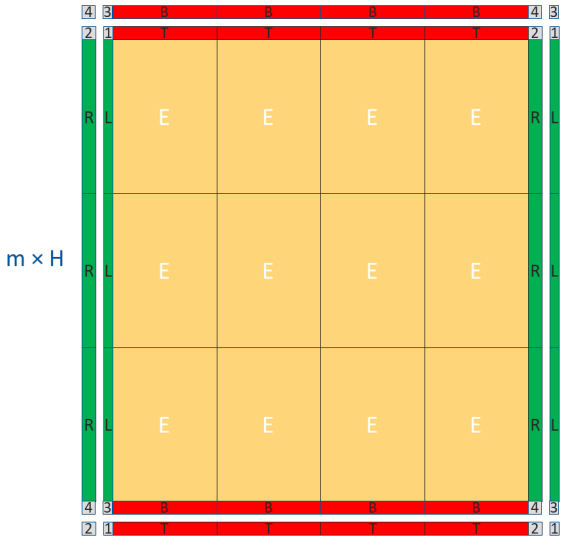
ER1: learning stitching and handling procedures

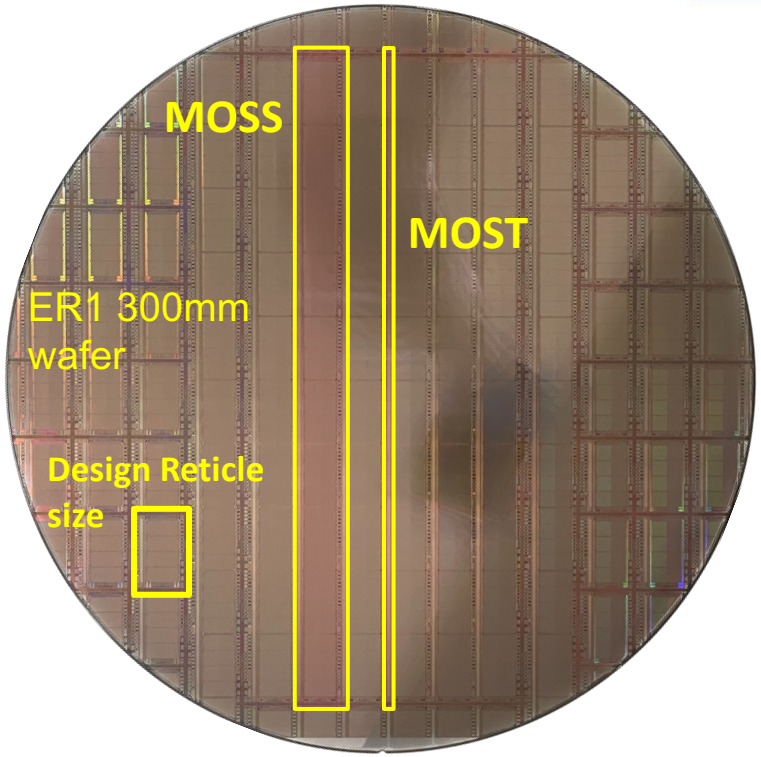
- Two wafer-scale stitched sensor chips
  - MOSS (Monolithic Stitched Sensor)
  - MOST (Monolithic Stitched Sensor with Timing)

Design Reticle
(typ. 2x3 cm)



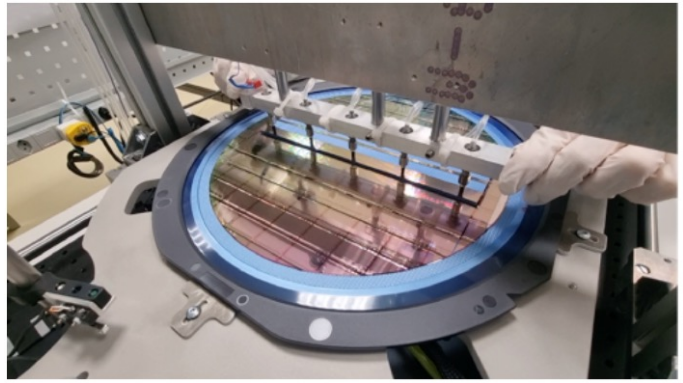
Stitched circuit on wafer
n × W

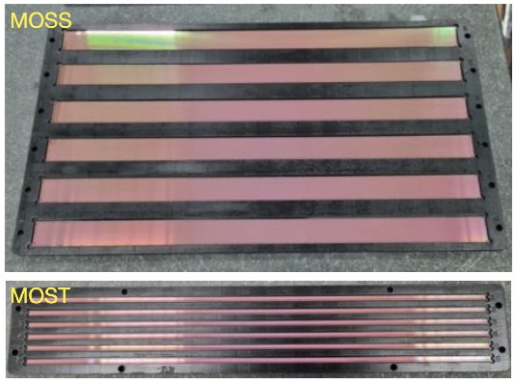




- Lots of learning on chip handling

- Several small test chips (1.5 mm × 1.5 mm)
  - H2M, PLL, pixel prototypes, fast serial links, SEU test chips, …

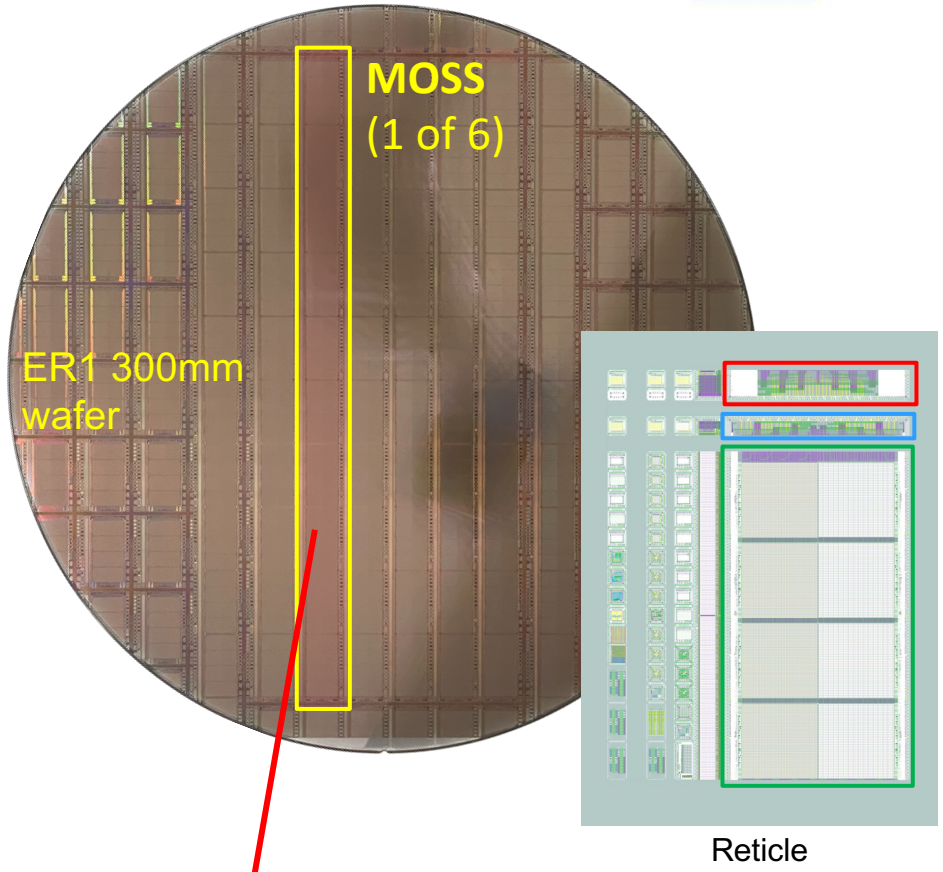


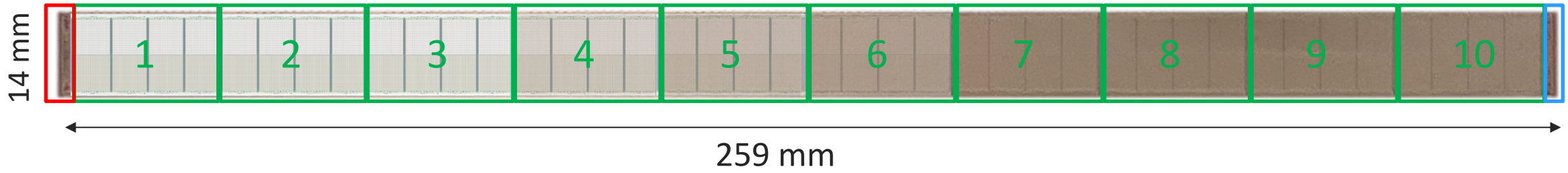


MOSS (Monolithic Stitched Sensor)

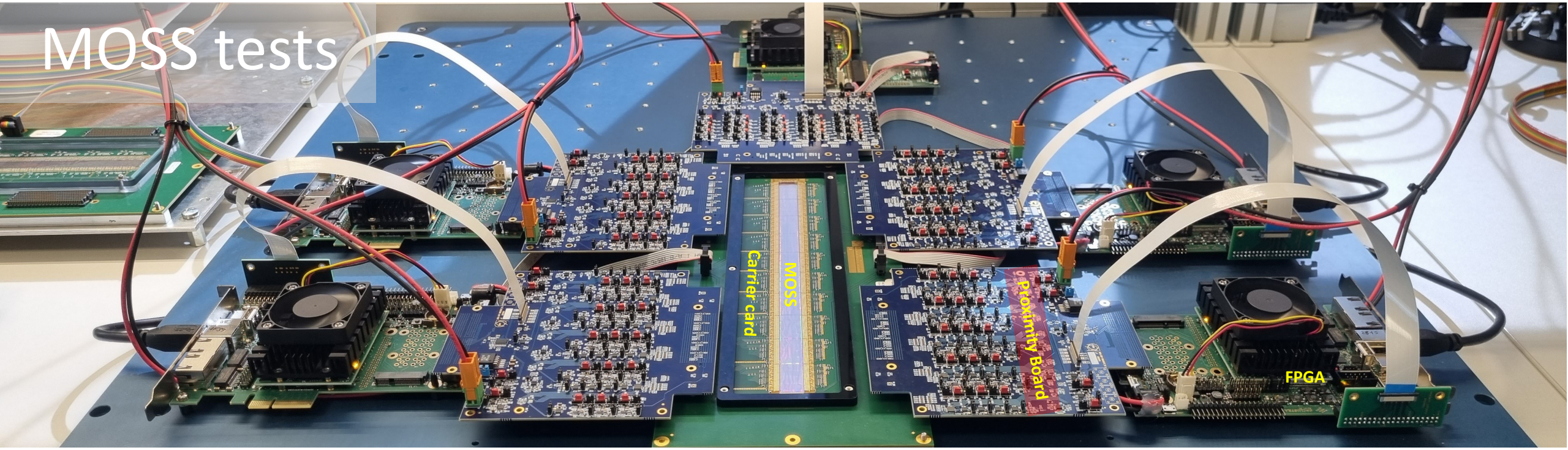
"Full-size" prototype for ALICE ITS3
14 mm × 259 mm, 6.72 Mpixels
Conservative design and layout, study yield and uniformity

- MOSS building blocks:
  - Repeated Sensor Unit (hosting pixel matrices, each RSU can be powered, controlled and read-out independently or from the Left Endcap)
  - Left Endcap (allows to provide power, control and read data from the short edge, as required by ITS3)
  - Right Endcap (allows to provide power from the short edge)
- Two pixel pitches (22.5 µm and 18 µm) to study the effects of layout density





MOSS tests

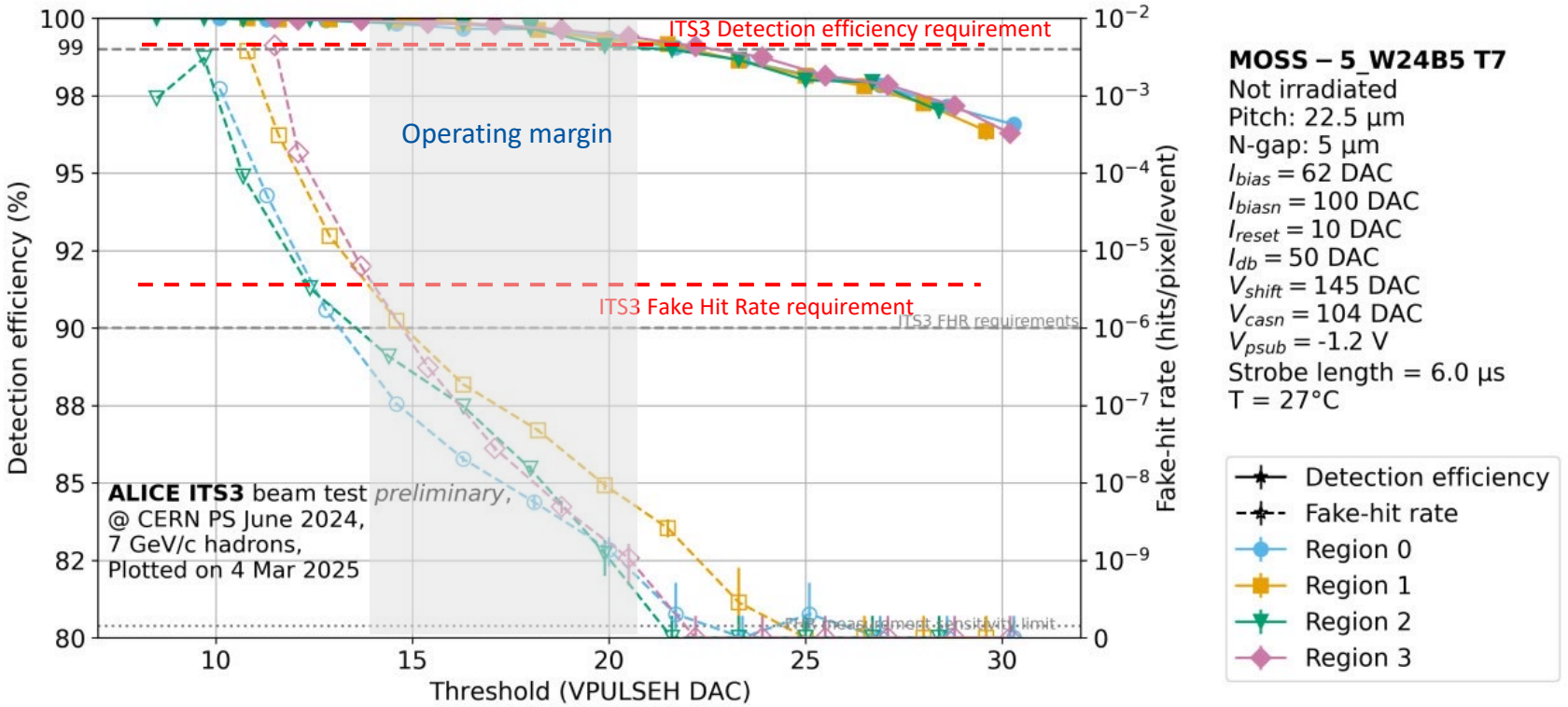


Testing of MOSS carried out entirely by the ALICE community.

Measurement setup: 1 carrier card + 5 proximity boards and 5 FPGA cards.

MOSS design has proven to be fully functional. Issue in a new, project-specific metal stack offered by the foundry, understood and addressed in a collaborative effort with the foundry, not expected in future runs.

MOSS Test beam results

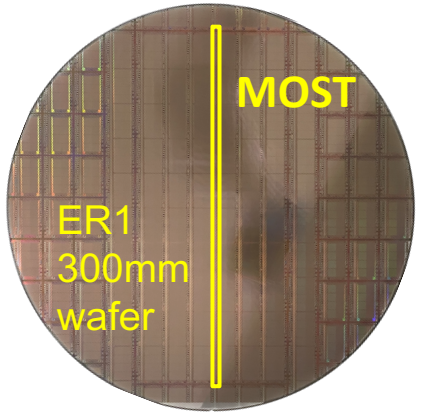


Before irradiation: good operating margin.

After irradiation: satisfactory operating margin at the radiation load estimated for ITS3 (~ 400 krad, ~ 4 x 10^{12} 1 MeV n_{eq}/cm^2, see [5]).

[5] L. Terlizzi. "Characterization of silicon Monolithic Stitched Sensors (MOSS) for the ALICE ITS3 for the LHC Run 4". In: Eleventh Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Strasbourg, November 2024).

MOST (Monolithic Stitched Sensor with timing)

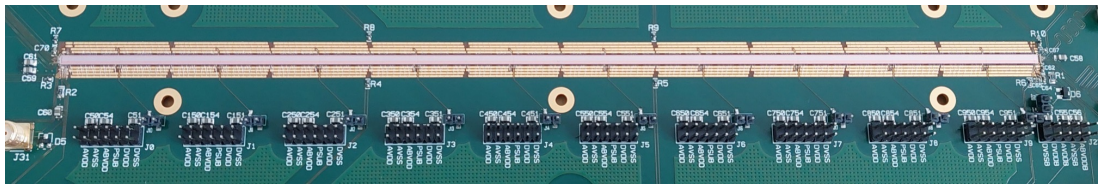


EP R&D

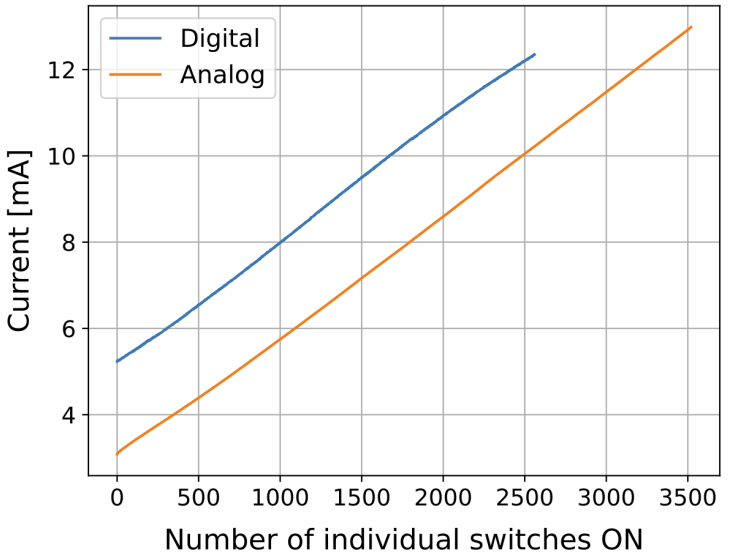
- MOST other stitched sensor on ER1
  - 259 x 2.5 mm, 18 micron pixel pitch
- Main differences with MOSS
  - Powering: global power distribution with power switches to switch off faulty parts, very densely designed circuit
  - Asynchronous, hit-driven readout for timing information + low power consumption
  - High-speed data transmission on chip
  - Reverse bias is applied to the sensor via the front-end

Significant testing effort, also at NIKHEF, more details in [6]

MOST on carrier board



25.9 cm



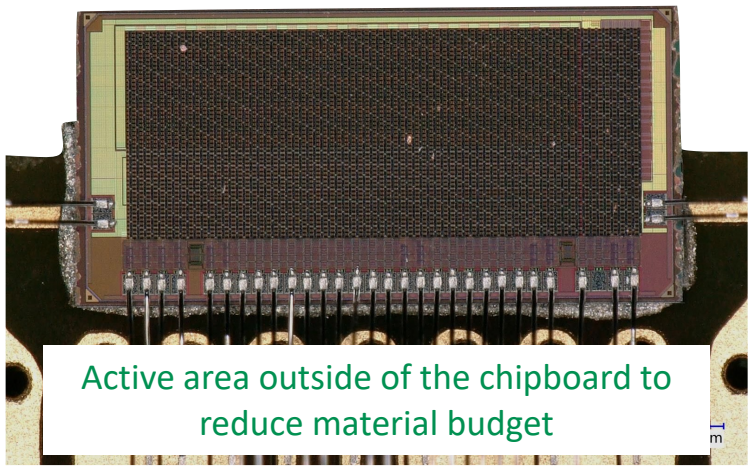
MOST current consumption vs. powered pixel groups (powered through power switches)

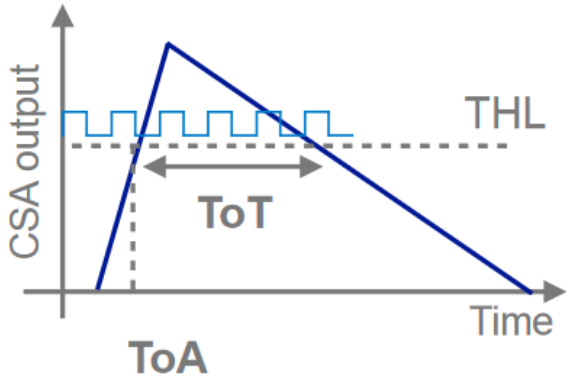
[6] M. Selina. "Exploring ALICE ITS3 MOST: Early Results on Power Segmentation and Asynchronous Readout for Timing in a Monolithic Stitched Sensor". In: Eleventh Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Strasbourg, November 2024), https://arxiv.org/pdf/2504.13696

[7] S. Bugiel et al. "ALICE ITS3 MOnolithic Stitched sensor with Timing (MOST): design overview and measurements highlights" TWEPP 2026"

H2M: yield and powering

- Technology demonstrator designed by WP 1.2, DESY and IFAE
- Ports a **hybrid pixel detector architecture into a monolithic chip**





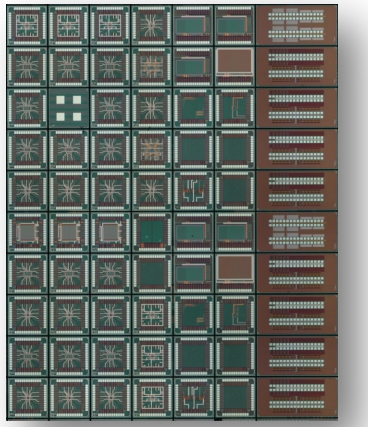
- **Pixel pitch: 35 µm in 64x16 pixel matrix**
- **Total thickness:** ~ 50 µm (epi ~10 µm)

- 4 Non-simultaneous acquisition modes
  - 8 bit **ToT**,
  - 8 bit **ToA** (100 MHz clock - 10 ns binning),
  - **counting** (#number of hits above threshold),
  - **triggered**.
- Readout: 40 MHz clock, frame-based without zero-suppression.

[8] S. Ruiz Daza at al. “The H2M Monolithic Active Pixel Sensor - characterizing non-uniform in-pixel response in a 65 nm CMOS imaging technology”. In: Eleventh Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Strasbourg, November 2024S. Ruiz Daza *et al* 2025 *JINST* **20** C06037

[9] C. Lemoine et al. “Impact of the circuit layout on the charge collection in a monolithic pixel sensor” C. Lemoine *et al* 2025 *JINST* **20** C06052

Timeline



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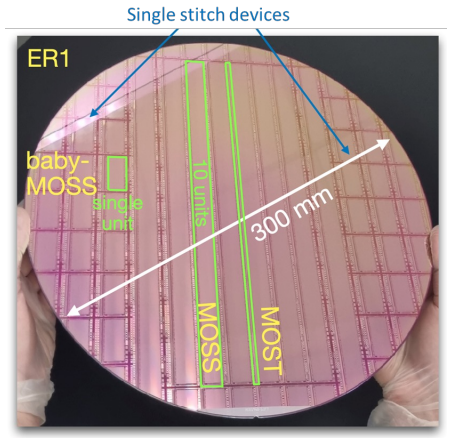

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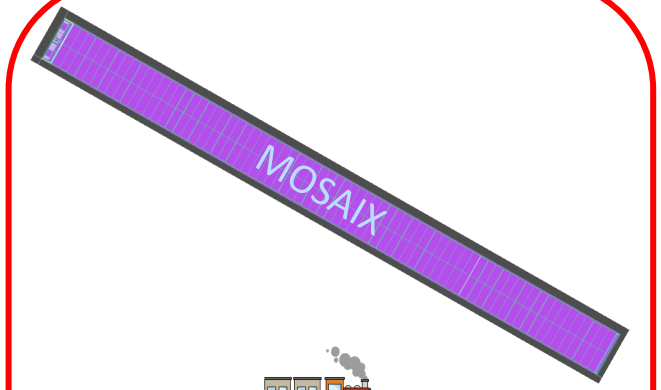
Prove we can design wafer-scale stitched sensors



ER2 (08/2025):

Full-scale stitched sensor prototype for ITS3

MOSAIX (1.9 x 26.6 cm)

~30 chiplets from: IPHC, SLAC, CPPM, BNL, INFN, Universität Heidelberg, CERN

MPR2

Shared engineering run

WP 1.2 "rail"

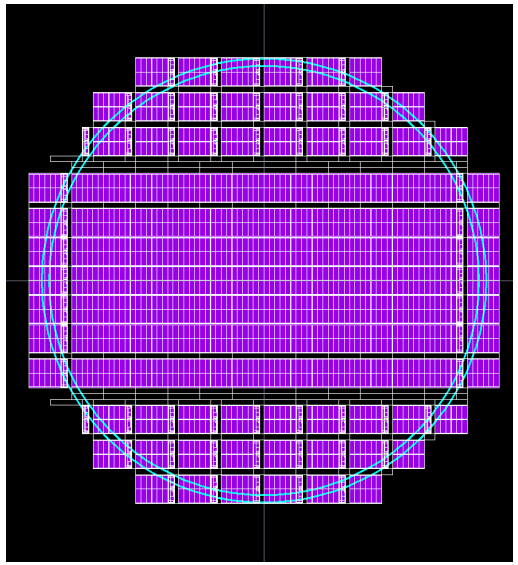
ALICE "rail"

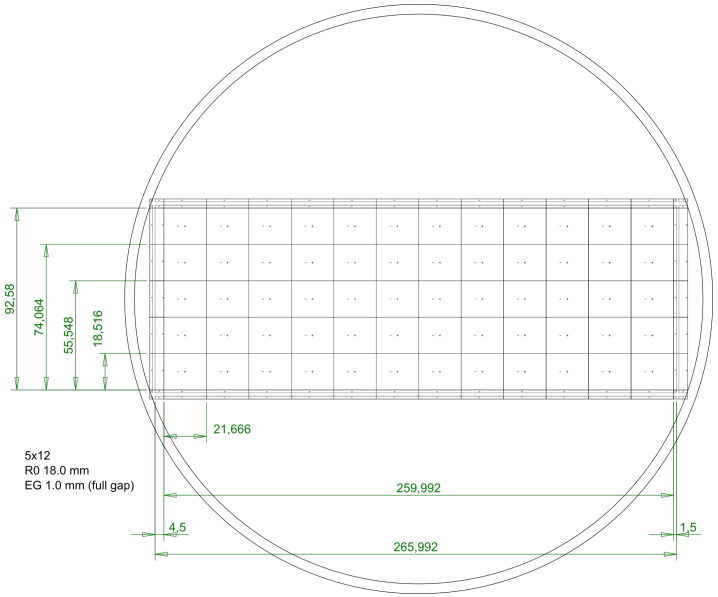
ER3 (2026):

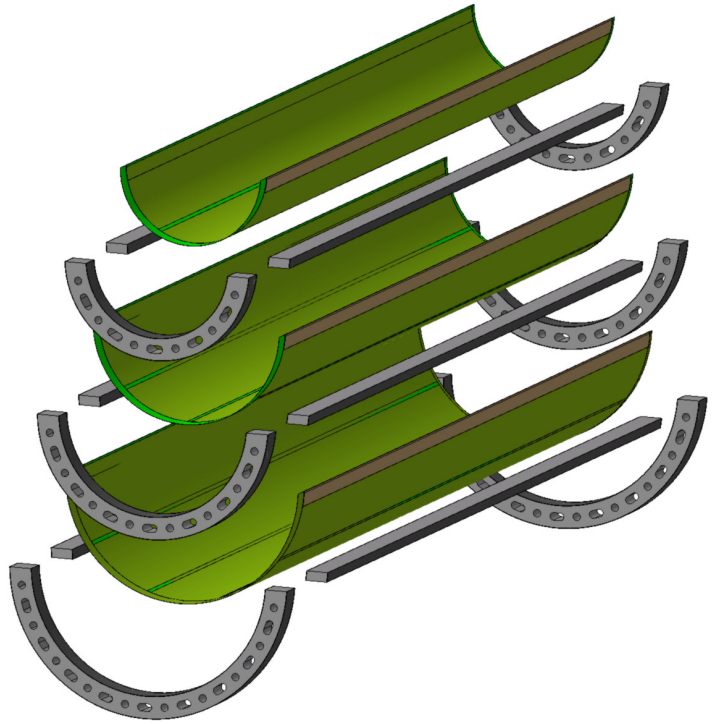
Stitched sensor production for ITS3 (ALICE-specific)

MOSAIX for the ALICE ITS3 upgrade, fabrication just started

- 12 repeated sensor units
- Learnings from MOSS and MOST on stitching are fed back into the design
- Power switches with power granularity from 20 in MOSS to 144 per segment here
- 3, 4 and 5 segments for layer 0, 1 and 2, respectively
- 12 pixel/bias variants, best one to be selected from measurements and submitted in ER3
- Includes ~ 30 chiplet positions, which can be changed for ER3.



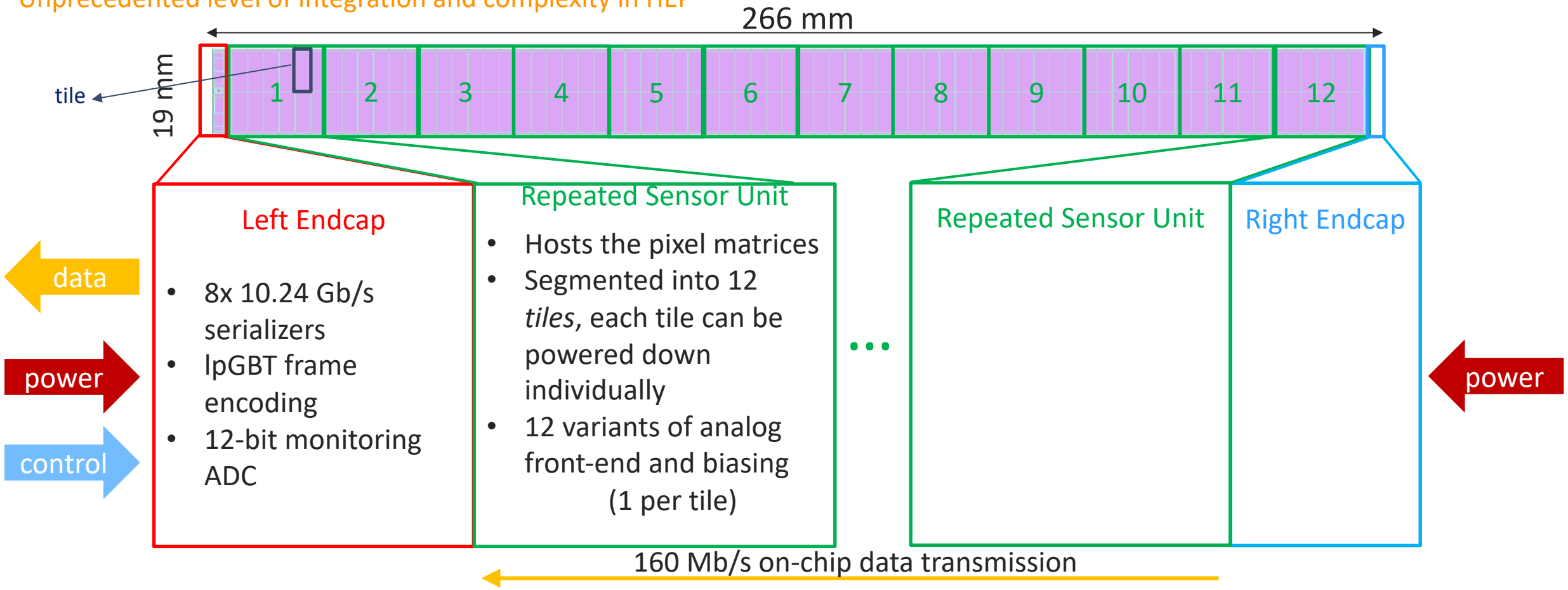




ITS3 TDR: https://cds.cern.ch/record/2890181?ln=en

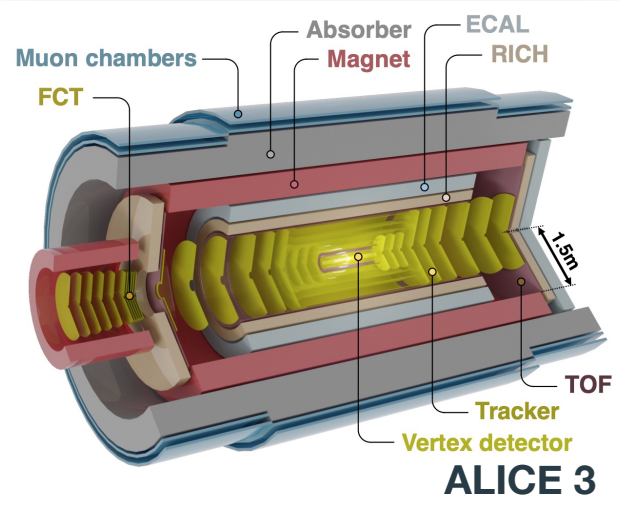
MOSAIX (Monolithic Stitched Active pIXel) SYSTEM ON CHIP

MOSAIX is the full-size, full-functionality, stitched sensor prototype for ALICE ITS3. 22.8 x 20.8 µm pixels, 9.97 Mpixels.
MOSAIX inherits features from MOSS (synchronous read-out, conservative layout) and MOST (power segmentation, data transmission on chip), but it includes many more complex functionalities. Attention to YIELD
Unprecedented level of integration and complexity in HEP



[9] P. Vicente Leitao. "Development of the MOSAIX chip for the ALICE ITS3 upgrade". In: Topical Workshop for Electronics in Particle Physics (Glasgow, September 2024).

ALICE 3:

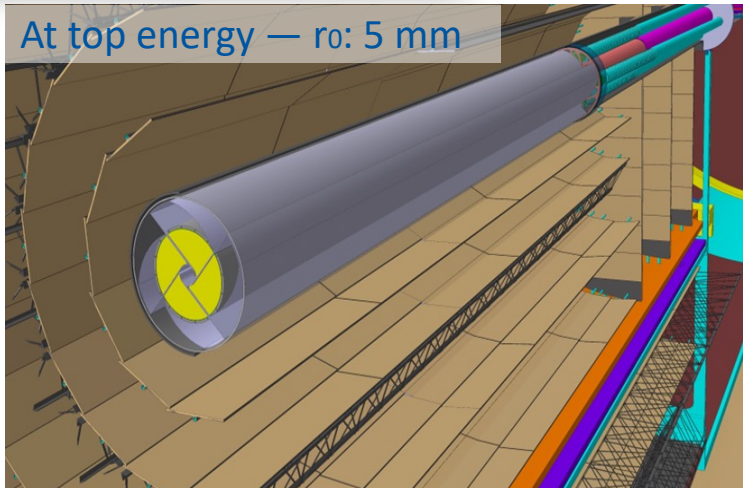


Detector concept

https://arxiv.org/pdf/2211.02491.pdf

EP R&D

- Compact, low-mass all-silicon tracker
- Retractable vertex detector
- Excellent vertex reconstruction and PID capabilities
- Large acceptance
- Super conduction magnet system
- Continuous readout and online processing



Vertex detector: key characteristics

- 3 detection layers
- Retractable: r_0 = 5 mm
- Material budget: 0.1% X0 / layer
- Spatial resolution 2.5 µm

main R & D challenges

- 10 µm pixel pitch
- Hit rate in the inner layer 1 MHz/mm^2 for a 50 cm barrel
- Tolerant to 1 x 10^{16} 1 MeV n_{eq}/cm^2 + 300 Mrad (numbers are reviewed to lower)
- 70 mW/cm^2: light-weight in-vacuum mechanics and cooling

Specifications of tracker/vertex detector very similar/equivalent to those of FCCee, except at higher radiation levels.
Ideal as a stepping stone towards an FCCee detector.

Perspectives for future HEP detectors: mainstream technologies

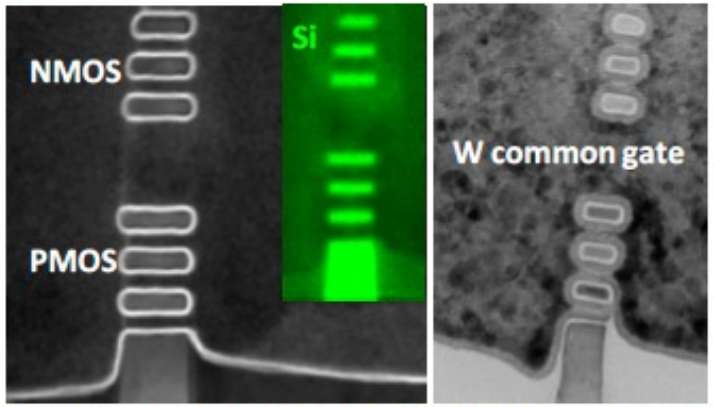
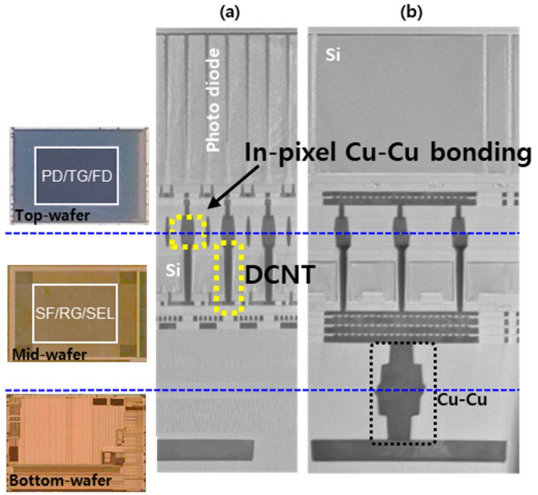
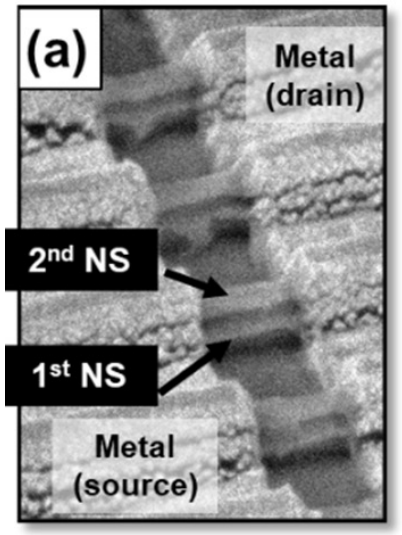


Fig. 5. TEM micrograph shows CFET device after ribbon release on the left demonstrating capable process despite high aspect ratio. TEM micrograph on the right is captured after common-gate fill and polish, showing that the gates of top n-MOS and bottom p-MOS are connected.

Intel IEDM 2023



Samsung IEDM 2023



TSMC IEDM 2023

Mainstream CMOS technology and CMOS imaging sensors for visible light are pushed by artificial intelligence towards wafer stacking and 3D integration.

- Transistor optimization goes 3D, back side power delivery, heterogenous integration, in-memory compute
- Device and Technology Co-Optimization (DTCO) & System and Technology Co-Optimization (STCO) required to meet the challenges
- Smaller feature size for the sensor wafer could bring deeper sub-fF sensor, smaller pitch and easier sensor depletion

Perspectives for future HEP detectors

- Monolithic CMOS sensors crucial for future HEP detectors
- MLR1, ER1 and ER2 experience was essential to learn about the TPSCo 65nm technology, stitching, powering and also yield. Foundry has been very flexible with process modifications in a collaborative effort.
- Submissions so far used to define a custom design flow and support for common run

  see Pedro Leitao's presentation https://indico.cern.ch/event/1553023/
- A smaller pixel pitch, and increased reverse bias are beneficial for sensor radiation tolerance
- Working on a non-stacked sensor for the ALICE3 vertex detector, with very similar requirements as the one for FCC-ee, except a more aggressive radiation tolerance.
- 2 layer wafer stacking offered in this technology will increase cost, but not the thickness, could stack a 65 nm sensor to a 65 nm or 28 nm readout.
- Present evolution towards wafer stacking and 3D integration in mainstream CMOS technology and CMOS imaging sensors for visible light very relevant for future detectors
- Future large area detectors will need concentration of resources in the community to take advantage of the technology evolution in volume production, test, assembly and mounting.

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THANK YOU !