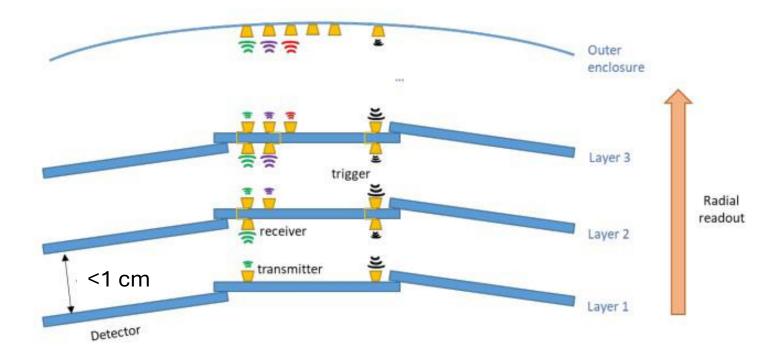
Wireless Communications for FCC-ee

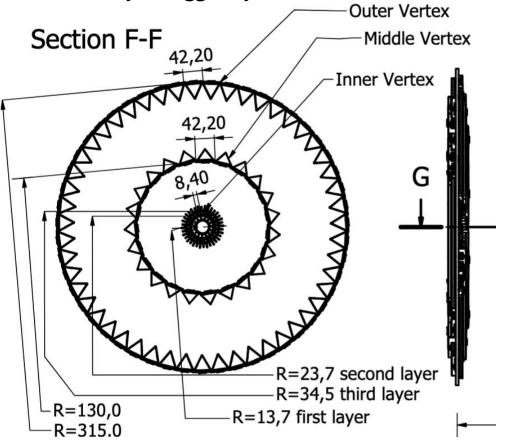
Mainly a summary of the activities of the **WADAPT Collaboration** from the DRD7 Annual workshop presentation and a report of initial tests at UZH

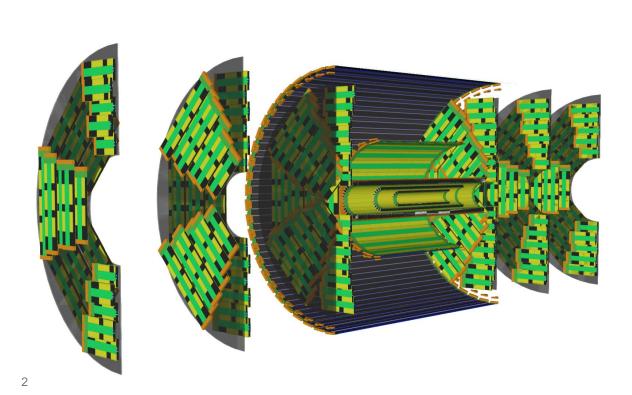
UZH group: Kimia Mirbaghestan, Ben Kilminster, Stefanos Leontsinis, Vagelis Gkougkousis, Armin Ilg, Anna Macchiolo ZHAW group: Luciano Sarperi, Teddy Loeliger, Marc Kuhn



Why wireless?

- Reduction in material budget related to cables and connectors
- Reduced latency: Radial readout instead of axial
- Interlayer intelligence:
 - explore the possibility of identifying hits from "good physics" tracks in L1 by correlating hits in L1 and L2 if an interlayer trigger system is used





Data rates for a Vertex detector at FCC-ee

Silicon data volume Pixels to read out for ARCADIA L1 (15 staves x 6 modules x 2 chips x 640 x256 pixels) \triangleright Z WWZHtt > 7.6 0.5 in 10 µsec window/2-chip module $x10^{3}$ per bunch crossing/2-chip modeule > 23.2 91.8 133.5 380.6 Assuming 32 bits/pixel including time stamp/2-chip module 8.5 1.6 Gbit/s Not triggered **24.4 149** N/AN/A N/A Mbit/s triggered 200 kHz trigger rate ➤ Total layer 1: ■ 2.2 Tbit/sec (NoTrigger) → 13.4 Gbit/sec (Triggered) at Z pole → port card transmission needs 1.1 Tbit or 7 Gbit/s/side Other layers and disks have lower data volumes Current ARCADIA ► Layer 2 has ~10x less data volume Max readout speed achievable on chip 100 - 200 MHz x 32 bits? \rightarrow 3.2 - 6.4 Gbit/sec Untriggered operation looks difficult F. Bedeschi, INFN-Pisa FCC Physics week, Annecy 2024

For Layer 1:

With 100 MHz/cm² incoherent pair hit rate and 32 bits per hit and a double chip module area of 2.05 cm²:

→ 6.6 Gbit/sec per double module

In OCTOPUS we consider to sample both the rising and falling edge for offline ToT measurement

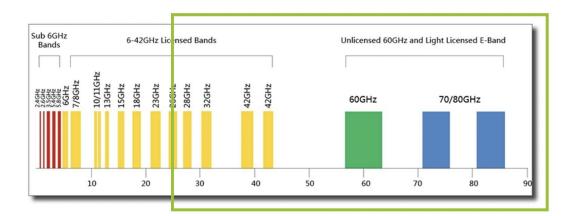
→13.2 Gbit/sec per double module

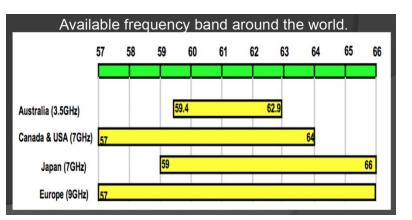
Millimeter Wave

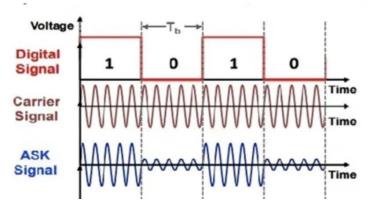
- 1-10 mm wavelength
- 30-300 GHz Carrier frequency
- o 60 GHz band
 - Unlicensed spectrum
 - o Can send **Gigabits/s** data over short distance
 - Low Interference
- Reliable low-cost & low-power technology: most transceivers are fabricated in 65 nm or 28 nm RF CMOS

ASK signal: Amplitude Shift Keying

- •The **amplitude of the carrier wave changes** according to the digital data being transmitted
 - typically a high amplitude for bit "1" and a low or zero amplitude for bit "0".
- •It is a simple form of **digital modulation**, where information is encoded in the **strength of the signal**, while the carrier **frequency (60 GHz) and phase remain constant**.







Antenna parameters

K. Mirbaghestan, UZH and ZHAW

Key Parameters

- Directivity: Focus of radiated power
- Gain: Power output with direction, including efficiency losses
- Bandwidth: Range of operating frequencies
- Max Data Rate without errors:
- Shannon-Hartley capacity formula

$$C = B \log_2(1 + \frac{S}{N})$$

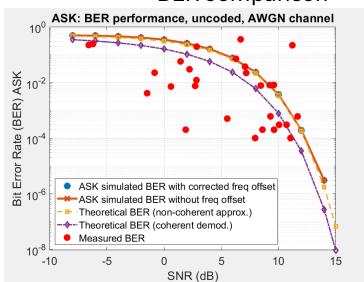
C = maximum data rate (bits/s)

B = channel bandwidth (Hz)

 $\frac{S}{N}$ = signal-to-noise ratio

C = maximum data rate (bits/s)

BER comparison



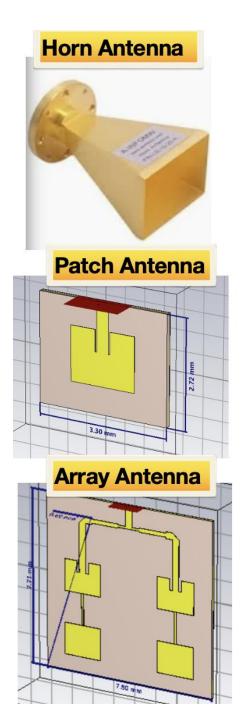
Different Antennas

Horn Antenna: Directional, High gain, Big size

Patch Antenna: Compact, Moderate gain, Narrow bandwidth

Array Antenna: High directivity, Compact -> multiple radiating elements combine

their field constructively in certain direction and destructively in others



Long-range MMW transceiver design









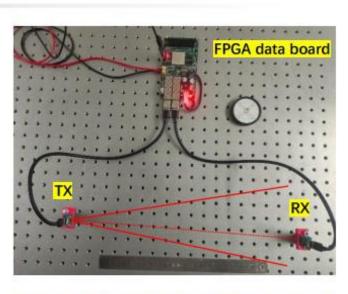
Long-range millimeter-wave transceiver module

- Based on ST60A2 with amplifier
- Utilizing PCB antenna minimizes size and material costs
- Features stamp-hole interface and simplified peripheral circuit
- Dimensions: 14mm x 9mm

Bandwidth test

- The transmission distance has reached
 67.5cm @ 1.25Gbps
- The maximum line speed has reached
 6.6Gbps @ 22.5cm

Modulation supports **ASK (Amplitude Shift Keying)**.



Line rate (Gbps)	Transmit Distance (cm)
1.25	67.5
4	50
5	45
6.6	22.5

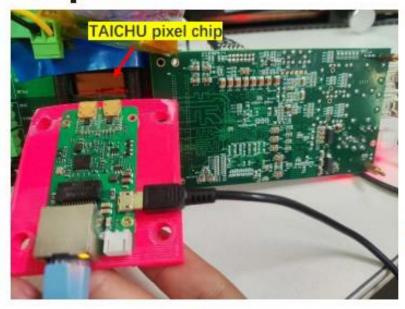
Transmission distance under different line rate

1

Interference with detectors



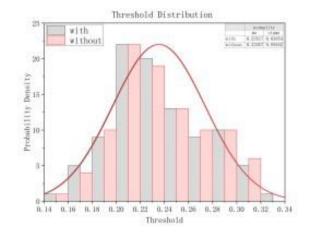
Results by IHEP CAS

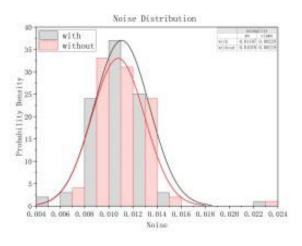


Taichu pixel

mm-wave

- Test with the vertex pixel prototype chip TAICHU3
 - Test two types of modules (short-range and longrange modules).
 - Approach Taichu3 from various directions and distances.
 - Assess the impact on chip threshold and noise levels.
- The test outcomes demonstrate that the influence of 60GHz millimeter waves on the detector signal is minimal.
- Furthermore, the detector signal poses little to no interference with the transmission of millimeter wave signals.

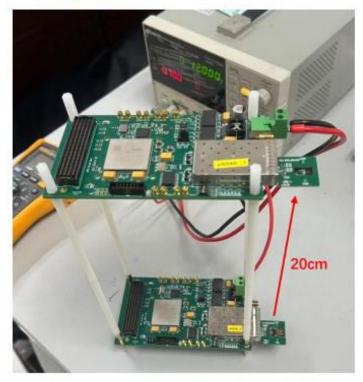




New module test

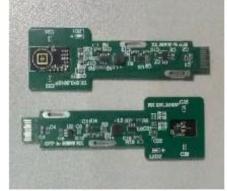


Results by IHEP CAS

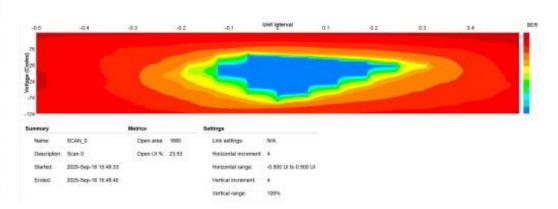


Test setup with new designed SFP module

2005 0 00



Custom-designed module, SFP-packaging compatible.



 Console
 Messages
 Serial I/O Links
 × Serial I/O Scans

 Q
 ★
 +

 Name
 TX
 RX
 Status
 Bits
 Errors
 BER
 BERT Reset
 TX Pattern

 □ Ungrouped Links (0)
 □
 Reset
 PRBS 7-bit
 ∨ PRBS 7-bit
 ∨

 > % Link Group 1 (6)
 □
 Reset
 PRBS 7-bit
 ∨
 PRBS 7-bit
 ∨

 Link 9
 MGT_X0Y1/TX MGT_X0Y1/RX 6.250 Gbps
 2.503...
 0E0
 3.995E-13
 Reset
 PRBS 7-bit
 ∨
 PRBS 7-bit
 ∨

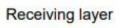
AMD Kintex 7 FPGA ibert test

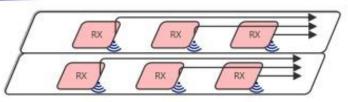
Achieve a BER of 4*E-13 at a maximum line rate of 6.25Gbps.

MMW demonstrator

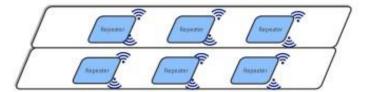


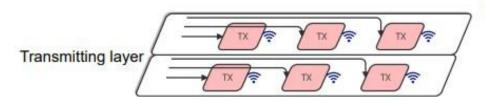
Results by IHEP CAS





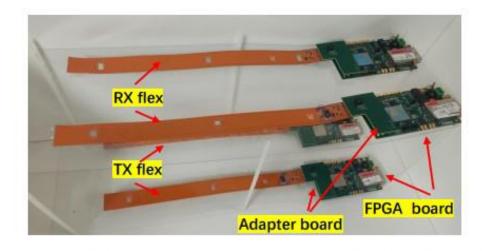
Repeat layer

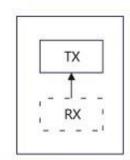




mmWave demonstrator schematic

- · Two flex PCBs per layer.
- Each flex PCB accommodates 3-channel transceiver modules.



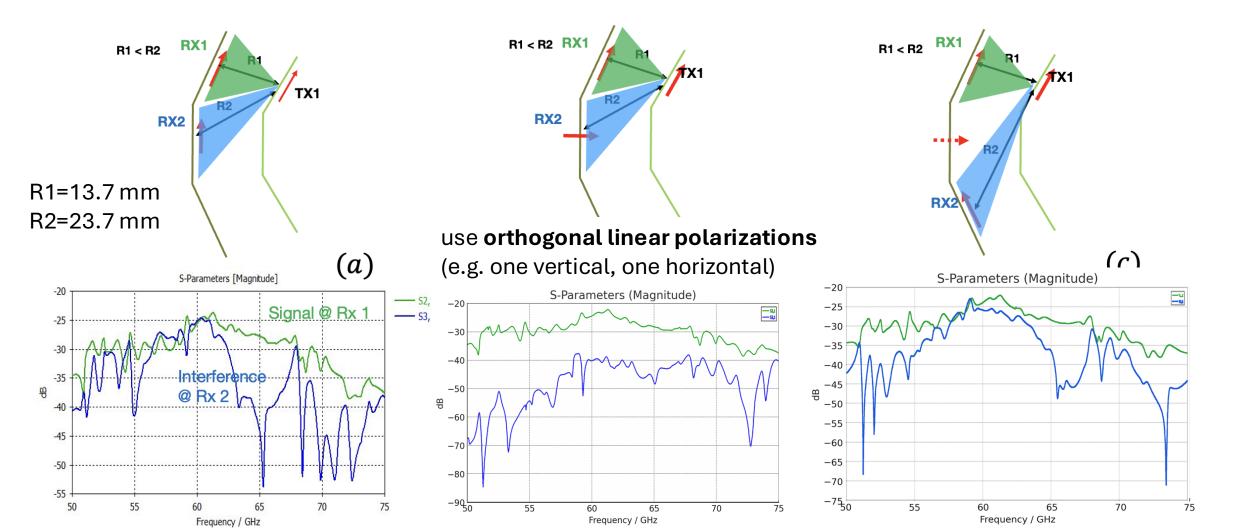


Repeater structure: RX is at the bottom layer of PCB, TX is at the top layer of PCB

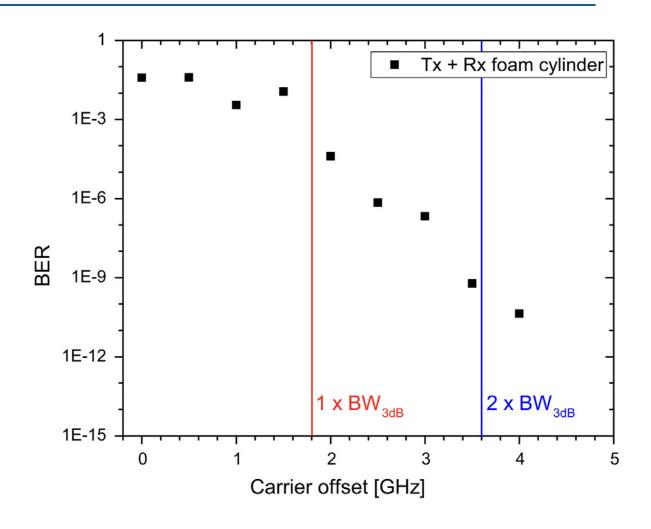
- Most hardware design and production have been completed
 - TX/RX flex PCBs, adapter boards, and FPGA board.
 - Repeater is still under design.
- Prelimilary test with one pair of transceiver module have been completed succesfully.
- This setup mainly focus Multi-channel crosstalk analysis and validation

Signal and interference

- Crosstalk is an issue for high link densities.
- Simulation performed including a homogenous metal layer in L1 and L2 to mimic Alu layers in monolithic sensors



Signal and interference



WADAPT Collaboration <u>Multi Gigabit Wireless</u>

Data Transfer in Detectors at Future Colliders

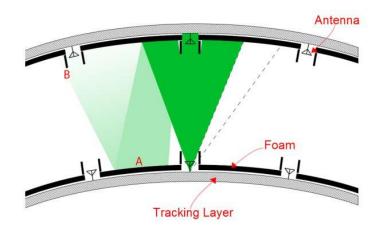
- BER has been measured as a function of the carrier offset when two parallel links are positioned at a pitch of 2.6 cm using the same polarization state
- Carrier frequency offset is varied in steps of 500 MHz
- Three frequency channels in parallel within the full 60 GHz band seems possible:
 - Once the offset exceeds roughly one full bandwidth (around ±1.8 GHz), the two channels are effectively isolated, and the BER approaches the single-link baseline (i.e., almost error-free).

Small carrier offsets may effectively isolate adjacent channels within the 60 GHz band

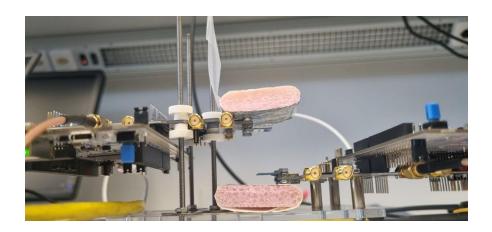
Vertex detector simulation

60 GHz setup with Patch antennas

- Test the new setup with 2 small patch antennas
- Aluminum layer to mimic layers in monolithic sensors
- Added foam to reduce reflections
- Measured the RSSI (Signal Strength)



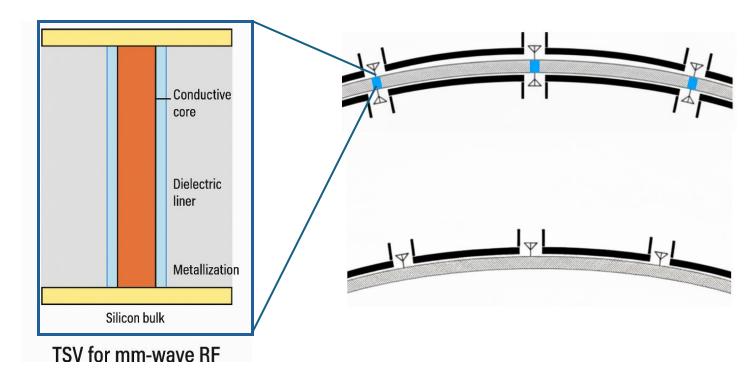
 Need flexes instead of rigid boards to insert the antennas in the Vertex mock-up





Bringing signals across a layer

Through Silicon Vias could be a good solution to get RF from one side of a monolithic sensor to the other **as a matched vertical feed** (signal via + ground fence) that connects transmission lines or an antenna on the far side.



Implementation of transducers and antenna in CMOS requires:

- High resistivity substrates
- Thick top metals (2–4 µm Cu or Al) for low-loss inductors, transmission lines, and antennas
- Calibrated S-parameter transistor models up to mmWave frequencies

Conclusions and outlook

First steps towards a feasibility study

- 60 GHz wireless links achieve multi-Gb/s rates over few cm distances
- compatible with FCC-ee vertex geometry.

•Crosstalk mitigation:

- •Orthogonal polarizations and small carrier offsets may effectively isolate adjacent channels within the 60 GHz band.
- •Integration potential: RF transceivers in 65 nm–28 nm CMOS enable compact, low-power, low-mass data transfer
 - •Will it be possible to implement these design feature in the CMOS technology used for MAPs?

•Next steps:

- Extend tests with realistic sensor stack (Al layers + carbon support).
- Characterize BER stability and timing jitter under varying conditions.
- Explore TSV-based vertical feedthroughs for signal routing across layers.
- Estimation of the required power for wireless transmission once embedded in the MAPs
- Qualify radiation tolerance of RF CMOS front-ends.
- Full system design and test

•Goal:

• Establish feasibility of wireless readout as a viable low-mass interconnect technology for the FCC-ee vertex detector.